

# SANYO Semiconductors DATA SHEET



## **CMOSIC** LC72F3781 — Electronic tuning radio for car audio **ETR Controller**

### Overview

The LC72F3781 is a ETR controller with an on-chip one-time PROM for use with the LC723781N, 2N, 3N, 4 and 5 mask versions. Since it has the equivalent electrical performance, pin layout and package as these mask versions, it is ideally suited for checking program operations, starting the initial shipment of finished products and reducing the switchover time frame when specifications are changed.

The PROM size is 128 Kbytes ( $64K \times 16$  bits).

### **Functions**

• ROM	: Up to 64K steps (65,535×16-bits)
	The subroutine area holds 4K steps (4,096×16-bits)
• RAM	: Up to 16K×4-bits (In banks 00 through FF)
Stack	: 32levels
• Serial I/O	<ul> <li>Three channels. These circuits can support both 2-wire and 3-wire 8-bit communication techniques, and can be switched between MSB first and LSB first operation.</li> <li>One of six internally generated serial transfer clock rates can be selected: 12.5kHz, 37.5kHz, 187.5kHz, 281.25kHz, 375kHz, and 450kHz</li> </ul>
• External interrupts	: Seven interrupt inputs (pins INT0 through INT5, and the HOLD pin) These interrupts can be set to switch between rising and falling edges, although the HOLD pin only supports falling edge detection.
• Internal interrupts	: Seven interrupts ; four internal timer interrupts, and three serial I/O interrupts.

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• Interrupt nesting levels	: 14 levels Interrupts are prioritized in hardware as follows : HOLD pin>INT0 pin>INT1 pin>INT2 pin>INT3 pin>INT4 pin>INT5 pin> S-I/O0>S-I/O1>S-I/O2>Internal TMR0>Internal TMR1>Internal TMR2>
• A/D Converter	• 8 bit resolution and 8 inputs
General purpose ports	: Input ports : 13
• General-purpose ports	Output ports : 15
	U/O ports : 62 (These pins can be switched between input and output in 1 bit units.)
• PLI block	: Includes a sub charge pump for high speed locking
• I LL DIOCK	Supports dead zone control
	Built in unlock detection circuit
	Turalya reference frequencies : 1kHz, 2kHz, 2 125kHz, 5kHz, 6 25kHz, 0kHz
	10kHz 12 5kHz 25kHz 20kHz 50kHz and 100kHz
	This 20 hit counter can be used for either frequency or period recommendation
Universal counter	: This 20-bit counter can be used for either frequency or period measurement and
- T.	supports four measurement (calculation) periods : Tins, 4ms, 8ms, and 32ms
• Timers	The second secon
	TMR0 : Supports four periods : 10µs, 100µs, 1ms, and 5ms
	TMR1 : Supports four periods : 10µs, 100µs, 1ms, and 10ms
	IMR2 and IMR3 : Programmable 8-bit counters.
	Input clocks with $10\mu s$ , $100\mu s$ , and $1ms$
D	One 125-ms timer flip-flop provided
• Beep circuit	: Provides 12 fixed beep tones :
	500Hz, 1kHz, 2kHz, 2.08kHz, 2.2kHz, 2.5kHz, 3kHz, 3.125kHz, 3.33kHz, 3.75kHz, 4.17kHz, and 7.03kHz
	Programmable 8-bit beep tone generator.
	Reference clocks with frequencies of 50kHz, 15kHz, and 5kHz.
• Reset	: Built-in voltage detection reset circuit
	External reset pin
• Cycle time	: 1.33µs/833ns (All instructions are one word), X'tal : 4.5MHz/7.2MHz
	Supports software switching (Initial cycle time is 1.33µs)
• Halt mode	: The microcontroller operating clock is stopped in Halt mode.
	There are four conditions that can clear Halt mode : Interrupt requests,
	timer flip-flop overflows, port PA inputs, and HOLD pin inputs.
• Operating supply voltage	: 4.5 to 5.5V (Microcontroller block only : 3.5 to 5.5V)
• Package	: QIP100E
• Development tools	: Emulator : RE128V
•	Evaluation chip : LC72EV3780
	Evaluation board : EB-72EV3780

## Specifications

## Absolute Maximum Ratings at $Ta=25^\circ C \ V_{SS}=0 V$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V <sub>DD</sub> max		-0.3 to +6.5	V
Input voltage	V <sub>IN</sub> 1	PC-PORT	-0.3 to +8	V
	V <sub>IN</sub> 2	All input pins other than $V_{IN}$ 1	-0.3 to V <sub>DD</sub> +0.3	V
Output voltage	VOUT1	PJ-PORT	-0.3 to +14	V
	V <sub>OUT</sub> 2	PC-PORT	-0.3 to +8	V
	V <sub>OUT</sub> 3	All input pins other than $V_{\mbox{OUT}}1$ and $V_{\mbox{OUT}}2$	-0.3 to V <sub>DD</sub> +0.3	V
Output current	IOUT1	PC, PJ-PORT	0 to +5	mA
	I <sub>OUT</sub> 2	PB, PD, PE, PF, PG, PK, PL, PM, PN, PO, PP PQ, PR, PS, PT-PORT, EO1, EO2, SUBPD	0 to +3	mA
Allowable power dissipation	Pd max	Ta = -40 to +85 °C	400	mW
Operating temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-40 to +125	°C

## Allowable Operating Range at Ta = -40 to +85°C, $V_{DD}$ = 3.5 to 5.5V

Deremeter	Symbol	Ding				
Falameter	Symbol	FIIIS	min	typ	mx	uit
Supply voltage	V <sub>DD</sub> 1	CPU and PLL operation	4.5	5.0	5.5	
	V <sub>DD</sub> 2	CPU operation	3.5		5.5	V
	V <sub>DD</sub> 3	Memory retention	1.1		5.5	
Input high-level voltage	V <sub>IH</sub> 1	PB, PC, PH, PI, PL, PM, PN, PP, PO, PQ, PR, PS, PT-PORT, HCTR, LCTR, INEO, SUBPD (with the I/O ports set to input mode)	0.7V <sub>DD</sub>		V <sub>DD</sub>	V
	V <sub>IH</sub> 2	PD, PE, PF, PG, PK-PORT, LCTR (in period measurement mode), HOLD, RESET	0.8V <sub>DD</sub>		V <sub>DD</sub>	V
	V <sub>IH</sub> 3	SNS	2.5		V <sub>DD</sub>	V
	V <sub>IH</sub> 4	PA-PORT	0.6V <sub>DD</sub>		V <sub>DD</sub>	V
Input low-level voltage	V <sub>IL</sub> 1	PB, PC, PH, PI, PL, PM, PN, PP, PO, PQ, PR, PS, PT-PORT, HCTR, LCTR, INEO, SUBPD (with the I/O ports set to input mode)	0		0.3V <sub>DD</sub>	V
	V <sub>IL</sub> 2	PA, PD, PE, PF, PG, PK-PORT, LCTR (in period measurement mode), RESET	0		0.2V <sub>DD</sub>	V
	V <sub>IL</sub> 3	SNS	0		1.1	V
	V <sub>IL</sub> 4	HOLD	0		0.4V <sub>DD</sub>	V
Input frequency	F <sub>IN</sub> 1	XIN	4.0	4.5	8.0	MHz
	F <sub>IN</sub> 2	FMIN : V <sub>IN</sub> 2, V <sub>DD</sub> 1	10		150	MHz
	F <sub>IN</sub> 3	FMIN : V <sub>IN</sub> 3, V <sub>DD</sub> 1	10		130	MHz
	F <sub>IN</sub> 4	AMIN(H) : V <sub>IN</sub> 3, V <sub>DD</sub> 1	2.0		40	MHz
	F <sub>IN</sub> 5	AMIN(L) : V <sub>IN</sub> 3, V <sub>DD</sub> 1	0.5		10	MHz
	F <sub>IN</sub> 6	HCTR : V <sub>IN</sub> 3, V <sub>DD</sub> 1	0.4		12	MHz
	F <sub>IN</sub> 7	LCTR : V <sub>IN</sub> 3, V <sub>DD</sub> 1	100		500	kHz
	F <sub>IN</sub> 8	LCTR (in period measurement) : VIH2, VIL2, VDD1	1		20×10 <sup>3</sup>	Hz
Input amplitude	V <sub>IN</sub> 1	XIN	0.5		1.5	Vrms
	V <sub>IN</sub> 2	FMIN	0.07		1.5	Vrms
	V <sub>IN</sub> 3	FMIN, AMIN, HCTR, LCTR	0.04		1.5	Vrms
Input voltage range	V <sub>IN</sub> 6	ADI0 to ADI7	0		V <sub>DD</sub>	V

### Electrical Characteristics in the allowable operating ranges

Deremeter	Sumbal	Ding		Ratings		upit
Parameter Symbol		PINS	min	typ	max	unit
Input high-level current	I <sub>IH</sub> 1	$XIN : V_I = V_{DD} = 5.0V$	2.0	5.0	15	μΑ
	I <sub>IH</sub> 2	FMIN, AMIN, HCTR, LCTR : $V_I = V_{DD} = 5.0V$	4.0	10	30	μΑ
	I <sub>IH</sub> 3	PA, PB, PC, PD, PE, PF, PG, PH, PI, PK, PL, PM, PN, PO, PP, PQ, PR, PS, PT-PORT, $\overline{SNS}$ , $\overline{HOLD}$ , $\overline{RESET}$ , HCTR, LCTR, INEO, SUBPD : V <sub>I</sub> = V <sub>DD</sub> = 5.0V (with the ports PB, PC, PD, PE, PF, PG, PK, PL, PM, PN, PP, PO, PQ, PR, PS, and PT-PORT set to input mode)			3	μΑ
Input low-level current	I <sub>IL</sub> 1	$XIN : V_I = V_{DD} = V_{SS}$	2.0	5.0	15	μΑ
	I <sub>IL</sub> 2	FMIN, AMIN, HCTR, LCTR : $V_I = V_{DD} = V_{SS}$	4.0	10	30	μΑ
	IIL3	PA, PB, PC, PD, PE, PF, PG, PH, PI, PK, PL, PM, PN, PO, PP, PQ, PR, PS, PT-PORT, $\overline{SNS}$ , $\overline{HOLD}$ , $\overline{RESET}$ , HCTR, LCTR, INEO, SUBPD : V <sub>I</sub> = V <sub>SS</sub> (with the ports PB, PC, PD, PE, PF, PG, PK, PL, PM, PN, PP, PO, PQ, PR, PS, and PT-PORT set to input mode)			3	μΑ
Hysteresis	VH	PD, PE, PF, PG, PK-PORT, RESET, LCTR (in period measurement)	0.1V <sub>DD</sub>	0.2V <sub>DD</sub>		V
Output high-level voltage	V <sub>OH</sub> 1	PB, PD, PE, PF, PG, PK, PL, PM, PN, PO, PP, PQ, PR, PS, PT-PORT : $I_O = -1mA$	V <sub>DD</sub> -1.0			V
	V <sub>OH</sub> 2	EO1, EO2, SUBPD : Ι <sub>Ο</sub> = -500μΑ	V <sub>DD</sub> -1.0			V
	V <sub>OH</sub> 3	XOUT : Ι <sub>Ο</sub> = -200μA	V <sub>DD</sub> -1.0			V
Output low-level voltage	V <sub>OL</sub> 1	PB, PD, PE, PF, PG, PK, PL, PM, PN, PO, PP PQ, PR, PS, PT-PORT : I <sub>O</sub> = -1mA			1.0	V
	V <sub>OL</sub> 2	EO1, EO2, SUBPD : Ι <sub>Ο</sub> = -500μΑ			1.0	V
	V <sub>OL</sub> 3	XOUT : Ι <sub>Ο</sub> = -200μA			1.5	V
	V <sub>OL</sub> 4	PC, PJ-PORT : I <sub>O</sub> = -5mA			2.0	V
Output off leakage current	IOFF <sup>1</sup>	PB, PD, PE, PF, PG, PK, PL, PM, PN, PO, PP, PQ, PR, PS, PT-PORT	-3		+3	μΑ
	IOFF2	EO1, EO2, SUBPD	-100		+100	nA
	I <sub>OFF</sub> 3	PC, PJ-PORT	-5		+5	μA
A/D conversion error		ADI0 to ADI7	-1.5		+1.5	LSB
Rejected pulse width	PREJ1	SNS			50	μs
Power down detection voltage	VDET		2.7	3.0	3.3	V
Power supply current	I <sub>DD</sub> 1	V <sub>DD</sub> 1 : F <sub>IN</sub> 2 = 130MHz Ta = 25°C		5	10	mA
	I <sub>DD</sub> 2	V <sub>DD</sub> 1 : F <sub>IN</sub> 2 = 130MHz Ta = 25°C		5.5	11	mA
	I <sub>DD</sub> 3	V <sub>DD</sub> 2 : Halt mode Ta = 25°C, X'tal : 4.5 MHz		0.45		mA
	I <sub>DD</sub> 4	V <sub>DD</sub> 2 : Halt mode Ta = 25°C, X'tal : 7.2MHz		0.55		mA
	I <sub>DD</sub> 5	Backup mode (OSC stopped) $V_{DD} = 5.5V$ , Ta = 25°C *2 (Fig. 2)			5	μΑ
	IDD6	Backup mode (OSC stopped) V <sub>DD</sub> = 2.5V, Ta = 25°C *2 (Fig. 2)			1	μΑ

\*1 : Twenty instruction steps are executed every millisecond. The PLL, universal counter, and other functions are stopped.

## **Test Circuits**





ILC05526

Figure 2. IDD3 and IDD4 in Backup Mode



## **Package Dimensions**

**Pin Assignment** 



ILC05527

### **Block Diagram**



No.0459-7/17

## **Pin Description**

Pin name	Pin No.	I/O	Pin explanation	Equivalent circuit
PA0 PA1 PA2 PA3	32 31 30 29	I	Dedicated input ports. These ports are designed with a low threshold voltage. Input is disabled in Backup mode.	BACK UP
PB0 PB1 PB2 PB3	28 27 26 25	I/O	General-purpose I/O ports. The mode (input or output) is set using the IOS2 instruction. Input is disabled and the pins go to the high-impedance state in Backup mode. These ports are set up as general-purpose input ports after a power on reset.	BACK UP
PC0 PC1 PC2 PC3	24 23 22 21	I/O	General-purpose I/O ports (middle-voltage input and output). The mode (input or output) is set using the IOS2 instruction. External pull-up resistors are required since the output circuits are open drain. Input is disabled and the pins go to the high-impedance state in Backup mode. These ports are set up as general-purpose input ports after a power on reset.	BACK UP
PD0/INT4 PD1/INT5 PD2 PD3	20 19 18 17	1/0	<ul> <li>General-purpose I/O and external interrupt shared function ports.</li> <li>The input formats are Schmitt inputs.</li> <li>The external interrupt function is enabled when the external interrupt enable flag is set.</li> <li>When used as general-purpose I/O ports :</li> <li>The mode (input or output) is set in 1-bit units using the IOS2 instruction.</li> <li>When used as external interrupt pins :</li> <li>The external interrupt functions are enabled by setting the corresponding external interrupt enable flag (INT4EN or INT5EN). In this case, the pins must be set to input mode in advance.</li> <li>Input is disabled and the pins go to the high-impedance state in Backup mode.</li> <li>These ports are set up as general-purpose input ports after a power on reset.</li> </ul>	BACK UP

Continued from preceding page.						
Pin name	Pin No.	I/O	Pin explanation	Equivalent circuit		
PE0	16	I/O	General-purpose I/O ports with shared functions as serial I/O ports.			
PE1/SCK2	15		The input formats are Schmitt inputs. The PE1/SCK2 and PE2/SO2			
PE2/SO2	14		pins can be switched to function as open drain outputs.			
PE3/SI2	13		The IOS1 instruction is used to switch between the general-purpose	BACK UP		
PF0	12		I/O port and serial I/O port functions.			
PF1/SCK1	11		When used as general-purpose I/O ports :			
PF2/SO1	10		The pins are set to the general-purpose I/O port function using the			
PF3/SI1	9		IOS1 instruction.			
PG0	8		The mode (input or output) is set in 1-bit units using the IOS1	ILC05532		
PG1/SCK0	7		instruction			
PG2/SO0	6		When used serial I/O ports :			
PG3/SI0	5		The pins are set to the serial I/O port function using the IOS1 instruction.			
			[Pin states when set to the serial I/O port function]			
			PE0, PF0, PG0 General-purpose I/O	BACK UP		
			PE1, PF1, PG1 SCK input or output			
			PE2, PF2, PG2 SO output			
			PE3, PF3, PG3 SI input	Open drain Control		
			The PE1/SCK2 and PE2/SO2 pins can be switched to function as			
			open drain outputs with the IOS2 instruction. When using this circuit			
			type, the external pull-up resistors must be connected to the same			
			power supply as that used by the IC.	PE1/PE2-Port		
			Input is disabled and the pins go to the high-impedance state in	IL C05522		
			Backup mode.	11203555		
			These ports are set up as general-purpose input ports after a power			
N/IN/			on reset.			
XIN	1		Connections for 4.5MHz/7.2MHz crystal oscillator element			
2001	100	0				
				+		
				XOUT Ļ		
				ILC05534		
EO1	98	0	Main charge pump outputs.	. <del>•</del>		
EO2	97		These pins output a high level when the frequency of the local			
			oscillator divided by n is higher than that of the reference frequency,			
			and they output a low level when that frequency is lower.			
			They go to the high-impedance state when the frequencies match.			
			These pins go to the high-impedance state in Backup mode, after a	1 777 ILC05535		
			power on reset, and in the PLL stopped state.			
V <sub>DD</sub> PORT	39	-	Power supply connections.			
VDDPLL	93		The VDDPORT and VSSPORT pins are mainly supply power for the			
V <sub>SS</sub> CPU	4		peripheral I/O blocks.			
VSSPURI	40		The VDPLL and VSSPLL pins are mainly for the PLL circuits and			
VacPU	01		The VeeCPLL bin is mainly used by the CPLL block			
VSSPLL	90		The VocADC bin is mainly used by the ADC block.			
			Since all the Vop and Vop nins are independent all must be			
			connected to the same power supply			
VREG	3	0	Internal low voltage output			
	J	Ŭ	Connect a bypass capacitor to this pin.			

Din r		page.			Din evaluation	
Pin name	Pin No.	I/O			Pin explanation	Equivalent circuit
FMIN	95	I	FM VCC	) (local o	scillator) input.	
				IS SELECT		
			The sign	al input i	to this pin must be capacitor coupled.	
				disabled	In Backup mode, after a power on reset, and in the	. <u> </u>
	0.1		PLL Stop	ped stat		
AMIN	94	1	AM VCC	) (local o	scillator) input.	
			I nis pin	is select	ed and the band set with CW1 (b1, b0) in the PLL	┆──┿┷╌╱╱╌┷╴
			Instructio	on.		
			b1	b0	Band	
			1	0	2 to 40MHz (SW, AM upconversion)	ILC05536
			1	1	0.5 to 10MHz (MW, LW)	
			The sign	al input	to this pin must be capacitor coupled.	
			Input is o	disabled	in Backup mode, after a power on reset, and in the	
			PLL stop	ped stat	е.	
SUBPD	92	I/O	Sub-cha	rge pum	p output and general-purpose input shared function	
			port.			
			The IOS	2 instruc	tion is used for switching between the sub-charge	
			pump ou	tput and	general-purpose input functions.	
			<ul> <li>When</li> </ul>	used as	the sub-charge pump output :	
			The su	b-charge	e pump output function is set up with the IOS2	
			instruc	tion.		
			A high-	-speed lo	ocking circuit can be formed by using this pin in	BACK UP
			conjun	ction with	n the main charge pump.	
			The su	b-charge	pump is controlled using the DZC instruction.	
			b3	b2	Operation	
			0	0	High impedance	┆╴╺┼╼
			0	1	Only operates when the PLL is unlocked	
			0	'	(450kHz)	· · · · · · · · · · · · · · · · · · ·
			1	0	Only operates when the PLL is unlocked	ILC05537
				-	(900kHz)	
			1	1	Normal operation	
			<ul> <li>When</li> </ul>	used as	a general-purpose input :	
			The ge	neral-pu	rpose input function is set up with the IOS2	
			instruc	tion.		
			Data is	read fro	m the port using the INR instruction.	
			This pin	goes to t	the high-impedance state in Backup mode, after a	
		<u> </u>	power of	n reset, a	and in the PLL stopped state.	
INEO	91		Dedicate	ed input p	DOR.	1
			Data is r	ead from	i the port using the INK Instruction	BACK UP
			Input is o	disabled	п васкир тоде.	
						ILC05538

Continued from preceding page.							
Pin name	Pin No.	I/O	Pin explanation	Equivalent circuit			
LCTR	90 90 89	1	<ul> <li>Pin explanation</li> <li>Universal counter and general-purpose input shared function input port.</li> <li>The IOS1 instruction is used for switching between the universal counter and general- purpose input functions.</li> <li>When used for frequency measurement :</li> <li>The universal counter function is set up with the IOS1 instruction.</li> <li>The counter is controlled using UCS and UCC instructions.</li> <li>Since this pin functions as an AC amplifier in this mode, the input signal must be input with capacitor coupling.</li> <li>When used as a general-purpose input pin :</li> <li>The general-purpose input function is set up with the IOS1 instruction.</li> <li>Data is read from the port using the INR (b0) instruction.</li> <li>Input is disabled in Backup mode. (The input pin will be pulled down.)</li> <li>The universal counter function is selected after a power on reset.</li> <li>Universal counter (frequency or period measurement) and general-purpose input port.</li> <li>The IOS1 instruction is used for switching between the universal</li> </ul>	Equivalent circuit			
			<ul> <li>counter and general-purpose input functions.</li> <li>When used for frequency measurement : The universal counter function is set up with the IOS1 instruction. Set up LCTR frequency measurement mode with the UCS instruction, and control operation with the UCC instruction. Since this pin functions as an AC amplifier in this mode, the input signal must be input with capacitor coupling.</li> <li>When used for period measurement i The universal counter function is set up with the IOS1 instruction. Set up LCTR frequency measurement : The universal counter function is set up with the IOS1 instruction. Set up LCTR frequency measurement mode with the UCS instruction, and control operation with the UCC instruction. Since the bias feedback resistor is disconnected in this mode, the input signal must be input with DC coupling.</li> <li>When used as a general-purpose input pin : The general-purpose input port function is set up with the IOS1 instruction. Data is read from the port using the INR (b1) instruction. Input is disabled in Backup mode. (The input pin will be pulled down.) The universal counter function (HCTR frequency measurement mode) is selected after a power on reset.</li> </ul>	ILC05536			
SNS	88	I	<ul> <li>Voltage sense and general-purpose input shared function port.</li> <li>This input circuit is designed with a low input threshold voltage.</li> <li>When used as a voltage sense input : <ul> <li>The pin is used to test for power failures on the return from Backup mode.</li> </ul> </li> <li>Application can test this condition using the internal SNS flip-flop. <ul> <li>The SNS flip-flop can be tested with the TST instruction.</li> <li>(This usage requires external components, capacitors and resistors.</li> <li>For the sample application circuit, see the user's manual.)</li> <li>When used as a general-purpose input port the pin state can be tested with the TST instruction.</li> <li>Unlike the other input ports, input to this pin is not disabled in Backup mode and after a power on reset. As a result, through currents must be taken into account when designing applications that use this pin as a general-purpose input.</li> </ul> </li> </ul>				
HOLD	87	I	Power supply monitor (with interrupt function) This is designed with a high input threshold voltage. This pin is normally connected to the ACC line and used for power off detection. When a power off state is detected, the HOLDON flag and the hold interrupt request flag will be set. To enter Backup mode, execute a CKSTP instruction when the HOLD pin is low. Set this pin high to clear Backup mode.	↓ ↓ ILC05539			

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Pin name	Pin No.	I/O	Pin explanation	Equivalent circuit				
RESET	86	I	System reset pin. When the CPU is operating or in Halt mode, the system is reset when this pin is held low for at least one machine cycle. Execution starts with the PC pointing to location 0. At this time the SNS flip-flop is set. A low level must be applied for at least 50ms when power is first applied.	ILC05540				
PH0/ADI0	85	I	General-purpose input and A/D converter input shared function ports.					
PH1/ADI1	84		The IOS1 instruction is used to switch between the general-purpose					
PH2/ADI2	83		input and the A/D converter input functions.					
PH3/ADI3	82		When used as general-purpose input ports :					
PI0/ADI4	81		The general-purpose input port function is set up with the IOS1					
PI1/ADI5	80		instruction. (In bit units)					
PI2/ADI6	79		When used as A/D converter input pins :					
PI3/ADI7	78		<ul> <li>The A/D converter input port function is set up with the IOS1 instruction. (In bit units)</li> <li>The pin whose voltage is to be converted is specified with the IOS1 instruction, and the conversion is started with UCC instruction.</li> <li>Note : Since input is disabled for ports specified for the ADI function, executing an input instruction for such a port will always return a low level.</li> <li>Input is disabled in Backup mode.</li> <li>These ports are set up as general-purpose input ports after a power on reset.</li> </ul>	To the A/D converter input ILC05541				
PJ0	76	0	General-purpose output ports (high-voltage output)					
PJ1	75		Since these are open-drain output circuits, external pull-up resistors	BACK UP				
PJ2 PJ3	74 73		are required. The internal transistors are turned off (resulting in a high-level output) in Backup mode and after a power on reset.	ILC05542				
PK0/INT0	72	I/O	General-purpose I/O and external interrupt shared function ports.					
PK1/INT1	71		The input formats are Schmitt inputs.					
PK2/INT2 PK3/INT3	70 69		The external interrupt function is enabled when the external interrupt enable flag is set.					
			<ul> <li>When used as general-purpose I/O ports : The mode (input or output) is set in 1-bit units using the IOS1 instruction.</li> <li>When used as external interrupt pins : The external interrupt functions are enabled by setting the corresponding external interrupt enable flag (INT0EN through INT3EN). Here, the pins must be set to input mode in advance. Input is disabled and the pins go to the high-impedance state in Backup mode. These ports are set up as general-purpose input ports after a power on recet</li> </ul>	BACK UP				

Continued from preceding page.							
Pin name	Pin No.	I/O	Pin explanation	Equivalent circuit			
Pin name PL0 to 3 PM0 to 3 PN0/BEEP PN1 PN2 PN3	Pin No. 68 to 61	1/O 1/O	Pin explanation General-purpose I/O ports The mode is switched between input and output with the IOS instruction. Input is disabled and the pins go to the high-impedance state in Backup mode. These ports are set up as general-purpose input ports after a power on reset. General-purpose I/O port and beep tone output shared function ports. The IOS2 instruction is used to switch between the general-purpose I/O port and the beep tone output functions. • When used as general-purpose I/O ports : The general-purpose I/O port function is set up with the IOS2 instruction. (Pins PN1 through PN3 are dedicated general-purpose output pins.) • When used as the beep tone output pin : The beep tone output function is set up with the IOS2 instruction. The frequency is set up with the BEEP instruction. When this pin is used as the beep tone output pin, executing an output instruction for this pin only sets the internal latch and has no influence on the output. Input is disabled and the pins go to the high-impedance state in Backup mode. These ports are set up as general-purpose input ports after a power	Equivalent circuit BACK UP			
PO0 to 3 PP0 to 3	56 to 49	I/O	General-purpose I/O ports The mode is switched between input and output with the IOS instruction. Input is disabled and the pins go to the high-impedance state in Backup mode. These ports are set up as general-purpose input ports after a power on reset.				
PQ0 to 3 PR0 to 3 PS0 to 3 PT0 to 3	48 to 41 38 to 33	I/O	General-purpose I/O ports. The mode is switched between input and output with the IOS instruction, and data is input with the INR instruction and output with the OUTR instruction. The SPB, RPB, TPT, and TPF instruction cannot be used with these ports. Input is disabled and the pins go to the high-impedance state in Backup mode. These ports are set up as general-purpose input ports after a power on reset.	BACK UP			
TEST1	99		LSI test pins.				
TEST2	2		These pins must be connected to GND.				

### Concerning Differences from the LC723781N, 2N, 3N, 4 and 5 Mask Versions

Item	Mask version (LC723781N, 2N, 3N, 4 and 5)	OTP version (LC72F3781)
Design rule	0.35μ process	0.45µ process
ROM	Masked ROM structure	Flash ROM structure
Write mode	Not available	Available

### **Design Considerations**

- 1) Although the electrical specifications are the same for the mask and OTP versions, differences may arise in the actual values for the threshold level of the input ports, output current of the output ports, input sensitivity, etc. Variations may also be found from lot to lot. It must therefore be kept in mind that if finished products are designed using the actual values of the samples, these variations may prevent the finished products from operating.
- 2) The undesirable radiation level is not listed among the specifications. Since differences may arise between the mask and OTP versions, this must be kept in mind when designing the finished products.

### **Concerning ROM Writing**

- 1) The job of writing data onto the ROM in-house at SANYO Semiconductor is not currently supported.
- 2) The LC72F3781 circuit board must be requested as the data writing board.
- 3) The AF-9706 or AF-9708 made by Ando or the 1890A or 1881XP made by Minato is recommended as the ROM writer.

### Example of Writing Data onto the on-chip Flash ROM of the LC72F3781

(using the AF-9706 or AF-9708)

I. Writing the data using the AF-9706 or AF-9708 (made by Ando) PROM programmer

1. ROMTYPE settings

ROMTYPE	$\rightarrow$	Select [MAKER]	$\rightarrow$	SET
	$\rightarrow$	Select [SST]	$\rightarrow$	SET
	$\rightarrow$	Select [29EE010]	$\rightarrow$	SET

2. Start/stop address settings

 $FUNCTION \rightarrow$ 1 : Address setting mode

\* The address that corresponds to the ROM capacity provided in the table below must be set as the stop address.

Type No.	ROM capacity	Stop address	
LC723781N	40KB	9FFF	
LC723782N	48KB	BFFF	
LC723783N	64KB	FFFF	
LC723784	96KB	17FFF	
LC723785	128KB	1FFFF	

3. Executing data erasure

DEVICE	$\rightarrow$	В	$\rightarrow$	SET	: For data erasure execution.
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4. Executing data writing

DEVICE	$\rightarrow$	F	$\rightarrow$	SET	: For program and verify execution.
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II. Writing board

The writing board is shown in the figure below. The position of pin 1 must be checked before connecting to the EPROM programmer.



Pin 1 of EPROM programmer

Note: The writing adapter has been changed.

To be used for the general-purpose EPROM programmer: Model LC72F3781-ADP-N EPROM programmer

### Example of writing data onto the on-chip Flash ROM of the LC72F3781

ENTRY

(using the 1890A)

- I. Data writing method
- 1. ROMTYPE settings

 $\boxed{\text{DEVICE}} \rightarrow \text{D734}$ 

ENTRY : Device code [29EE010]

2. Start/stop address settings

```
\begin{array}{ccc} \hline EDIT & \rightarrow & \hline PAE \end{array} : Address setting mode \\ \end{array}
```

<1> Since BEGIN ADD is displayed, 00000  $\rightarrow$  <2> Since END ADD is displayed, 1FFFF  $\rightarrow$ 

<u>ENTRY</u> (128kbytes = 1FFFF)

<3> Since BUF ADD is displayed, 00000  $\rightarrow$  (

ENTRY

\* The address that corresponds to the ROM capacity provided in the table below must be set as the stop address.

Type No.	ROM capacity	Stop address
LC723781N	40KB	9FFF
LC723782N	48KB	BFFF
LC723783N	64KB	FFFF
LC723784	96KB	17FFF
LC723785	128KB	1FFFF

3. Executing data writing

PROG

PAE : For program and verify execution.

#### II. Writing board

The writing board is shown in the figure below. The position of pin 1 must be checked before connecting to the EPROM programmer.



Note: The writing adapter has been changed.

To be used for the general-purpose EPROM programmer: Model LC72F3781-ADP-N EPROM programmer

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