TOSHIBA

CMOS 8–Bit Microcontrollers

TMP90PH48F

1. Outline and Characteristics

The TMP90PM48 is a system evalution LSI having a built in One-Time PROM for TMP90C848.
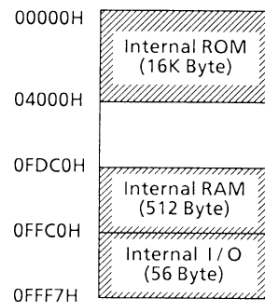
A programming and verification for the internal PROM is achieved by using a general EPROM programmer with an adapter socket.

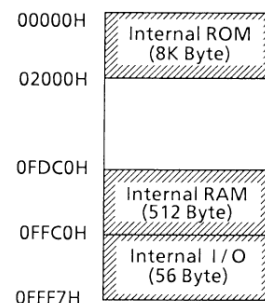The function of this device is exactly same as the TMP90C848 by programming to the internal PROM.

The differences between TMP90PH48 and TMP90C848 are the memory size (ROM).

The following are the memory map of TMP90PH48 and TMP90C848.

TMP90PH48F Memory Map   TMP90C848F Memory Map

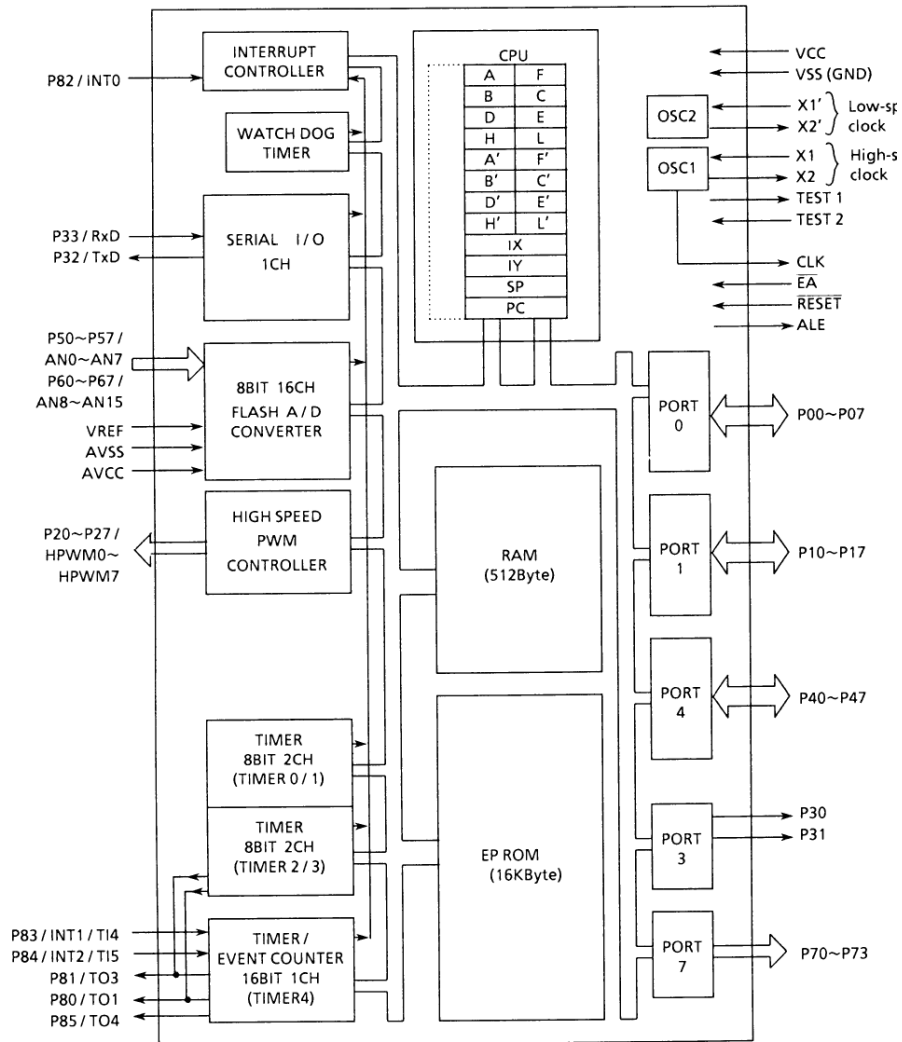| Parts No.	ROM	RAM	Package	Adapter Socket No.
TMP90PH48N	OTP 16384 x 8bit	512 x 8bit	80-FP	BM1153

Figure 1. TMP90PH48F Block Diagram

2. Pin Assignment and Functions

The assignment of input/output pins, their names and functions are described below.

2.1 Pin Assignment
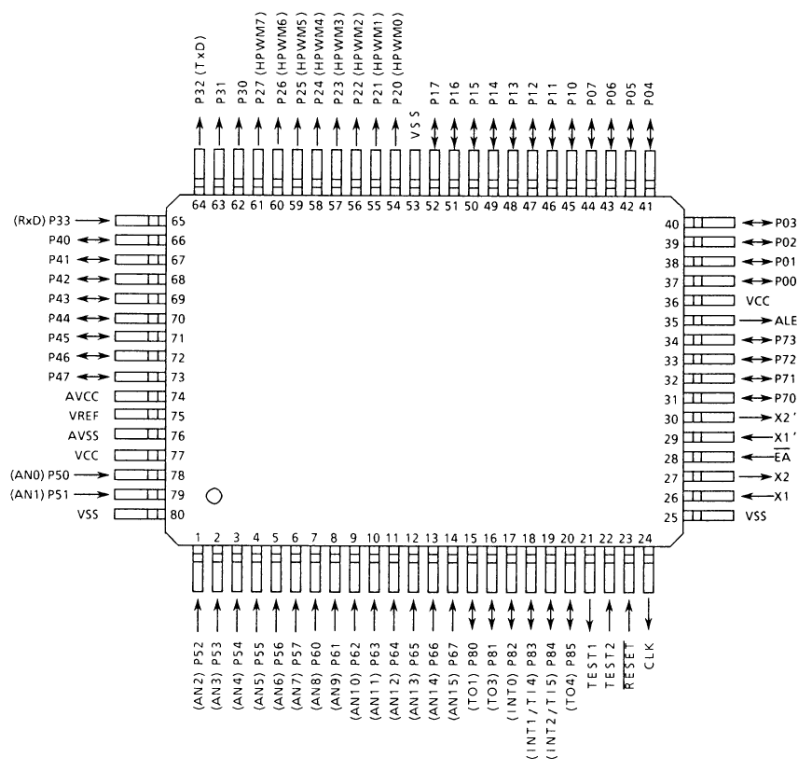
Figure 2.1 shows pin assignment of the TMP90PH48.

Figure 2.1 Pin Assignment (80-FP)

2.2 Pin Names and Functions

The TMP90PH48 has MCU mode and PROM mode.

(1)   MCU mode (The TMP90C848 and TMP90PH48 are pin compatible)

Table 2.2 (1/2)

Pin Name	No. of pins	I/O or tristates	Function
P00 ~ P07	8	I/O	Port 0: 8-bit I/O port. Each bit can be set for input or output.
P10 ~ P17	8	I/O	Port 1: An 8-bit I/O port.Each bit can be set for input or output Pull-up resistance included.
P20 ~ P27	8	I/O	Port 2: 8-bit output port.
P30	1	Output	Port 30: 1-bit output port.
P31	1	Output	Port 31: 1-bit output port.
P32 /TxD	1	Output	Port 32: 1-bit output port.
		Output	Used to transmit serial data.
P32 /RxD	1	Input	Port 33: 1-bit output port.
		Input	Used to receive serial data.
P40 ~ P47	8	I/O	Port 4: 8-bit I/O port. Each bit can be set for input or output (P40 - P43 O.D. 4mA sink, P44 - 47 10mA source).
P50 ~ P57 /AN0 ~ AN7	8	Input	Port 5: 8-bit input port.
		Input	Analog input: 8-bit analog input to the A/D converter.
P60 ~ 67 /AN8 ~ AN15	8	Input	Port 6: 8-bit input port.
		Input	Analog input: 8-bit analog input the A/D converter
P70 ~ P73	4	I/O	Port 7: 4-bit I/O port. Each bit can be set for input or output. Programmable pull-up resistance included.
P80 /T01	1	I/O	Port 80: 1-bit I/O port.
		Output	Timer output 1: Used for timer 0 or timer 1 output.
P81 /T03	1	I/O	Port 81: 1-bit I/O port.
		Output	Timer output 3: Used for timer 2 or timer 3 output.
P82 /INT0	1	I/O	Port 82: 1-bit I/O port.
		Input	Interrupt request pin 0: Level/rising edge programmable interrupt request pin.
P83 /INT1 /TI4	1	I/O	Port 83: 1-bit I/O port.
		Input	Interrupt request pin 1: Rising/falling edge programmable interrupt request pin.
		Input	Timer input 4: Count input/capture trigger signal for timer 4.

Table 2.2 (2/2)

Pin name	No. of pins	I/O or tristate	Function
P84 /INT2 /TI5	1	I/O	Port 84: 1-bit I/O port.
		Input	Interrupt request pin 2: Rising edge programmable interrupt request pin.
		Input	Timer input 5: Count input/capture trigger signal for timer 5.
P85 /TO4	1	I/O	Port 85: 1-bit I/O port.
		Output	Timer output 4: used as the timer 4 output.
ALE	1	Output	Address latch enable signal: The falling edge of this signal used as the timing to latch AD0 ~ AD7 addresses when accessing external memory.
CLK	1	Output	Clock output: Generates clock pulse at 1/4 frequency of clock oscillation. Pulled up during resetting.
$\overline{EA}$	1	Input	External access: Connected to the V_{CC} pin when using the TMP90C848F with built-in ROM.
$\overline{RESET}$	1	Input	Reset: Initializes the TMP90C848F.
X1/X2	2	I/O	High-speed crystal oscillator connection pin.
X1'/X2'	2	I/O	Low-speed crystal oscillator connection pin.
TEST1/TEST2	2	I/O	Testing pins Connects directly TEST1 and TEST2 at a normal state operation.
AVCC	1	–	Comparator power supply for the A/D converter.
VREF	1	–	A/D converter reference voltage input.
AVSS	1	–	Analog GND pin (0V)
V_{CC}	2	–	Power supply (+5V±10%)
V_{SS}	3	–	GND pin

(2)   PROM Mode

Pin Function Name	No. of pins	I/O	Function	Pin Name (MCU mode)
A7 ~ A0	8	Input	Address inputs	P27 ~ P20
A15 ~ A8	8	Input		P15 ~ P10
D7 ~ D0	8	I/O	Data Input/Output	P07 ~ P00
$\overline{OE}$	1	Input	Output Enable Input	P30
$\overline{CE}$	1	Input	Chip Enable Signal Input	P31
VPP	1	Power Supply	12.5V/5V(Programming Power Supply)	$\overline{EA}$
VCC	1	Power Supply	5V	VCC
VSS	1	Power Supply	0V	VSS

Pin Names	No. of pins	I/O	Pin Setting	
P16, P17	2	Output	Be fixed to "L" level (Note).	
P32, P33	2	Output, Input	Be fixed to "H" level.	
P40 ~ P47	8	I/O	Be fixed to "H" level.	
P50 ~ P57 P60 ~ P67	8 8	Input	Be fixed to "L" level.	
P70 ~ P73	4	I/O	Be fixed to "H" level.	
P80 ~ P85	6	I/O	Be fixed to "L" level.	
VREF/ AVss/AVcc	3		Be fixed to "L" level.	
$\overline{RESET}$	1	Input	Refer to Figure 3.2	
CLK	1	Output		
X1	1	Input	Resonator connection pin	
X2	1	Output		
X1'	1	Input		
X2'	1	Output		

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3. Operation

The TMP90PH48 is the OTP version of the TMP90CC848 that is replaced an internal ROM from Mask ROM to EPROM.

    The function of TMP90PH48 is exactly same as that of TMP90CC848 except the internal ROM size.

    Refer to the TMP90C848 except the functions which are not described this section.

    The following is an explanation of the hardware configuration and operation in relation to the TMP90CH48.

    The TMP90PH48 has an MCU mode and a PROM mode.

3.1 MCU Mode

(1)   Mode Setting and Function

    The MCU mode is set by opening the CLK pin (Output status).

    In the MCU mode, the operation is same as that of TMP90C848.

(2)   Memory Map

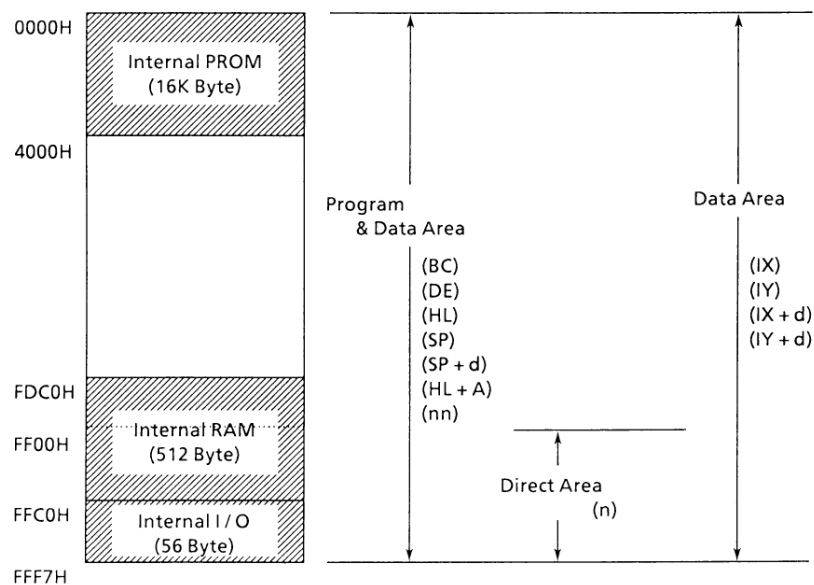   Figure 3.1 shows the memory map TMP90PH48, and the accessing area by the respective addressing mode.

Figure 3.1. TMP90PH48F Memory Map

3.2 PROM Mode

(1) Mode Setting and Function

PROM mode is set by setting the $\overline{\text{RESET}}$ and CLK pins to the "L" level.
The programming and verification for the internal

PROM is achieved by using a general EPROM programmer with the adapter socket. The device slection (ROM type) should be "27256" with following conditions.

Size = 256Kbit (32Kx 8bit) TPW = 1ms, VPP = 12.5V

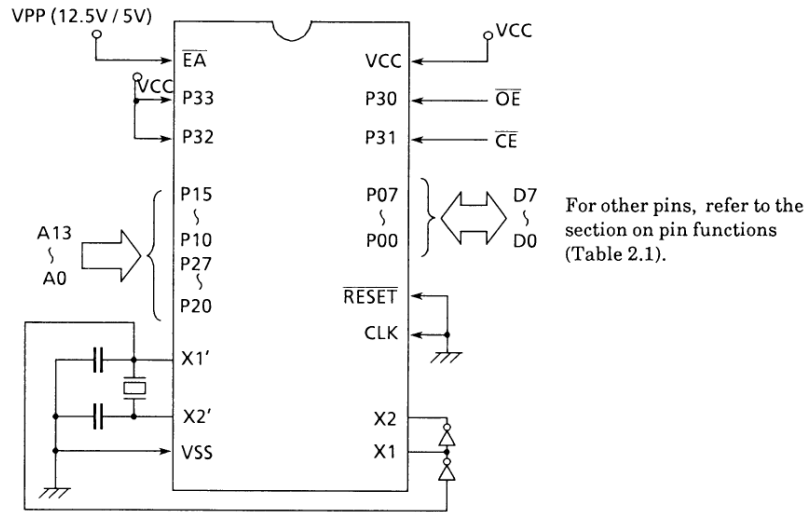Figure 3.2 shows the setting of pins in PROM mode

Figure 3.2. PROM Mode Pin Setting

(2) Programming Flow Chart

The programming mode is set by applying 12.5V (programming voltage) to the VPP pin when the following pins are set as follows,

(Vcc   : 6.0V)   *These conditions can be
($\overline{\text{RESET}}$: "L" level) obtained by using adaptor
(CLK   : "L" level) socket.

After the address and data have been fixed, a data on the Data Bus is programmed when the $\overline{\text{CE}}$ pin is set to "Low" (1ms plus is required).

General programming procedure of an EPROM programmer is as follows,

• Write a data to a specified address for 1ms.
• Verify the data. If the read-out data does not match the expected data, another writing is performed until the correct data is written (Max. 25 times).

After the correct data is written, an additional writing is performed by using three times longer programming pulse width (1ms x programming times), or using three times more programming pulse number. Then, verify the data and increment the address.

The verification for all data is done under the condition of Vpp = Vcc = 5V after all data were written.

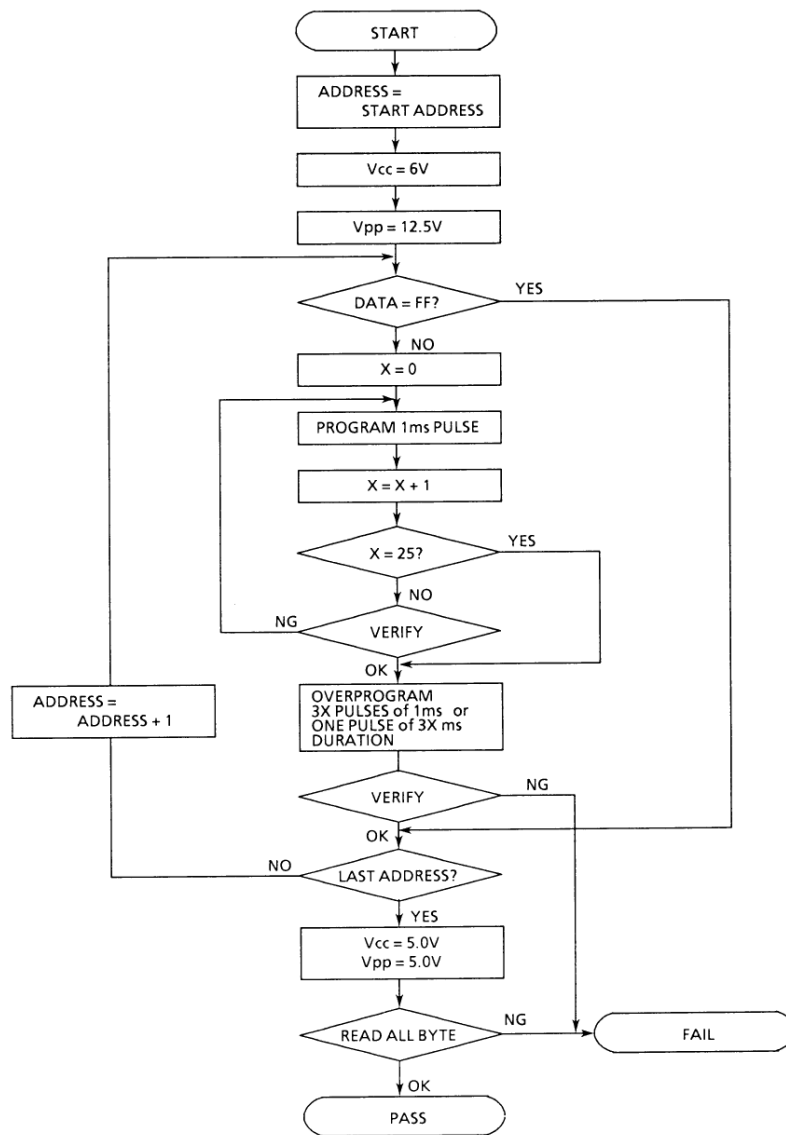Figure 3.3 shows the programming flow chart.

Figure 3.3. Flow Chart

(3)   The Security Bit

The TMP90PH48 has the Security Bit in PROM cell. If the Security Bit is programmed to "0", the content of the PROM is disable to read in PROM mode.

How to program the Security Bit.

1) Connect A15 pins to Vcc. [Otherwise connect them GND to program PROM, (address 0000H ~ 3FFFH)

2) Set programming address to 0000H.

3) To program the Security Bit, Do to "0"

4) Set D2 ~ D7 to "1", respectively.

Table 3.1 Data to Program

Bit to PROGRAM	D0 ~ D7	A0 ~ A12	A15
The Security Bit	FEH	all "0"	all "1"
PROM (0000H ~ 1FFFH)	–	–	all "0"

4. Electrical Characteristics

TMP90PH48

4.1 Absolute Maximum Ratings

Symbol	Item	Rating	Unit
V_{CC}	Power supply voltage	$-0.5 \sim +7$	V
V_{IN}	Input voltage	$-0.5 \sim V_{CC} + 0.5$	V
P_D	Power dissipation (Ta = 70°C)	500	mW
T_{SOLDER}	Soldering temperature (10s)	260	°C
T_{STG}	Storage temperature	$-65 \sim 150$	°C
T_{OPR}	Operating temperature	$-20 \sim 70$	°C

4.2 DC Characteristics

V_{CC} = 5V±10% TA = −20 ~ 70°C
High-speed clock: 16 ~ 20MHz, Low-speed clock: 0.5 ~ 1MHz
Typical values are for TA = 25°C and Vcc = 5V

Symbol	Parameter	Min	Max	Unit	Condition
V_{IL}	Input Low Voltage (P0)	-0.3	0.8	V	–
V_{IL1}	P1, P3, P4, P5, P6, P7, P8	-0.3	$0.3V_{CC}$	V	–
V_{IL2}	$\overline{RESET}$, P82 (INTO)	-0.3	$0.25V_{CC}$	V	–
V_{IL3}	$\overline{EA}$	-0.3	0.3	V	–
V_{IL4}	X1, X1'	-0.3	$0.2V_{CC}$	V	–
V_{IH}	Input High Voltage (P0)	2.2	$V_{CC} + 0.3$	V	–
V_{IH1}	P1, P3, P4, P5, P6, P7, P8	$0.7V_{CC}$	$V_{CC} + 0.3$	V	–
V_{IH2}	$\overline{RESET}$, P82 (INTO)	$0.75V_{CC}$	$V_{CC} + 0.3$	V	–
V_{IH3}	$\overline{EA}$	V_{CC}-0.3	$V_{CC} + 0.3$	V	–
V_{IH4}	X1, X1'	$0.8V_{CC}$	$V_{CC} + 0.3$	V	–
V_{OL} V_{OL1}	Output Low Voltage (OPEN DRAIN Sink)	– –	0.45 0.45	V 0.45	I_{OL} = 1.6mA I_{OL} = 4mA
V_{OH} V_{OH1} V_{OH2} V_{OH3}	Output High Voltage P44 ~ 47 (OPEN DRAIN Source)	2.4 $0.75V_{CC}$ $0.9V_{CC}$ 2.4	– – – –	V V V 0.45	I_{OH} = -400µA I_{OH} = -100µA I_{OH} = -20µA I_{OH} = 10µA
I_{LI}	Input Leakage Current	0.02 (Typ)	±5	µA	0.0≤ Vin ≤V_{CC}
I_{LO}	Output Leakage Current	0.05 (Typ)	±10	µA	0.2≤ Vin ≤V_{CC} - 0.2
I_{CC} (Vcc - Vss)	Operating Current (RUN) Idle 1	15 (Typ) 1.5 (Typ)	30 5	mA mA	High-speed clock: 20MHz Low-speed clock: 1MHz
	STOP (TA = -20 ~ 7°C) STOP (TA = 0 ~ 50°C)	0.2 (Typ)	40 10	µA µA	0.2≤Vin≤V_{CC}-0.2
Alcc AVcc - AVss)	Operating Current	7 (Typ)	15	mA	fosc = 10MHz AVcc = 5V ± 10%
V_{STOP}	Power Down Voltage (@STOP) RAM BACK UP	2.0	6.0	V	V_{IL2} = $0.2V_{CC}$, V_{IH2} = $0.8V_{CC}$
R_{RST}	$\overline{RESET}$, P1, P7, Pull Up Register	30	130	KΩ	–
CIO	Pin Capacitance	–	10	pF	testfreq = 1MHz
V_{TH}	Schmitt width ($\overline{RESET}$, P82)	0.4	1.0 (Typ)	V	–

4.3 A/D Converter Characteristics

<div align="right">
V_{CC} = 5V±10% TA = -20 ~ 70°C
High-speed clock: 16 ~ 20MHz, Low-speed clock: 0.5 ~ 1MHz
</div>

V_{CC} = 5V±10% TA = -20 ~ 70°C
High-speed clock: 16 ~ 20MHz, Low-speed clock: 0.5 ~ 1MHz

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{REF}	Analog reference voltage	–	3.5	Vcc	Vcc	V
ΔV_{REF}	Analog reference voltage range	V_{REF} - Vss	3.5	Vcc	Vcc	
AVss	Analog power supply voltage	–	Vss	Vss	Vss	
V_{AIN}	Analog input voltage range	–	Vss	–	Vcc	
I_{REFAD}	Supply current for analog reference voltage	–	–	0.8	2	mA

This A/D Converter is guaranteed only monotonicity because it has an offset value (when VAIN = 0V), but the 8-bit resolution is gotten except an offset value.

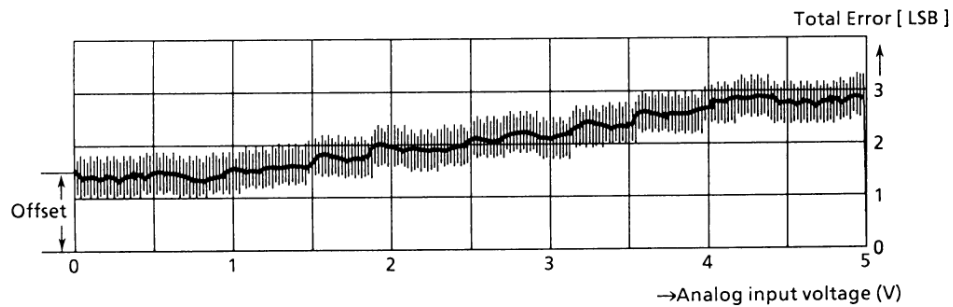The A/D converted data is recommended to be processed relatively.

Figure 4.3 (1). A/D Converter Typical Conversion Characterics (V_{REF} = 5V, Vss = 0V)

4.4 Zero-Cross Characteristics

V_{CC} = 5V±10% TA = -20 ~ 70°C
High-speed clock: 16 ~ 20MHz, Low-speed clock: 0.5 ~ 1MHz

Symbol	Item	Condition	Min	Max	Unit
V_{ZX}	Zero-cross detection input	For AC, C = 0.1µF	1	1.8	VAC $_{P-P}$
A_{ZX}	Zero-cross accuracy	50/60Hz sine wave	–	135	mV
F_{ZX}	Zero-cross detection input frequency	–	0.04	1	kHz

### 4.5 Timer/Counter Input Clock (TI0, TI2, and TI4)

V_{CC} = 5V±10%TA = -20 ~ 70°C
High-speed clock: 16 ~ 20MHz, Low-speed clock: 0.5 ~ 1MHz

Symbol	Parameter	Variable		10MHz Clock		Unit
		Min	Max	Min	Max	
t_{VCK}	Clock cycle	8x + 100	–	900	–	ns
t_{VCKL}	Low clock pulse width	4x + 40	–	440	–	ns
t_{VCKH}	High clock pulse width	4x + 40	–	440	–	ns

4.6 Interrupt Operation

Symbol	Item	Variable		10MHz Clock		Unit
		Min	Max	Min	Max	
t$_{INTAL}$	$\overline{NMI}$, INT0 Low level pulse width ⌐⌐_⌐	4x	–	400	–	ns
t$_{INTAH}$	$\overline{NMI}$, INT0 High level pulse width _⌐⌐_	4x	–	400	–	ns
t$_{INTBL}$	INT1, INT2 Low level pulse width ⌐⌐_⌐	8x + 100	–	900	–	ns
t$_{INTBH}$	INT1, INT2 High level pulse width _⌐⌐_	8x + 100	–	900	–	ns

4.7 Read Operation (PROM Mode)

DC Characteristic, AC Characteristic

TA = -40 ~ 85°C Vcc = 5V$\pm$10%

| Symbol	Parameter	Condition	Min	Max	Unit
V$_{PP}$	V$_{PP}$ read voltage	–	4.5	5.5	V
V$_{IH1}$	Input high voltage (A0 ~ A15, $\overline{CE}$, $\overline{OE}$)	–	0.7 x V$_{CC}$	Vcc + 0.3	V
V$_{IL1}$	Input low voltage (A ~ A15, $\overline{CE}$, $\overline{OE}$)	–	-0.3	0.3 x V$_{CC}$	V
t$_{ACC}$	Address to output delay	C$_L$ = 50$_P$F	–	2.25TCYC + α	ns

TCYC = 400ns (10MHz Clock)
α = 200ns

4.8 Programming Operation (PROM Mode)

DC Characteristic, AC Characteristic

TA = 25$\pm$5°C Vcc = 6V$\pm$0.25V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V$_{PP}$	Programming voltage	-	12.25	12.50	12.75	V
V$_{IH}$	Input high voltage (D0 ~ D7)	-	0.2V$_{CC}$ + 1.1		V$_{CC}$ + 0.3	V
V$_{IL}$	Input low voltage (D0 ~ D7)	-	-0.3		0.2V$_{CC}$ - 0.1	V
V$_{IH1}$	Input high voltage (A0 ~ A15, $\overline{CE}$, $\overline{OE}$)	-	0.7V$_{CC}$		V$_{CC}$ + 0.3	V
V$_{IL1}$	Input low voltage (A0 ~ A15, $\overline{CE}$, $\overline{OE}$)	-	-0.3		0.3V$_{CC}$	V
I$_{CC}$	V$_{CC}$ supply current	t$_{OSC}$ = 10MHz	-		50	mA
I$_{PP}$	V$_{PP}$ supply current	V$_{PP}$ = 13.00V	-		50	mA
t$_{PW}$	$\overline{CE}$ Program pulse width	C$_L$ = 50$_P$F	0.95	1.00	1.05	ms

4.9 Read Operation Timing Chart (PROM Mode)
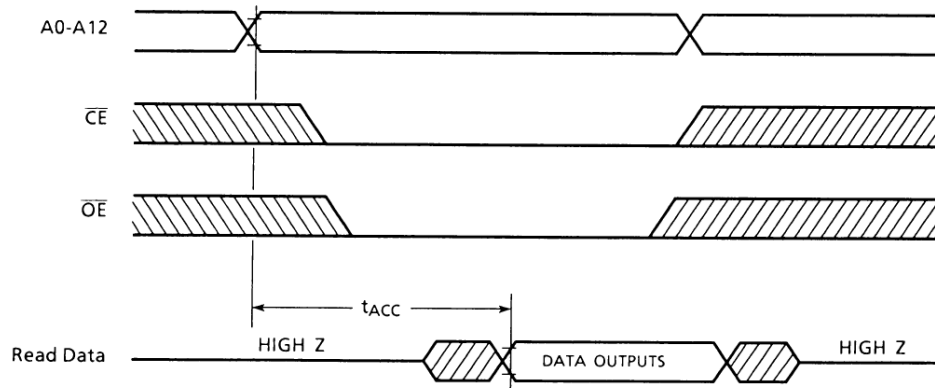
4.10 Programming Operation Timing Chart (PROM Mode)