

## Features

- High speed
  - $t_{AA} = 10 \text{ ns}$
- Low active power
  - 990 mW (max)
- Operating voltages of  $3.3 \pm 0.3 \text{ V}$
- 2.0 V data retention
- Automatic power down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with  $\overline{CE}_1$  and  $CE_2$  features
- Available in Pb-free 54-pin thin small outline package (TSOP II) package

## Functional Description

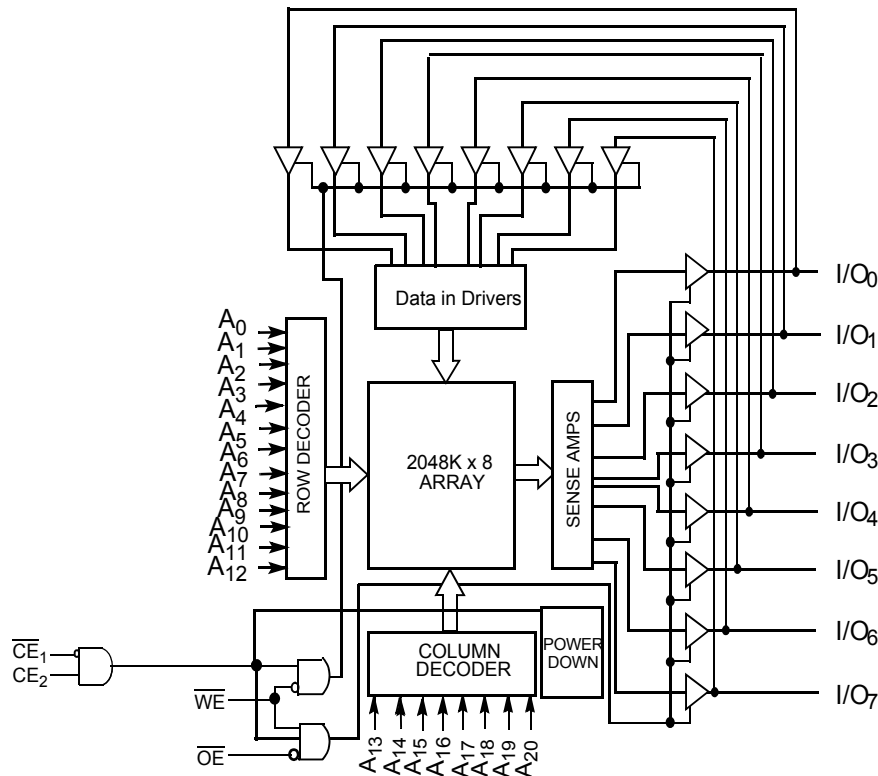
The CY7C1069AV33 is a high performance complementary metal oxide semiconductor (CMOS) static RAM organized as 2,097,152 words by 8 bits. Writing to the device is accomplished by enabling the chip (by taking  $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and Write Enable ( $\overline{WE}$ ) inputs LOW.

Reading from the device is accomplished by enabling the chip ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) as well as forcing the Output Enable ( $\overline{OE}$ ) LOW while forcing the  $\overline{WE}$  HIGH. See "Truth Table" on page 8 for a complete description of Read and Write modes.

The input/output pins ( $I/O_0$  through  $I/O_7$ ) are placed in a high impedance state when the device is deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW), the outputs are disabled ( $\overline{OE}$  HIGH), or during a Write operation ( $\overline{CE}_1$  LOW,  $CE_2$  HIGH, and  $\overline{WE}$  LOW).

The CY7C1069AV33 is available in a 54-pin TSOP II package with center power and ground (revolutionary) pinout.

## Logic Block Diagram



## Contents

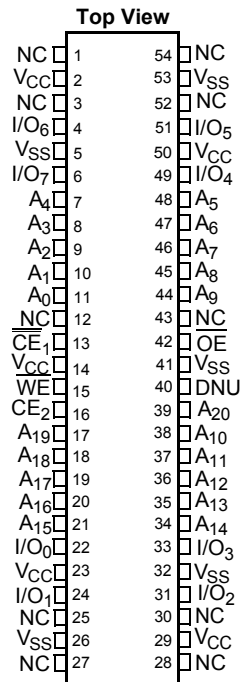
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**Selection Guide**

Description	-10	Unit
Maximum access time	10	ns
Maximum operating current	275	mA
Maximum CMOS standby current	50	mA

**Pin Configuration**

Figure 1. 54-pin TSOP II [1, 2]



**Notes**

1. NC pins are not connected on the die.
2. DNU pins have to be left floating or tied to V<sub>SS</sub> to ensure proper application.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C

Ambient temperature with power applied ..... -55 °C to +125 °C

Supply voltage on  $V_{CC}$  to relative GND<sup>[3]</sup> ..... -0.5 V to +4.6 V

DC voltage applied to outputs in high Z state<sup>[3]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V

DC input voltage<sup>[3]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V

Current into outputs (LOW) ..... 20 mA

## Operating Range

Range	Ambient Temperature	$V_{CC}$
Commercial	0 °C to +70 °C	3.3 V ± 0.3 V
Industrial	-40 °C to +85 °C	

## DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-10		Unit
			Min	Max	
$V_{OH}$	Output HIGH voltage	$V_{CC} = \text{Min}, I_{OH} = -4.0 \text{ mA}$	2.4	-	V
$V_{OL}$	Output LOW voltage	$V_{CC} = \text{Min}, I_{OL} = 8.0 \text{ mA}$	-	0.4	V
$V_{IH}$	Input HIGH voltage		2.0	$V_{CC} + 0.3$	V
$V_{IL}$	Input LOW voltage <sup>[3]</sup>		-0.3	0.8	V
$I_{IX}$	Input leakage current	$GND \leq V_I \leq V_{CC}$	-1	+1	μA
$I_{OZ}$	Output leakage current	$GND \leq V_{OUT} \leq V_{CC}$ , Output Disabled	-1	+1	μA
$I_{CC}$	$V_{CC}$ Operating supply current	$V_{CC} = \text{Max}, f = f_{MAX} = 1/t_{RC}$	-	275	mA
$I_{SB1}$	Automatic CE power down current —TTL Inputs	$\overline{CE}_2 \leq V_{IL}$ , Max $V_{CC}$ , $\overline{CE}_1 \geq V_{IH}$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = f_{MAX}$	-	70	mA
$I_{SB2}$	Automatic CE power down current —CMOS inputs	$\overline{CE}_2 \leq 0.3 \text{ V}$ , Max $V_{CC}$ , $\overline{CE}_1 \geq V_{CC} - 0.3 \text{ V}$ , $V_{IN} \geq V_{CC} - 0.3 \text{ V}$ , or $V_{IN} \leq 0.3 \text{ V}$ , $f = 0$	-	50	mA

## Capacitance

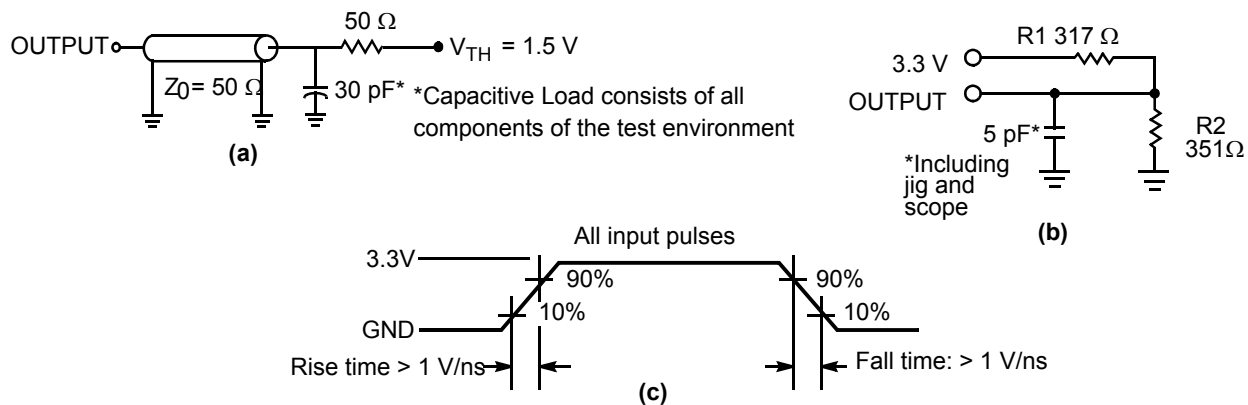
Tested initially and after any design or process changes that may affect these parameters.<sup>[4]</sup>

Parameter	Description	Test Conditions	TSOP II	Unit
$C_{IN}$	Input capacitance	$T_A = 25 \text{ °C}, f = 1 \text{ MHz}, V_{CC} = 3.3 \text{ V}$	6	pF
$C_{OUT}$	I/O capacitance		8	pF

### Notes

3.  $V_{IL}$  (min.) = -2.0 V for pulse durations of less than 20 ns.

4. Tested initially and after any design or process changes that may affect these parameters.

**Figure 2. AC Test Loads and Waveforms<sup>[5]</sup>**


## AC Switching Characteristics

Over the Operating Range <sup>[6]</sup>

Parameter	Description	-10		Unit
		Min	Max	
<b>Read Cycle</b>				
$t_{\text{power}}$	$V_{CC}$ (typical) to the first access <sup>[7]</sup>	1	–	ms
$t_{RC}$	Read cycle time	10	–	ns
$t_{AA}$	Address to data valid	–	10	ns
$t_{OHA}$	Data hold from address change	3	–	ns
$t_{ACE}$	$\overline{CE}_1$ LOW/ $CE_2$ HIGH to data valid	–	10	ns
$t_{DOE}$	OE LOW to data valid	–	5	ns
$t_{LZOE}$	$\overline{OE}$ LOW to low $Z$ <sup>[8]</sup>	1	–	ns
$t_{HZOE}$	$\overline{OE}$ HIGH to high $Z$ <sup>[8]</sup>	–	5	ns
$t_{LZCE}$	$\overline{CE}_1$ LOW/ $CE_2$ HIGH to low $Z$ <sup>[8]</sup>	3	–	ns
$t_{HZCE}$	$\overline{CE}_1$ HIGH/ $CE_2$ LOW to high $Z$ <sup>[8]</sup>	–	5	ns
$t_{PU}$	$\overline{CE}_1$ LOW/ $CE_2$ HIGH to power up <sup>[9]</sup>	0	–	ns
$t_{PD}$	$\overline{CE}_1$ HIGH/ $CE_2$ LOW to power down <sup>[9]</sup>	–	10	ns
<b>Write Cycle<sup>[9, 10]</sup></b>				
$t_{WC}$	Write cycle time	10	–	ns
$t_{SCE}$	$\overline{CE}_1$ LOW/ $CE_2$ HIGH to write end	7	–	ns
$t_{AW}$	Address setup to write end	7	–	ns
$t_{HA}$	Address hold from write end	0	–	ns
$t_{SA}$	Address setup to write start	0	–	ns

### Notes

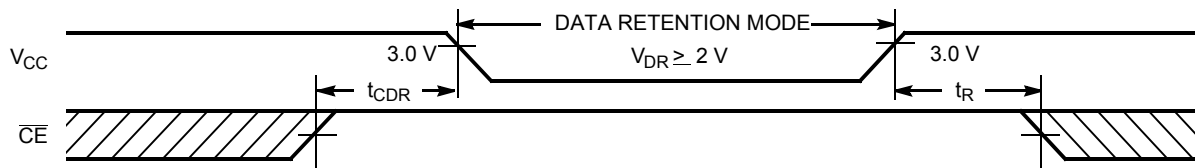
- Valid SRAM operation does not occur until the power supplies have reached the minimum operating  $V_{DD}$  (3.0V). As soon as 1ms ( $T_{\text{power}}$ ) after reaching the minimum operating  $V_{DD}$ , normal SRAM operation can begin including reduction in  $V_{DD}$  to the data retention ( $V_{CCDR}$ , 2.0V) voltage.
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and transmission line loads. Test conditions for the Read cycle use output loading shown in part a) of the AC test loads, unless specified otherwise.
- This part has a voltage regulator which steps down the voltage from 3V to 2V internally.  $t_{\text{power}}$  time has to be provided initially before a Read/Write operation is started.
- $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZWE}$  and  $t_{LZOE}$ ,  $t_{LZCE}$ , and  $t_{LZWE}$  are specified with a load capacitance of 5 pF as in (b) of AC Test Loads. Transition is measured  $\pm 200\ \text{mV}$  from steady-state voltage.
- These parameters are guaranteed by design and are not tested.
- The internal Write time of the memory is defined by the overlap of  $\overline{CE}_1$  LOW/ $CE_2$  HIGH, and  $\overline{WE}$  LOW.  $\overline{CE}_1$  and  $\overline{WE}$  must be LOW along with  $CE_2$  HIGH to initiate a Write, and the transition of any of these signals can terminate the Write. The input data setup and hold timing should be referenced to the leading edge of the signal that terminates the Write.

### AC Switching Characteristics

Over the Operating Range (continued)<sup>[6]</sup>

Parameter	Description	-10		Unit
		Min	Max	
t <sub>PWE</sub>	WE pulse width	7	–	ns
t <sub>SD</sub>	Data setup to write end	5.5	–	ns
t <sub>HD</sub>	Data hold from write end	0	–	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to low Z <sup>[8]</sup>	3	–	ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to high Z <sup>[8]</sup>	–	5	ns

Figure 3. Data Retention Waveform



Switching Waveforms

Figure 4. Read Cycle No. 1<sup>[11, 12]</sup>

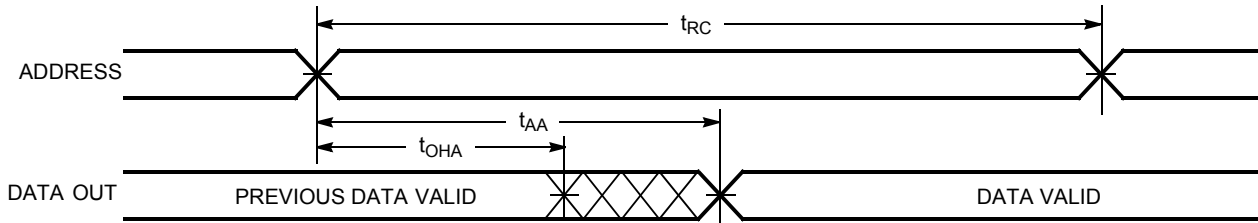
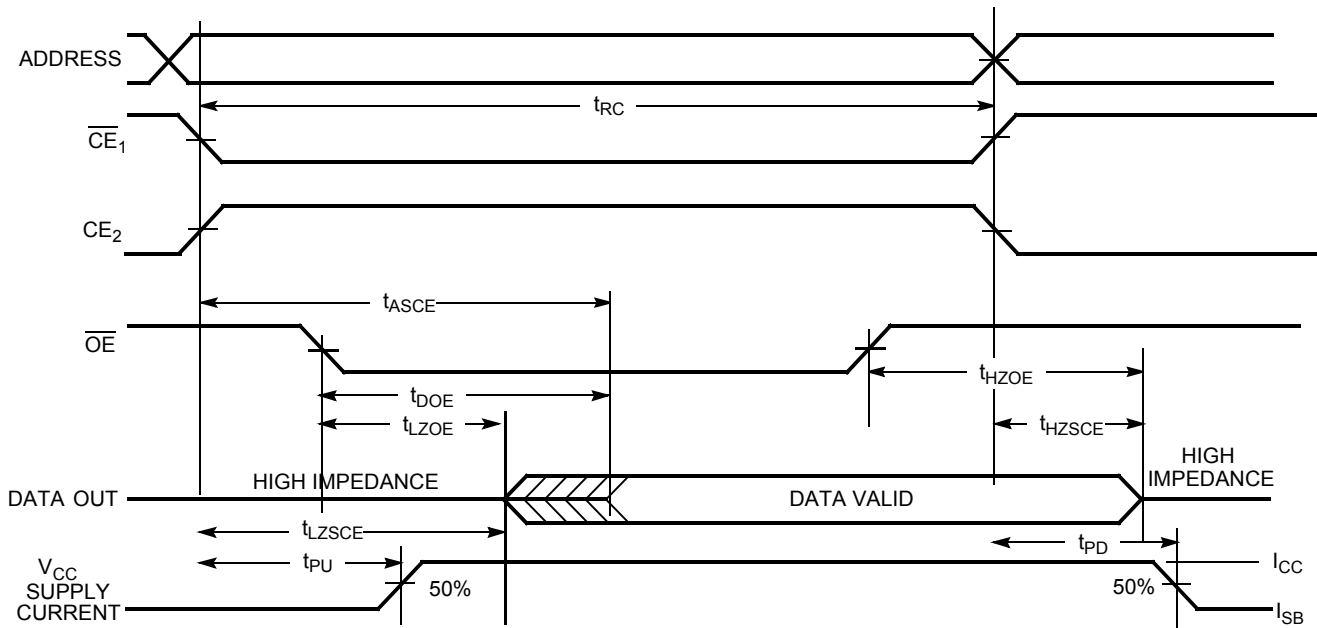


Figure 5. Read Cycle No. 2 ( $\overline{OE}$  Controlled)<sup>[12, 13]</sup>



Notes

- 11. Device is continuously selected.  $\overline{CE}_1 = V_{IL}$ ,  $CE_2 = V_{IH}$ .
- 12.  $\overline{WE}$  is HIGH for Read cycle.
- 13. Address valid prior to or coincident with  $\overline{CE}_1$  transition LOW and  $CE_2$  transition HIGH.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 1 ( $\overline{CE}_1$  Controlled)<sup>[14, 15, 16]</sup>

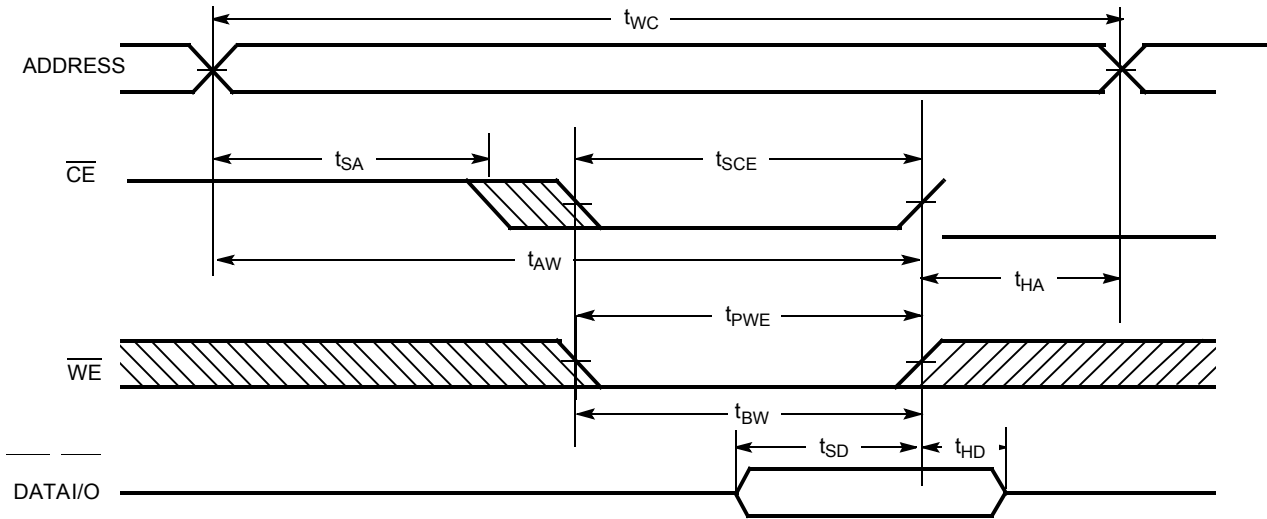
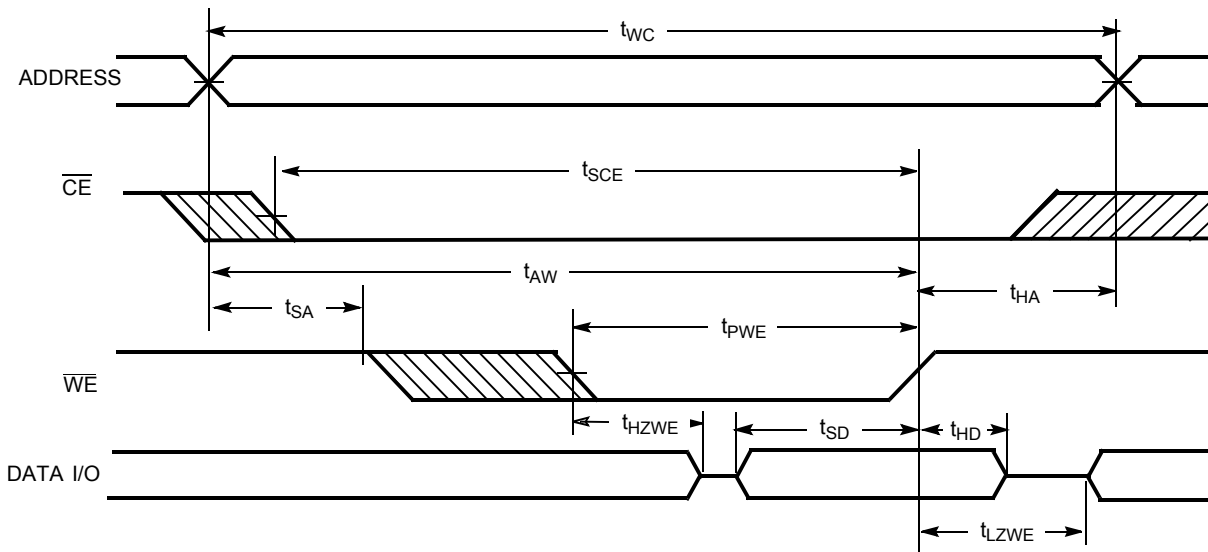


Figure 7. Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[14, 15, 16]</sup>



Truth Table

$\overline{CE}_1$	$\overline{CE}_2$	$\overline{OE}$	$\overline{WE}$	I/O <sub>0</sub> -I/O <sub>7</sub>	Mode	Power
H	X	X	X	High Z	Power down	Standby ( $I_{SB}$ )
X	L	X	X	High Z	Power down	Standby ( $I_{SB}$ )
L	H	L	H	Data Out	Read all bits	Active ( $I_{CC}$ )
L	H	X	L	Data In	Write all bits	Active ( $I_{CC}$ )
L	H	H	H	High Z	Selected, outputs disabled	Active ( $I_{CC}$ )

Notes

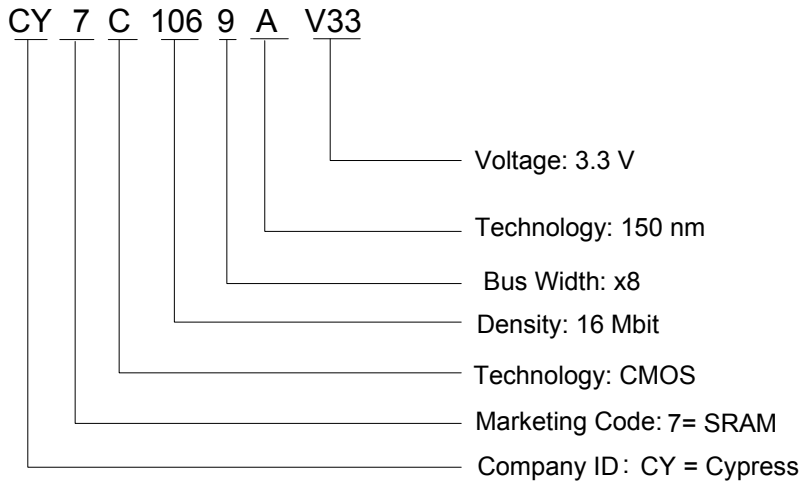
- 14. Data I/O is high-impedance if  $\overline{OE} = V_{IH}$ .
- 15. If  $\overline{CE}_1$  goes HIGH/ $\overline{CE}_2$  LOW simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.
- 16. CE above is defined as a combination of  $\overline{CE}_1$  and  $\overline{CE}_2$ . It is active low.



### Ordering Information

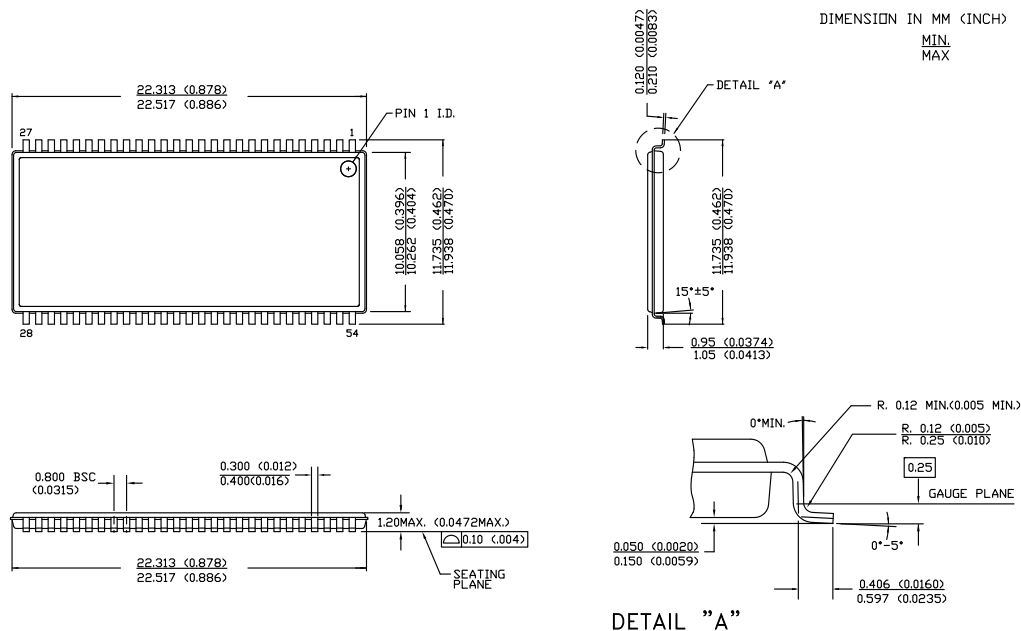
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1069AV33-10ZXC	51-85160	54-pin TSOP II (Pb-free)	Commercial

### Ordering Code Definition



### Package Diagram

Figure 8. 54-pin TSOP II, 51-85160



51-85160 \*A

## Acronyms

Acronym	Description
$\overline{BE}$	Byte Enable
CMOS	complementary metal oxide semiconductor
I/O	Input/output
$\overline{OE}$	Output Enable
SRAM	static random access memory
TSOP	thin small outline package
TTL	transistor-transistor logic
$\overline{WE}$	Write Enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
ns	nano seconds
V	Volts
$\mu A$	micro Amperes
mA	milli Amperes
mV	milli Volts
mW	milli Watts
ms	milli seconds
pF	pico Farad
$^{\circ}C$	degree Celcius
W	Watts
%	percent

**Document History Page**

Document Title: CY7C1069AV33 2 M × 8 Static RAM				
Document Number: 38-05255				
REV.	ECN NO.	Submission Date	Orig. of Change	Description of Change
**	113724	03/27/02	NSL	New Data Sheet
*A	117060	07/31/02	DFP	Removed 15-ns bin
*B	117990	08/30/02	DFP	Added 8-ns bin Changing I <sub>CC</sub> for 8, 10, 12 bins t <sub>power</sub> changed from 1 μs to 1 ms Load Cap Comment changed (for Tx line load) t <sub>SD</sub> changed to 5.5 ns for the 10-ns bin Changed some 8-ns bin #'s (t <sub>HZ</sub> , t <sub>DOE</sub> , t <sub>DBE</sub> ) Removed hz < I <sub>Z</sub> comments
*C	120385	11/13/02	DFP	Final Data Sheet Added note 4 to "AC Test Loads and Waveforms" and note 7 to t <sub>pu</sub> and t <sub>pd</sub> Updated Input/Output Caps (for 48BGA only) to 8 pf/10 pf and for the 54-pin TSOP to 6/8 pf
*D	124441	2/25/03	MEG	Changed ISB1 from 100 mA to 70 mA Shaded the 48fBGA product offering information
*E	403984	See ECN	NXR	Changed the Logic Block Diagram On page # 1 Added notes under Pin Configuration Changed the Package diagram of 51-85162 from Rev *A to Rev *D Changed 48-Ball FBGA to 60-Ball FBGA in Pin Configuration Updated the Ordering Information
*F	492137	See ECN	NXR	Removed 8 ns speed bin from product offering Changed the description of I <sub>Ix</sub> from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Updated the Ordering Information
*G	2784946	10/12/2009	VKN/PYRS	Updated template Corrected typo in footnote 9 Updated Ordering Information table
*H	2897049	03/25/10	AJU	Removed inactive parts from the ordering information table. Updated package diagrams.
*I	2950666	06/11/2010	VKN	Removed 12ns speed bin, Removed 60 Ball FBGA package Updated <a href="#">Ordering Information</a> Added <a href="#">Acronyms</a> and <a href="#">Ordering Code Definition</a> .
*J	3096933	11/29/2010	PRAS	Added <a href="#">Units of Measure</a> . Minor edits and updated in new template.

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