FAIRCHILD SEMICONDUCTOR®

May 2012

FSL136MRT
Green-Mode Fairchild Power Switch (FPS™)

Features

- Internal Avalanched-Rugged 650V SenseFET
- Advanced Soft Burst-Mode Operation for Low Standby Power and Low Audible Noise
- Random Frequency Fluctuation for Low EMI
- Pulse-by-Pulse Current Limit
- Various Protection Functions: Overload Protection (OLP), Over-Voltage Protection (OVP), Abnormal Over-Current Protection (AOCP), Internal Thermal Shutdown (TSD) with Hysteresis, and Under-Voltage Lockout (UVLO) with Hysteresis
- Low Operating Current (0.4mA) in Burst Mode
- Internal Startup Circuit
- Built-in Soft-Start: 15ms
- Auto-Restart Mode

Applications

- Power Supply for STB Home Appliances and DVD Combination

Description

The FSL136MRT is an integrated Pulse Width Modulation (PWM) controller and SenseFET specifically designed for offline Switch-Mode Power Supplies (SMPS) with minimal external components. The PWM controller includes an integrated fixed-frequency oscillator, Under-Voltage Lockout (UVLO), Leading-Edge Blanking (LEB), optimized gate driver, internal soft-start, temperature-compensated precise current sources for loop compensation, and self-protection circuitry. Compared with a discrete MOSFET and PWM controller solution, the FSL136MRT can reduce total cost, component count, size, and weight; while simultaneously increasing efficiency, productivity, and system reliability. This device provides a basic platform suited for cost-effective design of a flyback converter.

Ordering Information

Part Number	Package	Operating Junction Temperature	Current Limit	$R_{DS(ON)}$ (Max.)	Output Power Table(2)				Replaces Device
					$230V_{AC} \pm 15\%$(3)		$85\sim265V_{AC}$		
					Adapter(4)	Open Frame(5)	Adapter(4)	Open Frame(5)	
FSL136MRT	TO-220F 6-Lead(1) W-Forming	−40°C ~ +125°C	2.15A	4Ω	35W	50W	24W	35W	KA5M0365RY DTU

Notes:
1. Pb-free package per JEDEC J-STD-020B.
2. The junction temperature can limit the maximum output power.
3. $230V_{AC}$ or $100/115V_{AC}$ with voltage doubler.
4. Typical continuous power in a non-ventilated enclosed adapter measured at 50°C ambient temperature.
5. Maximum practical continuous power in an open-frame design at 50°C ambient temperature.

Application Circuit

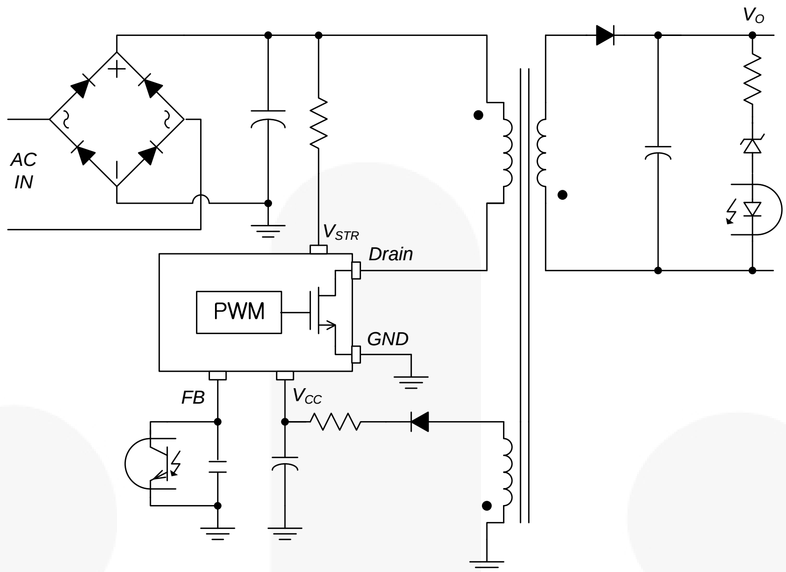

Figure 1. Typical Application Circuit

Internal Block Diagram

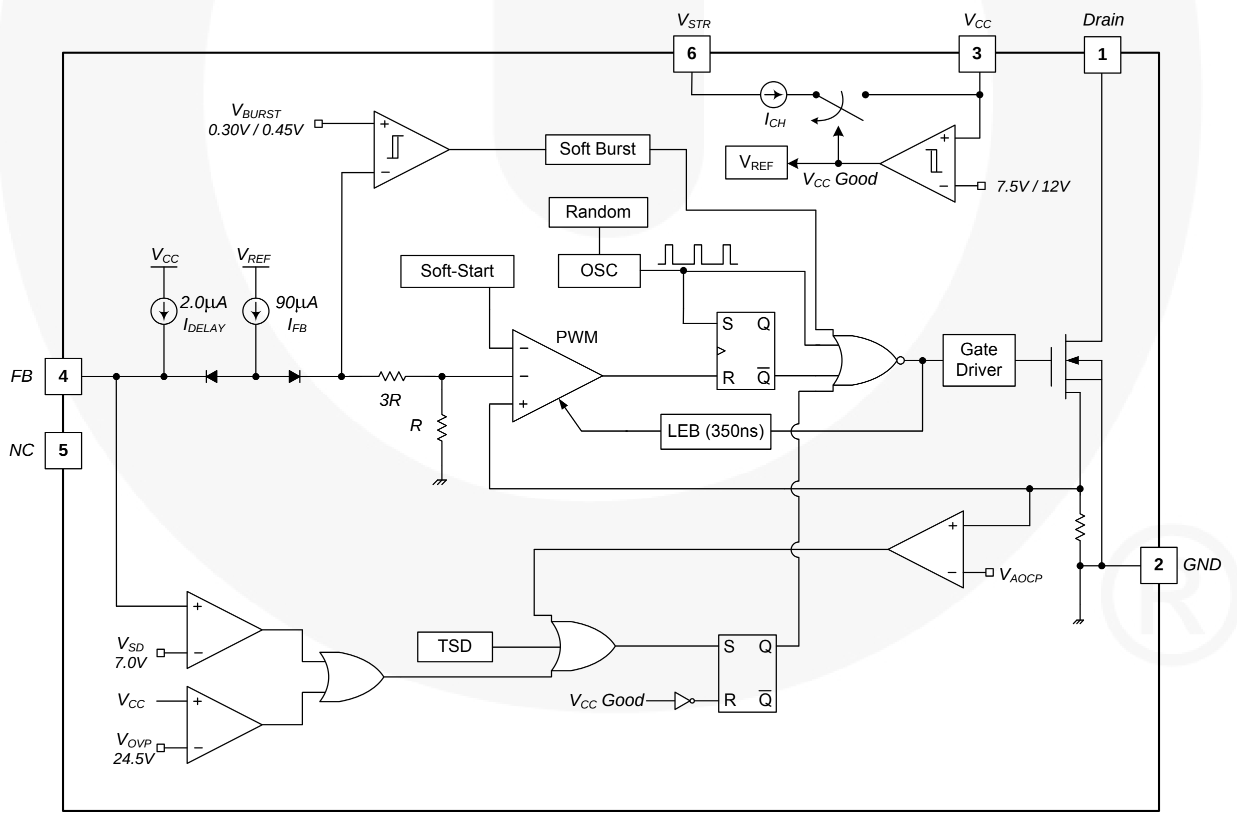

Figure 2. Internal Block Diagram

Pin Configuration

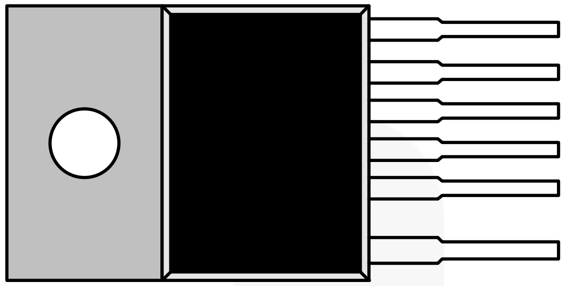

Figure 3. Pin Configuration (Top View)

Pin Definitions

Pin #	Name	Description
1	Drain	**SenseFET Drain**. High-voltage power SenseFET drain connection.
2	GND	**Ground**. This pin is the control ground and the SenseFET source.
3	V_{CC}	**Power Supply**. This pin is the positive supply input, which provides the internal operating current for both startup and steady-state operation.
4	FB	**Feedback**. This pin is internally connected to the inverting input of the PWM comparator. The collector of an opto-coupler is typically tied to this pin. For stable operation, a capacitor should be placed between this pin and GND. If the voltage of this pin reaches 7V, the overload protection triggers, which shuts down the FPS.
5	NC	No Connection
6	V_{STR}	**Startup**. This pin is connected directly, or through a resistor, to the high-voltage DC link. At startup, the internal high-voltage current source supplies internal bias and charges the external capacitor connected to the V_{CC} pin. Once V_{CC} reaches 12V, the internal current source (I_{CH}) is disabled.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{STR}	V_{STR} Pin Voltage		650	V
V_{DS}	Drain Pin Voltage		650	V
V_{CC}	V_{CC} Pin Voltage		26	V
V_{FB}	Feedback Pin Voltage	−0.3	10.0	V
I_{DM}	Drain Current Pulsed(6)		12	A
I_{DS}	Continuous Switching Drain Current		3	A
E_{AS}	Single Pulsed Avalanche Energy(7)		230	mJ
P_D	Total Power Dissipation (T_C=25°C)(8)		50	W
T_J	Maximum Junction Temperature		150	°C
	Operating Junction Temperature(9)	−40	+125	°C
T_{STG}	Storage Temperature	−55	+150	°C

Notes:
6. Repetitive peak switching current when the inductive load is assumed: Limited by maximum duty (D_{MAX}=0.74) and junction temperature *(see Figure 4)*.
7. L=45mH, starting T_J=25°C.
8. Infinite cooling condition *(refer to the SEMI G30-88)*.
9. Although this parameter guarantees IC operation, it does not guarantee all electrical characteristics.

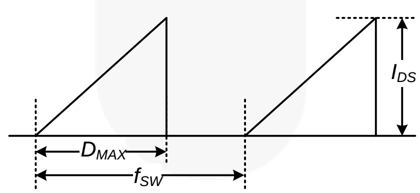

Figure 4. Repetitive Peak Switching Current

ESD Capability

Symbol	Parameter	Value	Unit
ESD	Human Body Model, JESD22-A114	5	KV
	Charged Device Model, JESD22-C101	2	

Thermal Impedance

T_A=25°C unless otherwise specified.

Symbol	Parameter	Value	Unit
θ_{JA}	Junction-to-Ambient Thermal Impedance(10)	63.5	°C/W
θ_{JC}	Junction-to-Case Thermal Impedance(11)	2.8	°C/W

Notes:
10. Free standing without heat sink under natural convection condition, per JEDEC 51-2 and 1-10.
11. Infinite cooling condition per Mil Std. 883C method 1012.1.

Electrical Characteristics

T_J = 25°C unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
SenseFET Section						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{CC}=0V, I_D=250µA	650			V
I_{DSS}	Zero-Gate-Voltage Drain Current	V_{DS}=520V, T_A=125°C			250	µA
$R_{DS(ON)}$	Drain-Source On-State Resistance	V_{GS}=10V, I_D =1A		3.5	4.0	Ω
C_{ISS}	Input Capacitance(12)	V_DS=25V, V_{GS}=0V, f=1MHz		290		pF
C_{OSS}	Output Capacitance(12)	V_{DS}=25V, V_{GS}=0V, f=1MHz		45		pF
C_{RSS}	Reverse Transfer Capacitance(12)	V_{DS}=25V, V_{GS}=0V, f=1MHz		5.5		pF
t_r	Rise Time	V_{DS}=325V, I_D=3.5A		22		ns
t_f	Fall Time	V_{DS}=325V, I_D=3.5A		19		ns
$t_{d(on)}$	Turn-On Delay	V_{DS}=325V, I_D=3.5A		12		ns
$t_{d(off)}$	Turn-Off Delay	V_{DS}=325V, I_D= 3.5A		20		ns
Control Section						
f_S	Switching Frequency(12)	V_{CC}=14V, V_{FB}=4V	61	67	73	kHz
Δf_S	Switching Frequency Variation(12)	−25°C < T_J < 125°C		±5	±10	%
D_{MAX}	Maximum Duty Ratio	V_{CC}=14V, V_{FB}=4V	61	67	73	%
D_{MIN}	Minimum Duty Ratio	V_{CC}=14V, V_{FB}=0V			0	%
I_{FB}	Feedback Source Current	V_{FB}=0	65	90	115	µA
V_{START}	UVLO Threshold Voltage	V_{FB}=0V, V_{CC} Sweep	11	12	13	V
V_{STOP}		After Turn-on, V_{FB}=0V	7.0	7.5	8.0	V
$t_{S/S}$	Internal Soft-Start Time	V_{CC} Sweep		15		ms
Burst-Mode Section						
V_{BURH}	Burst-Mode Voltage	V_{CC}=14V, V_{FB} Sweep	0.39	0.45	0.51	V
V_{BURL}			0.26	0.30	0.34	V
Hys				150		mV
Protection Section						
I_{LIM}	Peak Drain Current Limit	di/dt=300mA/µs	1.89	2.15	2.41	A
V_{SD}	Shutdown Feedback Voltage	V_{CC}=14V, V_{FB} Sweep	6.45	7.00	7.55	V
I_{DELAY}	Shutdown Delay Current	V_{CC}=14V, V_{FB}=4V	1.2	2.0	2.8	µA
t_{LEB}	Leading-Edge Blanking Time(12,14)			350		ns
V_{OVP}	Over-Voltage Protection	V_{CC} Sweep	23.0	24.5	26.0	V
T_{SD}	Thermal Shutdown Temperature(12)	Shutdown Temperature	130	140	150	°C
Hys		Hysteresis		60		°C

Continued on the following page…

Electrical Characteristics (Continued)

T_J=25°C unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Total Device Section						
I_{OP}	Operating Supply Current, (Control Part in Burst Mode)	V_{CC}=14V, V_{FB}=0V	0.3	0.4	0.5	mA
I_{OPS}	Operating Switching Current, (Control Part and SenseFET Part)	V_{CC}=14V, V_{FB}=2V		1.00	1.35	mA
I_{START}	Start Current	V_{CC}=11V (Before V_{CC} Reaches V_{START})	85	120	155	µA
I_{CH}	Startup Charging Current	V_{CC}=V_{FB}=0V, V_{STR}=40V	0.7	1.0	1.3	mA
V_{STR}	Minimum VSTR Supply Voltage	V_{CC}=V_{FB}=0V, V_{STR} Sweep		26		V

Notes:

12. Although these parameters are guaranteed, they are not 100% tested in production.
13. Average value.
14. t_{LEB} includes gate turn-on time.

Comparison of KA5M0365R and FSL136MRT

Function	KA5M0365RYDTU	FSL136MRT	Advantages of FSL136MRT
Random Frequency Fluctuation	N/A	Built−in	Low EMI
Operating Current	7mA	0.4mA	Very low stand-by power
High-Voltage Startup Circuit	N/A	Built−in	
Protections	OLP OVP TSD	OLP OVP AOCP TSD with Hysteresis	Enhanced protections and high reliability
Power Balance	Long t_{CLD}	Very Short t_{CLD}	The difference of input power between the low and high input voltage is quite small

Typical Performance Characteristics

Characteristic graphs are normalized at T_A=25°C.

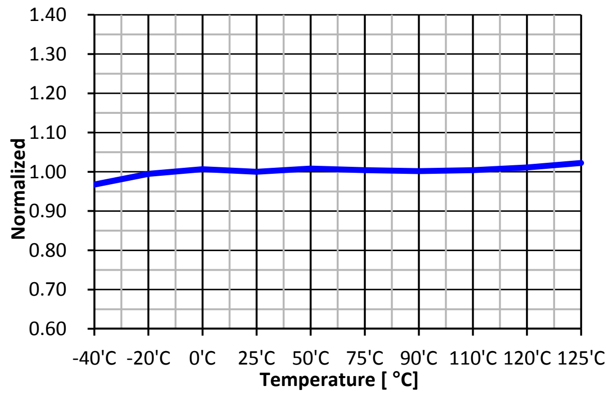

Figure 5. Operating Supply Current (I_{OP}) vs. T_A

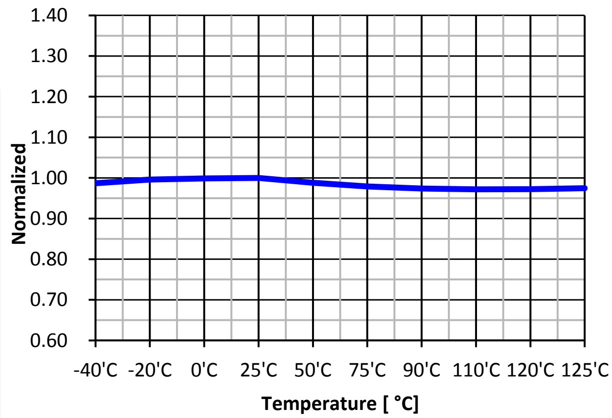

Figure 6. Operating Switching Current (I_{OPS}) vs. T_A

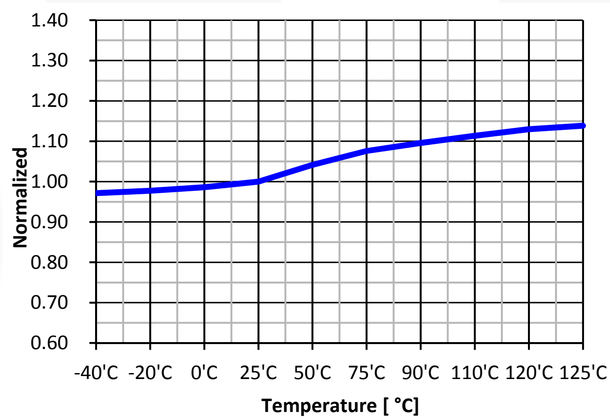

Figure 7. Startup Charging Current (I_{CH}) vs. T_A

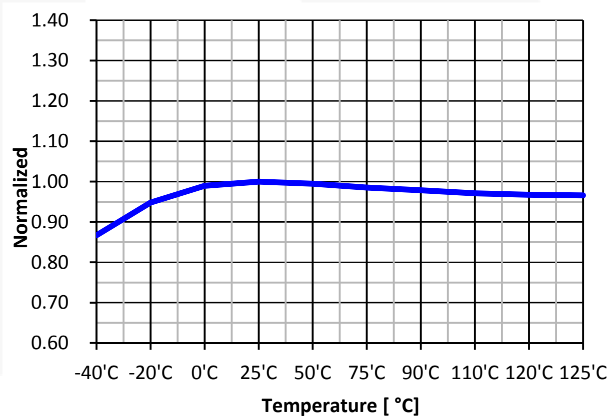

Figure 8. Peak Drain Current Limit (I_{LIM}) vs. T_A

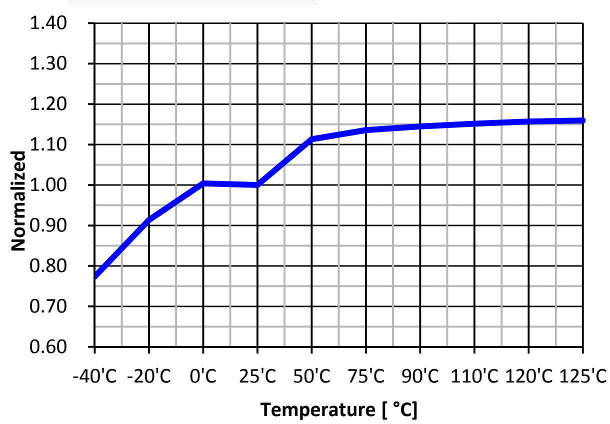

Figure 9. Feedback Source Current (I_{FB}) vs. T_A

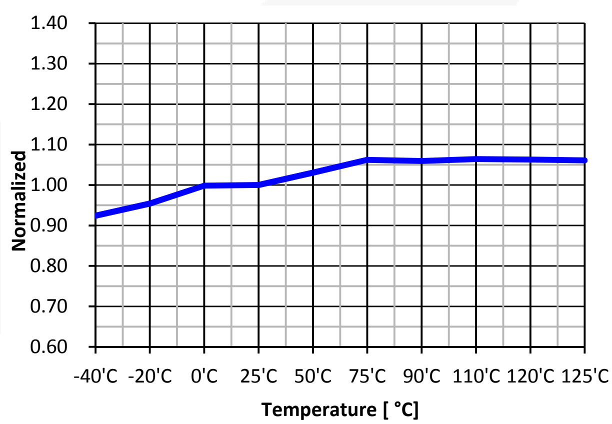

Figure 10. Shutdown Delay Current (I_{DELAY}) vs. T_A

Typical Performance Characteristics

Characteristic graphs are normalized at T_A=25°C.

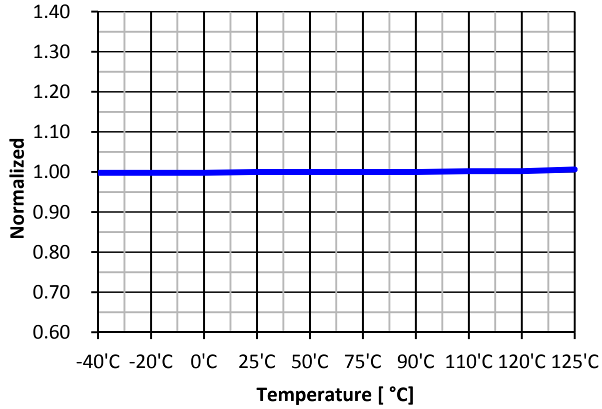

Figure 11. UVLO Threshold Voltage (V_{START}) vs. T_A

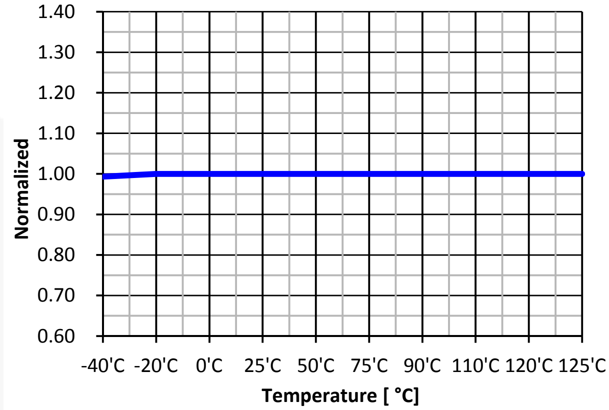

Figure 12. UVLO Threshold Voltage (V_{STOP}) vs. T_A

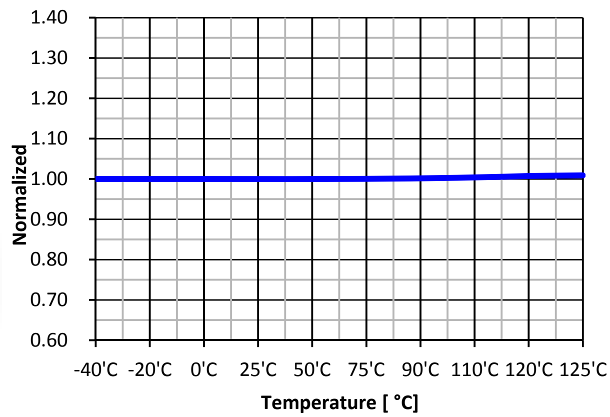

Figure 13. Shutdown Feedback Voltage (V_{SD}) vs. T_A

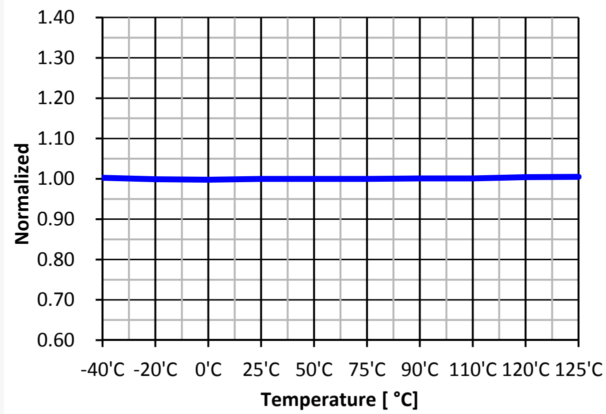

Figure 14. Over-Voltage Protection (V_{OVP}) vs. T_A

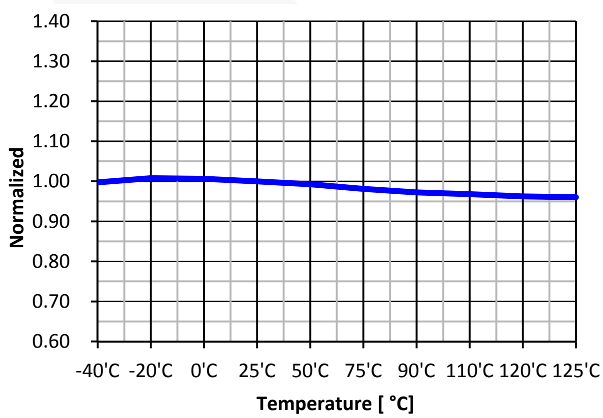

Figure 15. Switching Frequency (f_S) vs. T_A

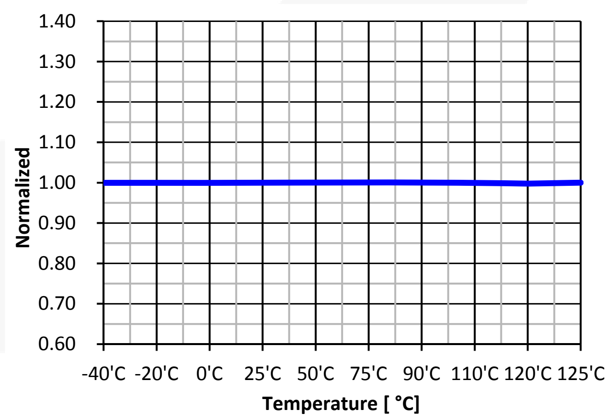

Figure 16. Maximum Duty Ratio (D_{MAX}) vs. T_A

Functional Description

1. Startup: At startup, an internal high-voltage current source supplies the internal bias and charges the external capacitor (C_{VCC}) connected to the V_{CC} pin, as illustrated in Figure 17. When V_{CC} reaches 12V, the FSL136MRT begins switching and the internal high-voltage current source is disabled. Normal switching operation continues and the power is supplied from the auxiliary transformer winding unless V_{CC} goes below the stop voltage of 7.5V.

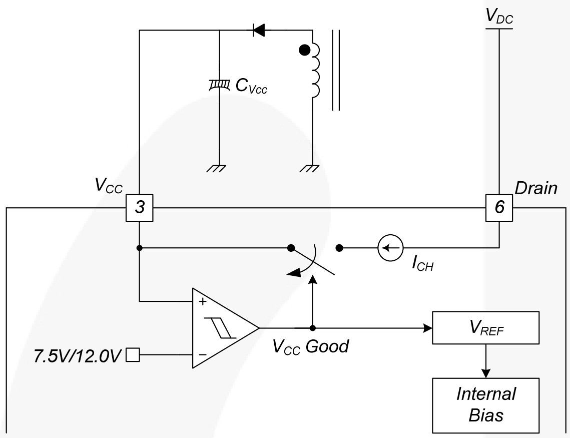

Figure 17. Startup Block

2. Soft-Start: The internal soft-start circuit increases PWM comparator inverting input voltage, together with the SenseFET current, slowly after startup. The typical soft-start time is 15ms. The pulse width to the power switching device is progressively increased to establish the correct working conditions for the transformers, inductors, and capacitors. The voltage on the output capacitors is progressively increased to smoothly establish the required output voltage. This helps prevent transformer saturation and reduces stress on the secondary diode during startup.

3. Feedback Control: This device employs Current-Mode control, as shown in Figure 18. An opto-coupler (such as the FOD817) and shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the R_{SENSE} resistor makes it possible to control the switching duty cycle. When the reference pin voltage of the shunt regulator exceeds the internal reference voltage of 2.5V, the opto-coupler LED current increases, pulling down the feedback voltage and reducing drain current. This typically occurs when the input voltage is increased or the output load is decreased.

3.1 Pulse-by-Pulse Current Limit: Because Current-Mode control is employed, the peak current through the SenseFET is limited by the inverting input of PWM comparator (V_{FB}*), as shown in Figure 18. Assuming that the 90µA current source flows only through the internal resistor (3R + R =27kΩ), the cathode voltage of diode D2 is about 2.4V. Since D1 is blocked when the feedback voltage (V_{FB}) exceeds 2.4V, the maximum voltage of the cathode of D2 is clamped at this voltage. Therefore, the peak value of the current through the SenseFET is limited.

3.2 Leading-Edge Blanking (LEB): At the instant the internal SenseFET is turned on, a high-current spike usually occurs through the SenseFET, caused by primary-side capacitance and secondary-side rectifier reverse recovery. Excessive voltage across the R_{SENSE} resistor leads to incorrect feedback operation in the Current-Mode PWM control. To counter this effect, the leading-edge blanking (LEB) circuit inhibits the PWM comparator for t_{LEB} (350ns) after the SenseFET is turned on.

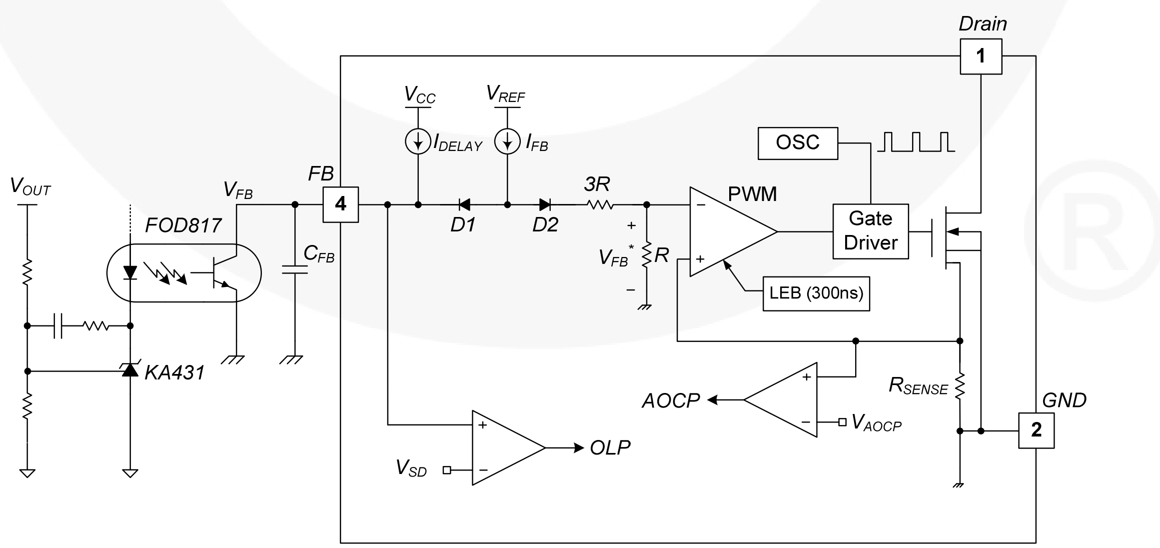

Figure 18. Pulse Width Modulation Circuit

4. Protection Circuits: The FSL136MRT has several self-protective functions, such as Overload Protection (OLP), Abnormal Over-Current Protection (AOCP), Over-Voltage Protection (OVP), and Thermal Shutdown (TSD). All the protections are implemented as auto-restart. Once the fault condition is detected, switching is terminated and the SenseFET remains off. This causes V_{CC} to fall. When V_{CC} falls to the Under-Voltage Lockout (UVLO) stop voltage of 7.5V, the protection is reset and the startup circuit charges the V_{CC} capacitor. When V_{CC} reaches the start voltage of 12.0V, the FSL136MRT resumes normal operation. If the fault condition is not removed, the SenseFET remains off and V_{CC} drops to stop voltage again. In this manner, the auto-restart can alternately enable and disable the switching of the power SenseFET until the fault condition is eliminated. Because these protection circuits are fully integrated into the IC without external components, reliability is improved without increasing cost.

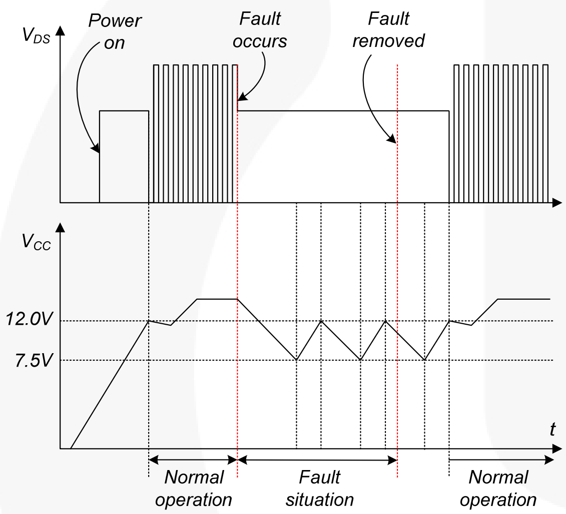

Figure 19. Auto-Restart Protection Waveforms

4.1 Overload Protection (OLP): Overload is defined as the load current exceeding its normal level due to an unexpected abnormal event. In this situation, the protection circuit should trigger to protect the SMPS. However, even when the SMPS is in normal operation, the overload protection circuit can be triggered during the load transition. To avoid this undesired operation, the overload protection circuit is designed to trigger only after a specified time to determine whether it is a transient situation or a true overload situation. Because of the pulse-by-pulse current limit capability, the maximum peak current through the SenseFET is limited and, therefore, the maximum input power is restricted with a given input voltage. If the output consumes more than this maximum power, the output voltage (V_{OUT}) decreases below the set voltage. This reduces the current through the opto-coupler LED, which also reduces the opto-coupler transistor current, increasing the feedback voltage (V_{FB}). If V_{FB} exceeds 2.4V, D1 is blocked and the 2.0µA current source starts to charge C_{FB} slowly up. In this condition, V_{FB} continues increasing until it reaches 7.0V, when the switching operation is terminated, as shown in Figure 20. The delay for shutdown is the time required to charge C_{FB} from 2.4V to 7.0V with 2.0µA. This protection is implemented in Auto-Restart Mode.

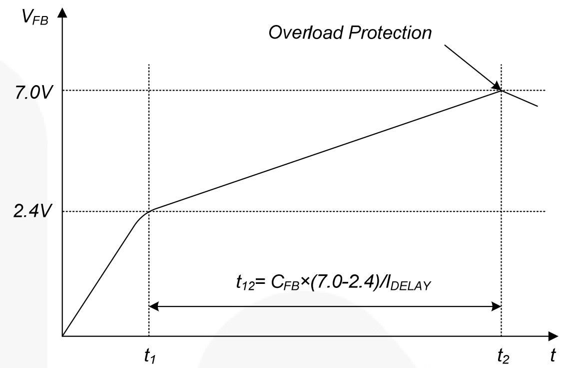

Figure 20. Overload Protection

4.2 Abnormal Over-Current Protection (AOCP): When the secondary rectifier diodes or the transformer pins are shorted, a steep current with extremely high di/dt can flow through the SenseFET during the minimum turn-on time. Even though the FSL136MRT has overload protection, it is not enough to protect the FSL136MRT in that abnormal case; due to the severe current stress imposed on the SenseFET until OLP is triggered. The internal AOCP circuit is shown in Figure 21. When the gate turn-on signal is applied to the power SenseFET, the AOCP block is enabled and monitors the current through the sensing resistor. The voltage across the resistor is compared with a preset AOCP level. If the sensing resistor voltage is greater than the AOCP level, the set signal is applied to the S−R latch, resulting in the shutdown of the SMPS.

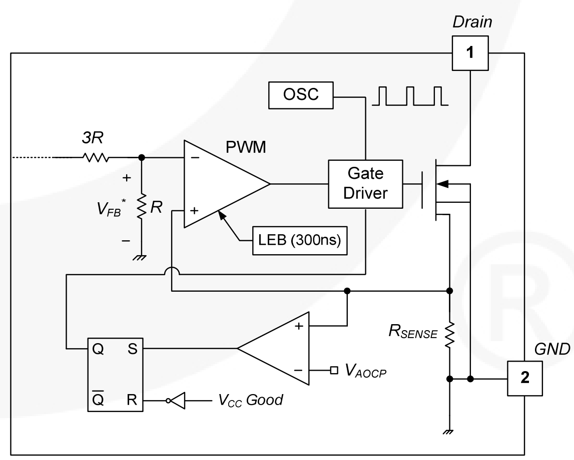

Figure 21. Abnormal Over-Current Protection

4.4 Over-Voltage Protection (OVP): If the secondary-side feedback circuit malfunctions or a solder defect causes an opening in the feedback path, the current through the opto-coupler transistor becomes almost zero. Then V_{FB} climbs up in a similar manner to the overload situation, forcing the preset maximum current to be supplied to the SMPS until the overload protection is triggered. Because more energy than required is provided to the output, the output voltage may exceed the rated voltage before the overload protection is triggered, resulting in the breakdown of the devices in the secondary side. To prevent this situation, an OVP circuit is employed. In general, the V_{CC} is proportional to the output voltage and the FS136MRT uses V_{CC} instead of directly monitoring the output voltage. If V_{CC} exceeds 24.5V, an OVP circuit is triggered, resulting in the termination of the switching operation. To avoid undesired activation of OVP during normal operation, V_{CC} should be designed to be below 24.5V.

4.5 Thermal Shutdown (TSD): The SenseFET and the control IC on a die in one package makes it easier for the control IC to detect the over temperature of the SenseFET. If the temperature exceeds 140°C, the thermal shutdown is triggered and stops operation. The FSL136MRT operates in Auto-Restart Mode until the temperature decreases to around 80°C, when normal operation resumes.

5. Soft Burst-Mode Operation: To minimize power dissipation in Standby Mode, the FSL136MRT enters Burst-Mode operation. As the load decreases, the feedback voltage decreases. The device automatically enters Burst Mode when the feedback voltage drops below V_{BURL} (300mV), as shown in Figure 22. At this point, switching stops and the output voltages start to drop at a rate dependent on standby current load. This causes the feedback voltage to rise. Once it passes V_{BURH} (450mV), switching resumes. The feedback voltage then falls and the process repeats. Burst Mode alternately enables and disables switching of the SenseFET, reducing switching loss in Standby Mode.

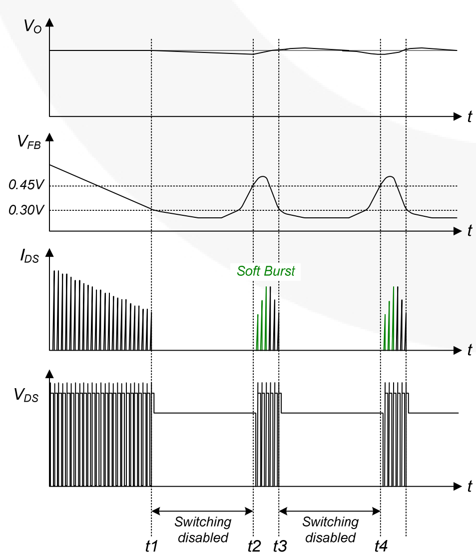

Figure 22. Burst-Mode Operation

6. Random Frequency Fluctuation (RFF): Fluctuating switching frequency of an SMPS can reduce EMI by spreading the energy over a wide frequency range. The amount of EMI reduction is directly related to the switching frequency variation, which is limited internally. The switching frequency is determined randomly by external feedback voltage and an internal free-running oscillator at every switching instant. This random frequency fluctuation scatters the EMI noise around typical switching frequency (67kHz) effectively and can reduce the cost of the input filter included to meet the EMI requirements (e.g. EN55022).

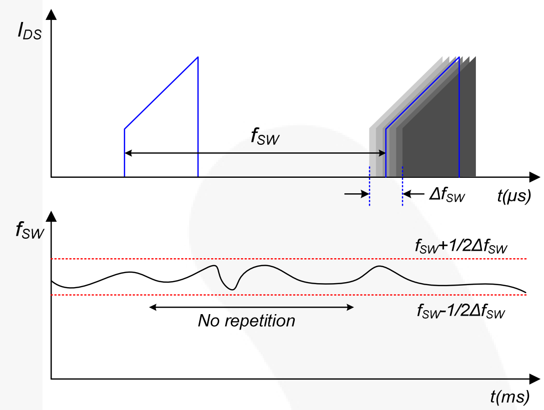

Figure 23. Random Frequency Fluctuation

Physical Dimensions

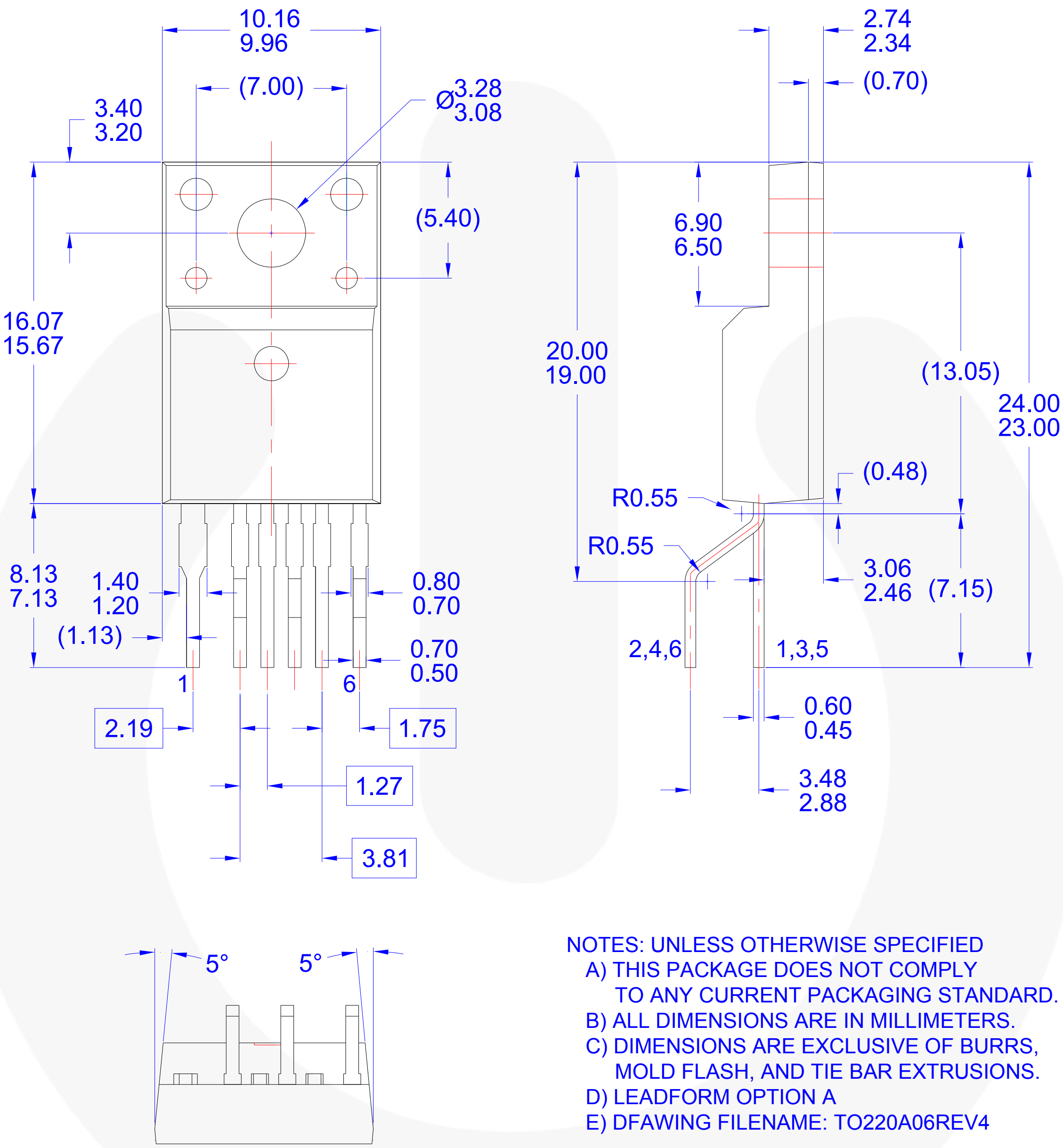

Figure 24. TO−220F−6L (W−Forming)

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FastvCore™
FETBench™
FlashWriter®*
FPS™
F-PFS™
FRFET®
Global Power Resource℠
GreenBridge™
Green FPS™
Green FPS™ e-Series™
G*max*™
GTO™
IntelliMAX™
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Making Small Speakers Sound Louder and Better™
MegaBuck™
MICROCOUPLER™
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mWSaver™
OptoHiT™
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®
PowerTrench®
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Programmable Active Droop™
QFET®
QS™
Quiet Series™
RapidConfigure™
™
Saving our world, 1mW/W/kW at a time™
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SmartMax™
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Solutions for Your Success™
SPM®
STEALTH™
SuperFET®
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SuperSOT™-6
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TinyBoost™
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TriFault Detect™
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Definition of Terms

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