PaceMips™ R2010A FPA 32-BIT RISC CO-PROCESSOR (FLOATING POINT ACCELERATOR)

PRELIMINARY

FEATURES

- 32-BIT RISC Co-Processor:
  - Contains sixteen 64-bit registers to support single-precision or double-precision arithmetic
- Fully conforms to the requirements of ANSI/IEEE Standard 754-1985, "IEEE Standard for Binary Floating Point Arithmetic"
- Up to three PaceMips R2010A Co-Processors can be used with the PR2000A Processor
- Compatible with the MIPS R3010 RISC Co-Processor
- Comprehensive System Development Support
- Produced with PACE II Technology™
- Tightly-coupled interface with the PaceMips R2000A increases system performance:
  - 5 MFLOPS for single precision and 3 MFLOPS for double precision arithmetic when used with the PaceMips R2000A RISC Processor (Floating Point Operations for LINPACK Benchmark)
- Available Package:
  - 84 Pin Quad J-Lead CerPak
- Military Temperature and MIL-STD-883C, Class B devices

DESCRIPTION

The PaceMips R2010A Co-Processor is a floating point accelerator that operates in conjunction with the PaceMips R2000A Processor and fully supports the requirements of ANSI/IEEE Standard 754-1985, "IEEE Standard for Binary Floating Point Arithmetic".

Like the PaceMips R2000A, the PR2010A uses a LOAD/STORE architecture to increase system performance. In a LOAD/STORE architecture all operations are carried out on operands contained in the processor registers, and only the load and store instructions can access the main memory system. Included in the PR2010A there are sixteen 64-bit registers that can be used to store both single and double-precision values. All IEEE-Standard exception handling requirements are supported by a 32-bit status/control register. The PR2010A is functionally compatible with the PR3010 25MHz Floating Point Accelerator.

The PaceMips R2010A Co-Processor is manufactured using PACE II Technology™ which is Performance Advanced CMOS Engineered to use 0.7 micron effective channel lengths resulting in 400 picoseconds loaded* internal gate delays. PACE Technology includes two-level metal and epitaxial substrates. In addition to very high performance and very high density, the technology features latch-up protection and single event upset protection, and is supported by a Class 1 environment volume production facility.

The PaceMips R3010 Co-Processor is available in a 84 Pin Quad J-Lead CerPak.

* For a fan-in/fan-out of 4 at 85°C junction temperature and 5.0 V supply.

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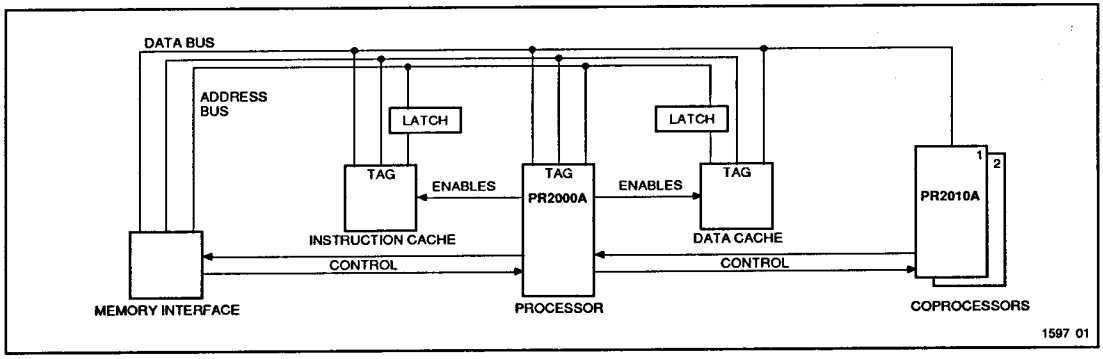
Processor System Block Diagram



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1. SIGNAL DESCRIPTIONS

Data (31:0): (I/O) A multiplexed 32-bit bus used for instruction and data transfers on phase 1 and phase 2, respectively.

DataP(3:0): (O) A 4-bit bus containing even parity over the data bus. Parity is generated by the FPC on stores.

$\overline{\text{Run}}$: (I) Input to the FPC which indicates whether the processor-coprocessor system is in the run or stall state.

$\overline{\text{Exception}}$: (I) Input to the FPC which indicates exception related status information.

FpBusy: (O) Signal to the CPU indicating a request for a coprocessor busy stall.

FpCond: (O) Signal to the CPU indicating the result of the last comparison operation.

$\overline{\text{FpInt}}$: (O) Signal to the CPU indicating that a floating-point exception has occured for the current FPC instruction.

$\overline{\text{Reset}}$: (I) Synchronous initialization input used to distinguish the processor-FPC synchronization period from the execution period. $\overline{\text{Reset}}$ must be synchronized by the leading edge of SysOut from the CPU.

$\overline{\text{PllOn}}$: (I) Input which during the reset period determines whether the phase lock mechanism is enabled and during the execution period determines the output timing model.

$\overline{\text{FpPresent}}$: (O) Output which is pulled to ground through an impedance of approximately 0.5k ohms. By providing an external pullup on this line an indication of the presence or absence of the FPC can be obtained.

Clk2xSys: (I) A double frequency clock input used for generating $\overline{\text{FpSysOut}}$.

Clk2xSmp: (I) A double frequency clock input used to determine the sample point for data coming into the FPC.

Clk2xRd: (I) A double frequency clock input used to determine the disable point for the data drivers.

Clk2xPhI: (I) A double frequency clock input used to determine the position of the internal phases, phase 1 and phase 2.

$\overline{\text{FpSysOut}}$: (O) Synchronization clock from the FPC.

$\overline{\text{FpSysIn}}$: (I) Input used to receive the synchronization clock from the FPC.

$\overline{\text{FpSync}}$: (I) Input used to receive the synchronization clock from the CPU.

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2. ELECTRICAL SPECIFICATIONS

2.1 MAXIMUM RATINGS

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{CC}	Supply Voltage		–.5	+7.0	V
V_{IN}	Input Voltage (1)		–.5	+7.0	V
T_{STG}	Storage Temperature		–65	+150	°C
T_A	Operating Temperature		0	+70	°C

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Notes:
1. V_{IN} Min. = –3.0V for pulse width less than 15ns.
2. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

2.2 RECOMMENDED OPERATING CONDITIONS

Grade	Ambient Temperature	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ± 5%

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2.3 CAPACITIVE LOAD DERATING FACTOR

Symbol	Parameter	Conditions	16MHz		Unit
			Min	Max	
C_{LD}	Load Derate		.5	2	ns/25pF

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2.4 DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	16MHz		Unit
			Min	Max	
V_{OH}	Output HIGH Voltage	V_{CC} = Min I_{OH} = –4mA	3.5		V
V_{OL}	Output LOW Voltage	V_{CC} = Min. I_{OL} = 4mA		.4	V
V_{IH}	Input HIGH Voltage		2	V_{CC} + .5	V
V_{IL} (1)	Input LOW Voltage		–.5	.8	V
V_{IHS}	Input HIGH Voltage		3	V_{CC} + .5	V
V_{ILS}	Input LOW Voltage		–.5	.4	V
V_{IHC}	Input HIGH Voltage		4.0	V_{CC} + .5	V
V_{ILC}	Input LOW Voltage		–.5	.4	V
C_{IN}	Input Capacitance			10	pF
C_{OUT}	Output Capacitance			10	pF
I_{CC}	Operating Current	V_{CC} = 5.5V		550	mA
C_{Ld}	Load Capacitance			100	pF

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Notes:
1. V_{IL} Min. = –3.0V for pulse width less than 15ns.
2. V_{IHS} and V_{ILS} apply to Clk2xSys, Clk2xSmp, Clk2xRd, Clk2Phi, $\overline{\text{FpSysIn}}$, $\overline{\text{FpSync}}$ and $\overline{\text{Reset}}$.
3. V_{IHC} and V_{ILC} apply to $\overline{\text{Run}}$ and $\overline{\text{Exception}}$.
4. Operation above the C_{Ld} maximum may impair the useful life of the device.

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2.5 AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	16MHz		Unit
			Min	Max	
T_{CkHigh}	Input Clock High	Transition ≤ 5ns	12		ns
T_{CkLow}	Input Clock Low	Transition ≤ 5ns	12		ns
T_{CkP}	Input Clock Period		30	1000	ns
	Clk2xSys to Clk2xSmp		0	$t_{Cyc/4}$	ns
	Clk2xSmp to Clk2xRd		0	$t_{Cyc/4}$	ns
	Clk2xSmp to Clk2xPhi		9	$t_{Cyc/4}$	ns
T_{DEn}	Data Enable		–1	–2	ns
T_{DDis}	Data Disable		0	–1	ns
T_{DVal}	Data Valid		2	3	ns
T_{DS}	Data Setup		9		ns
T_{DH}	Data Hold		–2.5		ns
T_{FpCond}	Fp Condition		0	35	ns
T_{FpBusy}	Fp Busy		0	15	ns
T_{FpInt}	Fp Interrupt		0	40	ns
T_{FpMov}	Fp Move To		0	35	ns
T_{ExS}	Exception Setup		10		ns
T_{ExH}	Exception Hold		0		ns
T_{RunS}	Run Setup		10		ns
T_{RunH}	Run Hold		–2		ns

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Notes:
1. All output timings are given assuming 25pF of capacitive load.
2. All timings referenced to 1.5V.
3. The clock parameters apply to all four 2xClocks.

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3. MECHANICAL DATA

3.1 PIN ASSINGMENT AND PACKAGE DIMENSIONS

3.1.1 84 Pin Quad J-Lead CerPak

Table 3.1 Pinout—84 Pin Quad J-Lead CerPak

Pin Name	Pin Number	Pin Name	Pin Number
Data(0)	33	$\overline{\text{FpSync}}$	23
Data(1)	34	$\overline{\text{Reset}}$	22
Data(2)	35	$\overline{\text{PllOn}}$	28
Data(3)	36	$\overline{\text{Run}}$	66
Data(4)	39	$\overline{\text{Exception}}$	67
Data(5)	40	$\overline{\text{FpInt}}$	68
Data(6)	41	FpBusy	69
Data(7)	42	FpCond	70
Data(8)	44	VCC0	7
Data(9)	45	VCC1	15
Data(10)	46	VCC2	24
Data(11)	47	VCC3	26
Data(12)	50	VCC4	29
Data(13)	51	VCC5	31
Data(14)	52	VCC6	38
Data(15)	53	VCC7	49
Data(16)	76	VCC8	55
Data(17)	77	VCC9	57
Data(18)	78	VCC10	61
Data(19)	79	VCC11	63
Data(20)	82	VCC12	72
Data(21)	83	VCC13	75
Data(22)	84	VCC14	81
Data(23)	1	Gnd0	6
Data(24)	3	Gnd1	16
Data(25)	4	Gnd2	25
Data(26)	5	Gnd3	27
Data(27)	8	Gnd4	30
Data(28)	9	Gnd5	32
Data(29)	10	Gnd6	37
Data(30)	11	Gnd7	48
Data(31)	14	Gnd8	54
DataP(0)	43	Gnd9	56
DataP(1)	73	Gnd10	60
DataP(2)	2	Gnd11	62
DataP(3)	17	Gnd12	71
Clk2xSys	19	Gnd13	74
Clk2xSmp	20	Gnd14	80
Clk2xRd	12	Resvd0	58
Clk2xPhi	21	Resvd1	64
$\overline{\text{FpSysIn}}$	13	Resvd2	65
$\overline{\text{FpSysOut}}$	18	$\overline{\text{FpPresent}}$	59

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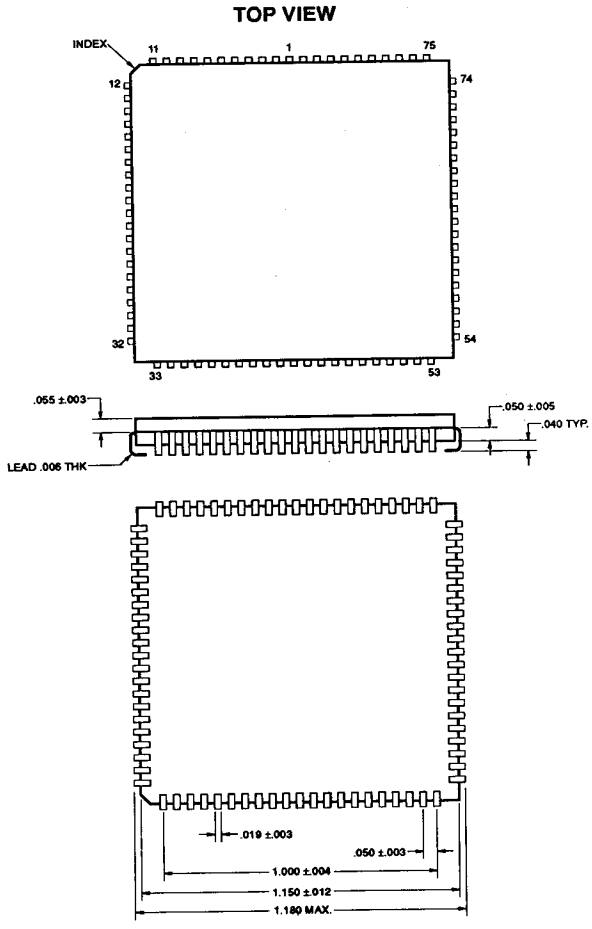
Figure 3.1 Dimensions—84 Pin Quad J-Lead CerPak



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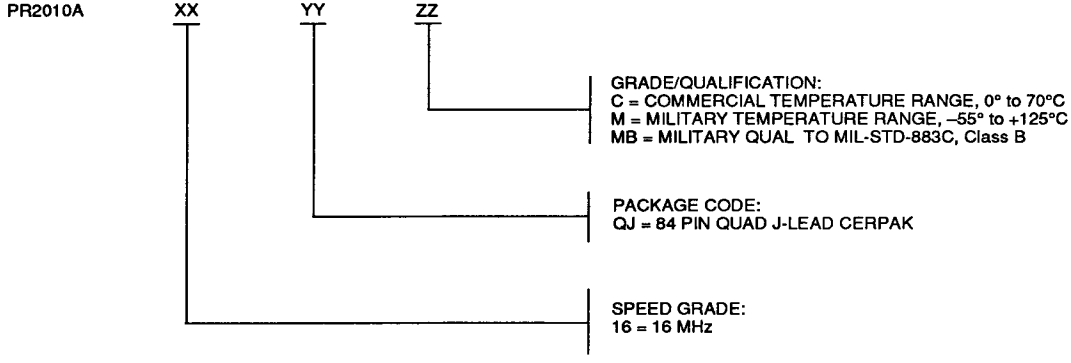
3.2 MOUNTING

A variety of sockets allow low insertion force or zero insertion force mountings, and a choice of terminals such as soldertail, surface mounts or wire wrap. Several sockets are available from the following sample list of socket manufacturers. Contact the manufacturer directly for the latest socket specifications.

- AMP Incorporated
  P.O. Box 3608
  Harrisburg, PA 17105-3608
  (800) 522-6752
- Burndy Corporation
  Richards Avenue
  Norwalk, CT 06856
  (203) 838-4444
- Yamaichi Electronics Inc.
  1425 Koll Circle, Suite 106
  San Jose, CA 95112
  (408) 452-0797
- Textool/3M Test
  and Interconnect Products Department
  3M Austin Center
  P.O. Box 2963
  Austin, TX 78769-2963
  (800) 225-5373

4. ORDERING INFORMATION



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