BGT24MTR12

Silicon Germanium 24 GHz Transceiver MMIC

Preliminary Data Sheet

Revision 2.0, 2012-09-19

RF & Protection Devices

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BGT24MTR12 Silicon Germanium 24 GHz Transceiver MMIC

Revision History: 2012-09-19, Revision 2.0

Previous Revision:

Page	Subjects (major changes since last revision)

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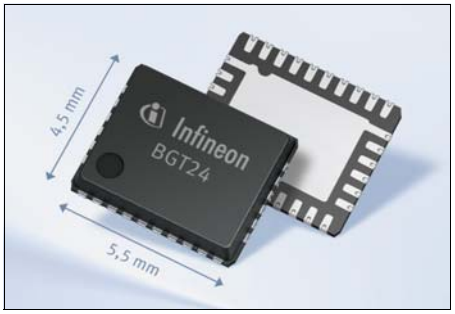

- 24 GHz ISM band transceiver MMIC with one transmitter and two receiver units
- Fully integrated low phase noise VCO
- Switchable prescaler with 1.5 GHz and 23 kHz output
- On chip power and temperature sensors
- Gilbert based homodyne quadrature receiver
- Single ended RF input terminal
- Low noise figure NF_{SSB}: 12 dB
- High conversion gain: 26 dB
- High 1 dB input compression point: -12 dBm
- Single supply voltage 3.3 V
- Low power consumption 660 mW
- 200 GHz bipolar SiGe:C technology b7hf200
- Fully ESD protected device
- VQFN-32-9 leadless plastic package incl. LTI feature
- Pb-free (RoHS compliant) package

RoHS

Description

The BGT24MTR12 is a Silicon Germanium MMIC for signal generation and reception, operating from 24.00 to 26.00 GHz. It is based on a 24 GHz fundamental voltage controlled oscillator. A switchable frequency prescaler is included with output frequencies of 1.5 GHz and 23 kHz. The main RF output delivers up to 8 dBm signal power to feed an antenna. A RC polyphase filter (PPF) is used for LO quadrature phase generation of the homodyne quadrature downconversion mixer. Output power sensors as well as a temperature sensor are implemented for monitoring purposes. The device is controlled via SPI and is manufactured in a 0.18µm SiGe:C technology offering a cutoff frequency of 200 GHz. The MMIC is packaged in a 32 pin leadless RoHs compliant VQFN package.

Product Name	Package	Chip	Marking
BGT24MTR12	VQFN32-9	T0825	BGT24MTR12

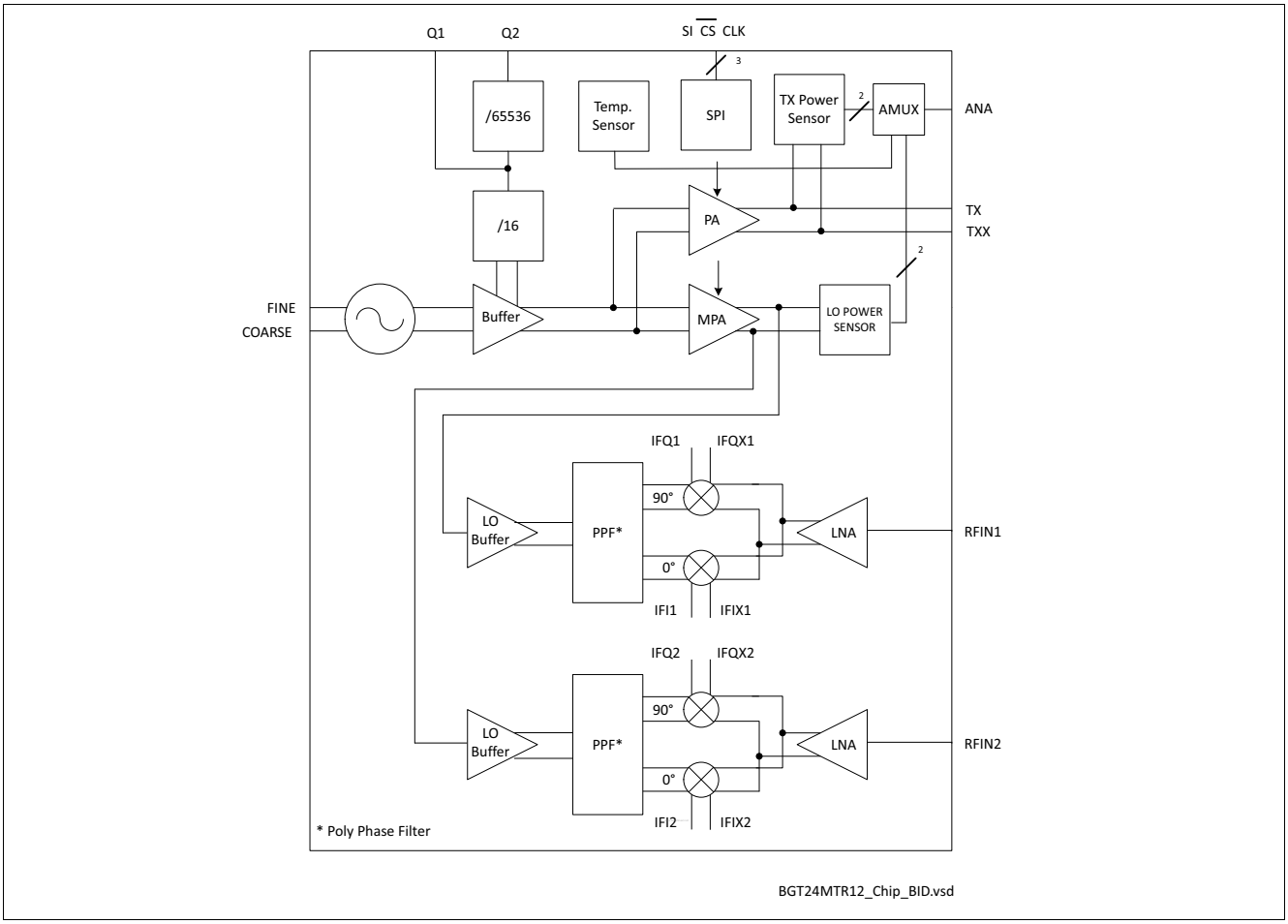

Figure 1 BGT24MTR12 Block Diagram

2 Electrical Characteristics

2.1 Absolute Maximum Ratings

T_A = -40 °C to 105 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)[1)]

Table 1 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{CC}	-0.3	–	3.6	V	–
DC voltage at RF Pins TX, TXX, RFIN1, RFIN2	VDC_{RF}	–	–	0	V	MMIC provides short circuit to GND for all RF pins
DC current into Pins IFxI, IFxIX, IFxQ, IFxQX	I_{IF}	-6	–	3.5	mA	max. values indicate current due to short circuit to GND and Vcc respectively
DC current into Pin ANA	I_{ANA}	-5	–	0.3	mA	max. values indicate current due to short circuit to GND and Vcc respectively
DC current into Pin Q1	I_{Q1}	-8	–	8	mA	–
DC current into Pin Q2	I_{Q2}	-2.2	–	2.2	mA	–
RF input power into Pins RFIN1, RFIN2	P_{RF}	–	–	0	dBm	–
DC voltage at Pins Fine, Coarse	V_{Fine}, $V_{FCoarse}$	0	–	5	V	–
Total power dissipation	P_{DISS}	–	–	830	mW	–
Junction temperature	T_J	-40	–	150	°C	–
Ambient temperature range	T_A	-40	–	105	°C	T_A = temperature at package soldering point
Storage temperature range	T_{STG}	-40	–	150	°C	–

Attention: Stresses exceeding the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

1) Not subject to production test, specified by design

2.2 Thermal Resistance

Table 2 Thermal Resistance

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Junction - soldering point[1)]	R_{thJS}	–	–	40	K/W	–

1) For calculation of R_{thJS} please refer to application note thermal resistance

2.3 ESD Integrity

Table 3 ESD Integrity

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ESD robustness RFIN1, RFIN2, TX, TXX[1)]	$V_{ESD-HBM}$	1000	–	–	V	All RF-pins
ESD robustness low frequency and DC pins[1)]	$V_{ESD-HBM}$	1000	–	–	V	All other pins

1) According to ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing, Human Body Model (HBM)-Component Level, ANSI/ESDA/JEDEC JS-001-2011
Please note that this result is subject to
- lot variations within the manufacturing process as specified by Infineon
- changes in the specific test setup

2.4 Measured RF Characteristics

2.4.1 Power Supply

Table 4 Typical Characteristics T_A = -40 .. 105 °C

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{CC}	3.135	3.3	3.465	V	–
Supply current	I_{CC}	170	200	230	mA	Max. TX output power, all prescalers are activated, LO and TX output buffer in high mode

2.4.2 TX Section

Table 5 Typical Characteristics T_A = -40 .. 105 °C[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
VCO frequency range	f_{VCO}	24.00	–	26.00	GHz	–
VCO tuning voltage	V_{Fine}, $V_{FCoarse}$	0.5[2)]	–	5[3)]	V	At tuning pins chip-internal pull-up of 60kΩ to VCC
VCO tuning slope	$\Delta f / \Delta V_{FINE}$	–	–	1000	MHz/V	–
VCO tuning slope	$\Delta f / \Delta V_{COARSE}$	–	–	1800	MHz/V	–
VCO pushing	$\Delta f / \Delta V_{CC}$	–	–	300	MHz/V	@ f = 24 GHz
VCO phase noise	P_N	–	-85	-75	dBc/Hz	@ 100kHz offset
TX/TXX load impedance[4)]	Z_{TXLOAD}	–	100	–	Ω	With off chip compensation network as proposed
Max. TX output power	P_{TX}	1	8	12	dBm	Combined output power
TX ouput power adjustable range	a_{TX}	3	9	–	dB	Adjustable via SPI
TX ouput power in “off” mode	P_{TXoff}	–	–	-15	dBm	–
Q1 Prescaler division ratio	D_{Q1}	–	16	–	–	–
Q1 Prescaler output power	P_{Q1}	-12	-9	-6	dBm	Q1 loaded with 100 Ohm (AC- coupled)
Q2 Prescaler division ratio	D_{Q2}	–	1048576	–	–	–

Table 5 Typical Characteristics T_A = -40 .. 105 °C[1)] (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Q2 Prescaler max. output voltage	V_{maxQ2}	Vcc-0.7	–	–	V	Test condition: Q2 loaded with high impedance probe (1 MOhm,13 pF)
Q2 Prescaler min. output voltage	V_{minQ2}	–	–	0.5	V	Test condition: Q2 loaded with high impedance probe (1 MOhm, 13 pF)
Q2 Prescaler max. output source current	$I_{maxsource\ Q2}$	2	–	–	mA	Test condition: Q2 loaded with 50 Ohm to Vcc
Q2 Prescaler max. output sink current	$I_{maxsink\ Q2}$	2	–	–	mA	Test condition: Q2 loaded with 50 Ohm to Vcc

1) Performance based on application circuit in Figure 2 on Page 14
2) Min. limit @ 25°C = 0.8V; min. limit @ 105°C = 1.15V
3) Max. limit for max. frequency of 24.25GHz = 3.1V; max. limit for max. frequency of 24.5GHz = 3.8V
4) Guaranteed by device design

2.4.3 RX Section

Table 6 Typical Characteristics T_A = -40 .. 105 °C[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RFIN frequency range	f_{RFIN}	24.00	–	26.00	GHz	–
RFIN port impedance[2)]	Z_{RFIN}	–	50	–	Ω	With off chip compensation network as proposed
RFIN VSWR	$VSWR$	–	–	2:1	–	With off chip compensation network as proposed
IF frequency range	f_{IF}	0	–	1	MHz	–
IF port impedance[2)]	Z_{IF}	–	800	–	Ω	Differential
Voltage conversion gain	G_C	18	26	33	dB	$R_{LOAD,IF}$ > 10 kΩ
SSB noise figure	N_{SSB}	–	12	20	dB	Single sideband at f_{IF} = 100 kHz
IF 1/f corner frequency	f_c	–	10	20	kHz	–
Input compression point	IP_{1dB}	-18	-12	–	dBm	–
Input 3rd order intercept point	$IIP3$	-8	-4	–	dBm	–
Quadrat. phase imbalance	ε_p	–	–	10	deg	–
Quadrat. amplitude imbalance	ε_A	–	–	1	dB	–

1) Performance based on application circuit in Figure 2 on Page 14
2) Guaranteed by device design

2.5 Temperature Sensor

Monitoring of the chip temperature is provided by the on-chip temperature sensor which delivers temperature-proportional voltage.

Table 7 Typical Characteristics Temperature Sensor T_A = -40 .. 105 °C, V_{CC} = 3.3 V[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Temperature range	T_{TSENS}	-40	–	105	°C	–
Output temperature voltage	$V_{OUT,TEMP}$	–	1.55	–	V	@ 25°C
Sensitivity	S_{TSENS}	3	4	–	mV/K	–

1) all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

2.6 Power Detector

For power indication, peak voltage detectors are connected to the output of the TX power amplifier and to the LO medium power amplifier. To eliminate temperature and supply voltage variations, a reference output VREF is available through the ANA output for the TX and LO power sensor. The compensated detector output voltage is given by the difference between VOUT and VREF for both power sensor respectively. This voltage is proportional to the RF voltage swing at the individual amplifier outputs, its characteristic is non-directional.

Table 8 Typical Characteristics Power Detector T_A = -40 .. 105 °C, V_{CC} = 3.3 V[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power range	P_{PSENS}	-10	–	12	dBm	–
TX power sensor	$V_{OUT,TX}$ - $V_{REF,TX}$	–	500	–	mV	@ P_{TX} = 8 dBm
LO power sensor	$V_{OUT,LO}$ - $V_{REF,LO}$	–	50	–	mV	@ typ. internal P_{LO}

1) all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

3 Application Circuit and Block Diagram

3.1 Application Circuit Schematic

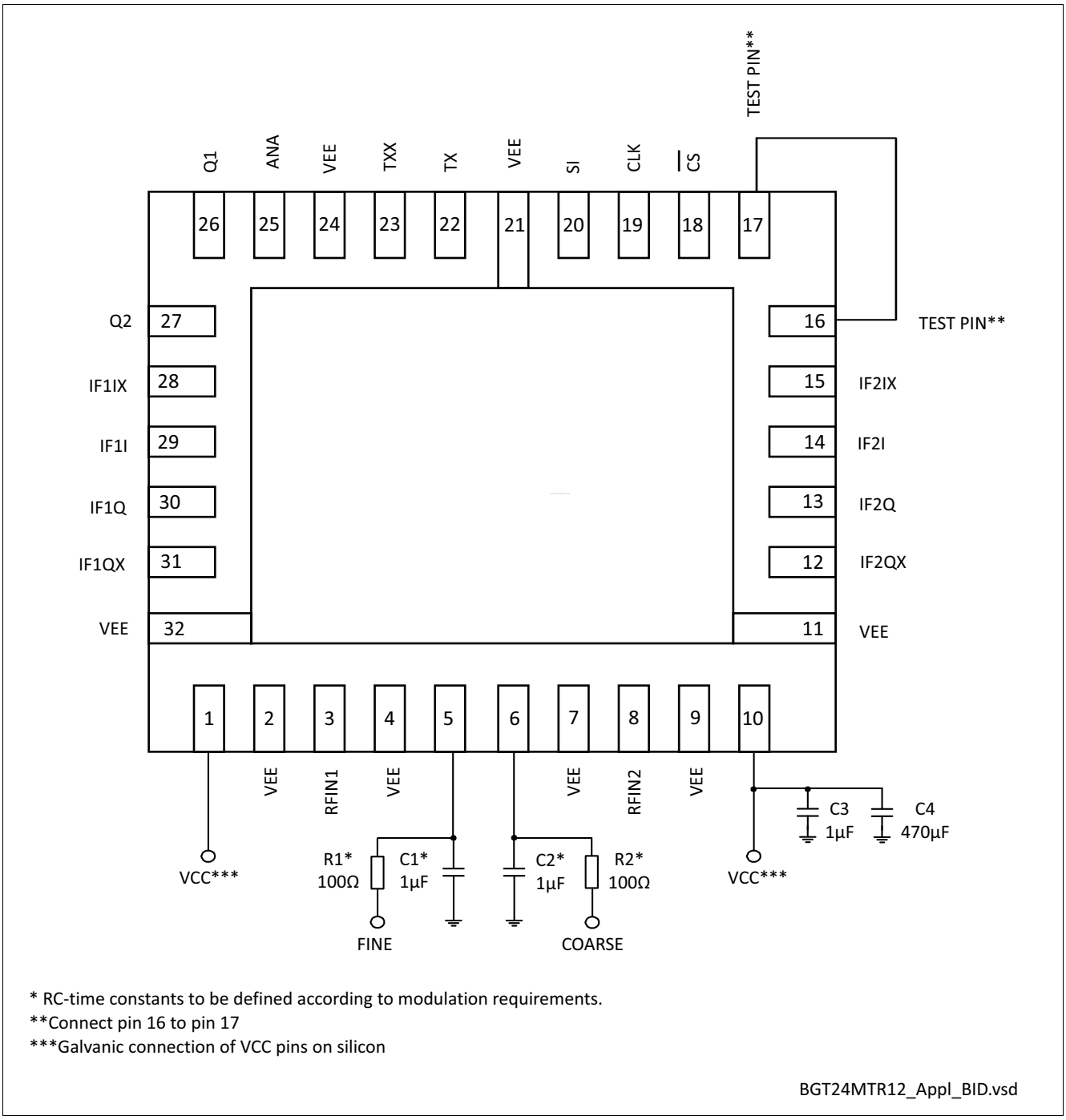

Figure 2 Application Circuit with Chip Outline (Top View)

Table 9 Bill of Materials

Part Number	Part Type	Manufacturer	Size	Comment
C1 ... C4	Chip capacitor	Various	Various	–
R1 ... R2	Chip resistor	Various	0402	–

3.2 Pin Description

Table 10 Pin Definition and Function

Pin No.	Name	Function
1	VCC	Supply voltage
2	VEE	Ground
3	RFIN1	RF input downconverter 1
4	VEE	Ground
5	FINE	VCO fine tuning input
6	COARSE	VCO coarse tuning input
7	VEE	Ground
8	RFIN2	RF input downconverter 2
9	VEE	Ground
10	VCC	Supply voltage
11	VEE	Ground
12	IF2QX	Complementary quadrature phase IF output downconverter 2
13	IF2Q	Quadrature phase IF output downconverter 2
14	IF2I	In phase IF output downconverter 2
15	IF2IX	Complementary in phase IF output downconverter 2
16	TEST PIN	Test pin; DC coupled pin
17	TEST PIN	Test pin; DC coupled pin
18	$\overline{CS}$	Chip select input SPI (inverted)
19	CLK	Clock input SPI block
20	SI	Data input SPI block
21	VEE	Ground
22	TX	Transmit output
23	TXX	Complementary transmit output
24	VEE	Ground
25	ANA	Analog output
26	Q1	Prescaler output 1.5GHz
27	Q2	Prescaler output 23kHz
28	IF1IX	Complementary in phase IF output downconverter 1
29	IF1I	In phase IF output downconverter 1
30	IF1Q	Quadrature phase IF output downconverter 1
31	IF1QX	Complementary quadrature phase IF output downconverter 1
32	VEE	Ground

3.3 SPI

Communication to the transceiver is done via a Serial-Peripheral-Interface (SPI). The 16 bit SPI has a hardwired Power-On reset, which sets the output bits to a defined state after turning on the supply voltage. Data transmission is started by a negative edge on $\overline{CS}$. Data at SI is then read at the falling edge of CLK. The most significant bit (MSB) is read first.

Table 11 SPI Block Data Bit Description

Data Bit	Name	Description (Logic High)	Power ON State
15	GS	LNA Gain reduction	low
14	–	Not used	low
13	AMUX2	Analog multiplexer control bit 2	high
12	DIS_PA	Disable Power Amplifier	high
11	Test Bit	Test bit, must be low otherwise malfunction	low
10	Test Bit	Test bit, must be low otherwise malfunction	low
9	Test Bit	Test bit, must be low otherwise malfunction	low
8	AMUX1	Analog multiplexer control bit 1	low
7	AMUX0	Analog multiplexer control bit 0	low
6	DIS_DIV64k	Disable 64k divider	low
5	DIS_DIV16	Disable 16 divider	low
4	PC2_BUF	High LO buffer output power	low
3	PC1_BUF	High TX buffer output power	low
2	PC2_PA	TX power reduction bit 2	high
1	PC1_PA	TX power reduction bit 1	high
0	PC0_PA	TX power reduction bit 0	high

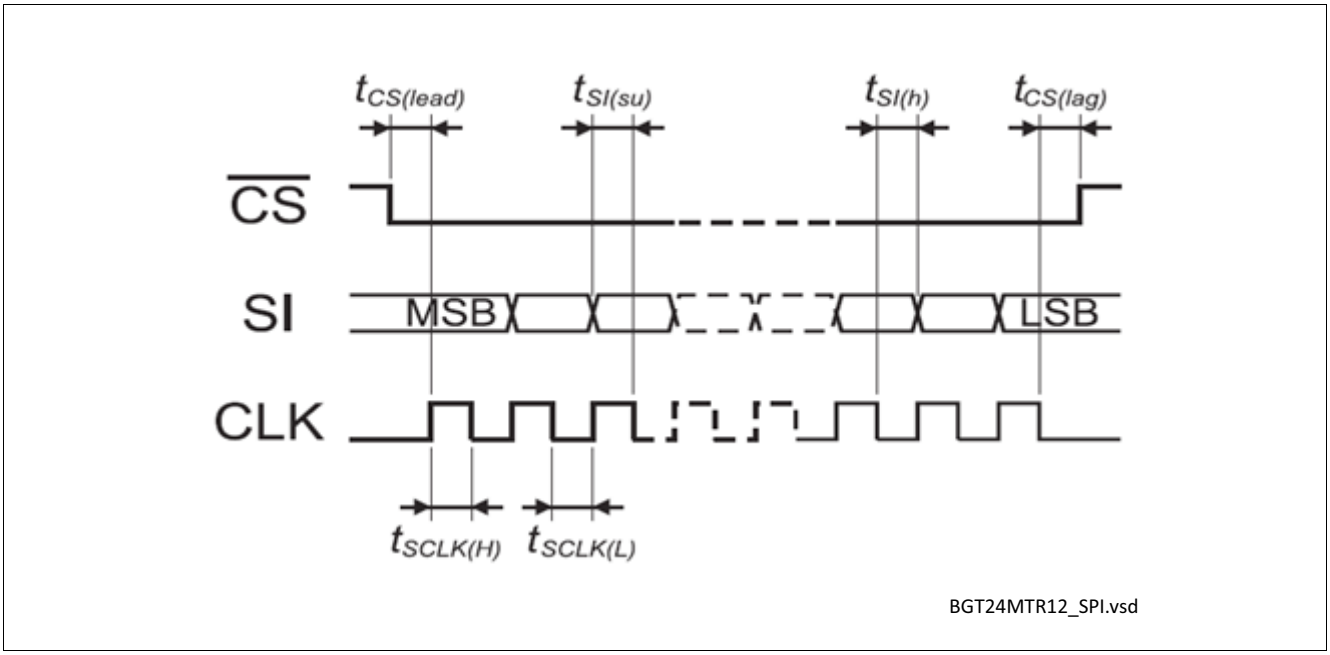

Figure 3 Timing Diagram of the SPI

Table 12 SPI Timing and Logic Levels

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
Serial clock frequency	f_{SCLK}	0	–	50	MHz
Serial clock high time	$f_{SCLK(H)}$	10	–	–	ns
Serial clock low time	$t_{SCLK(L)}$	10	–	–	ns
Chip select lead time	$t_{CS(lead)}$	20	–	–	ns
Chip select lag time	$t_{CS(lag)}$	20	–	–	ns
Data setup time	$t_{SI(su)}$	10	–	–	ns
Data hold time	$t_{SI(h)}$	10	–	–	ns
Low level (SI, CLK, $\overline{CS}$)	$V_{IN(L)}$	0	–	0.8	V
High level (SI, CLK, $\overline{CS}$)	$V_{IN(H)}$	2.0	–	V_{CC} + 0.3V	V
Input current	I_{IN}	-150	–	150	µA

Table 13 Truth Table AMUX

Output signal ANA	AMUX2	AMUX1	AMUX0
$P_{OUT,TX}$	low	low	low
$P_{REF,TX}$	low	low	high
$P_{OUT,LO}$	low	high	low
$P_{REF,LO}$	low	high	high
V_{TEMP}	high	low	low
Test_Signal1	high	low	high
Test_Signal2	high	high	low
Test_Signal2	high	high	high

3.4 Application Board

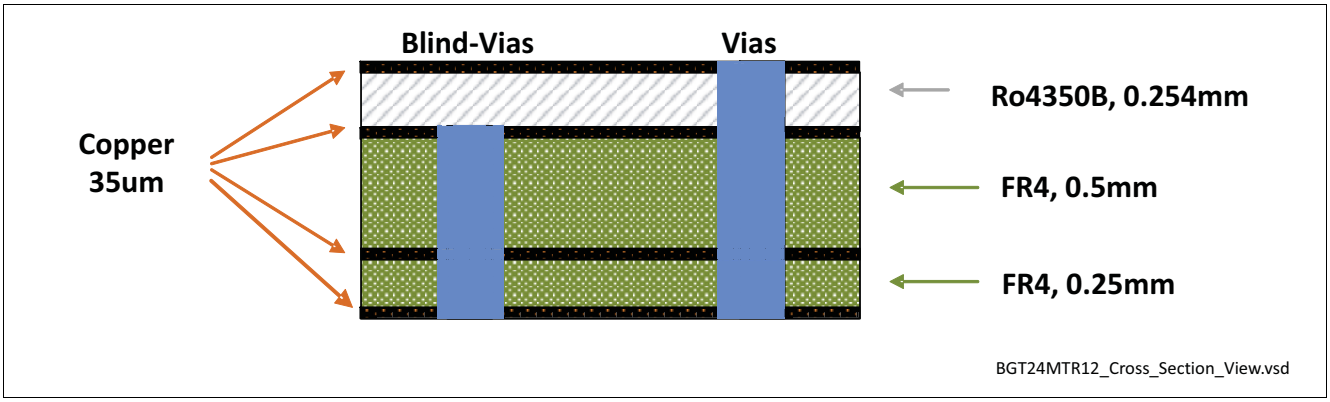

Figure 4 Cross-Section View of Application Board

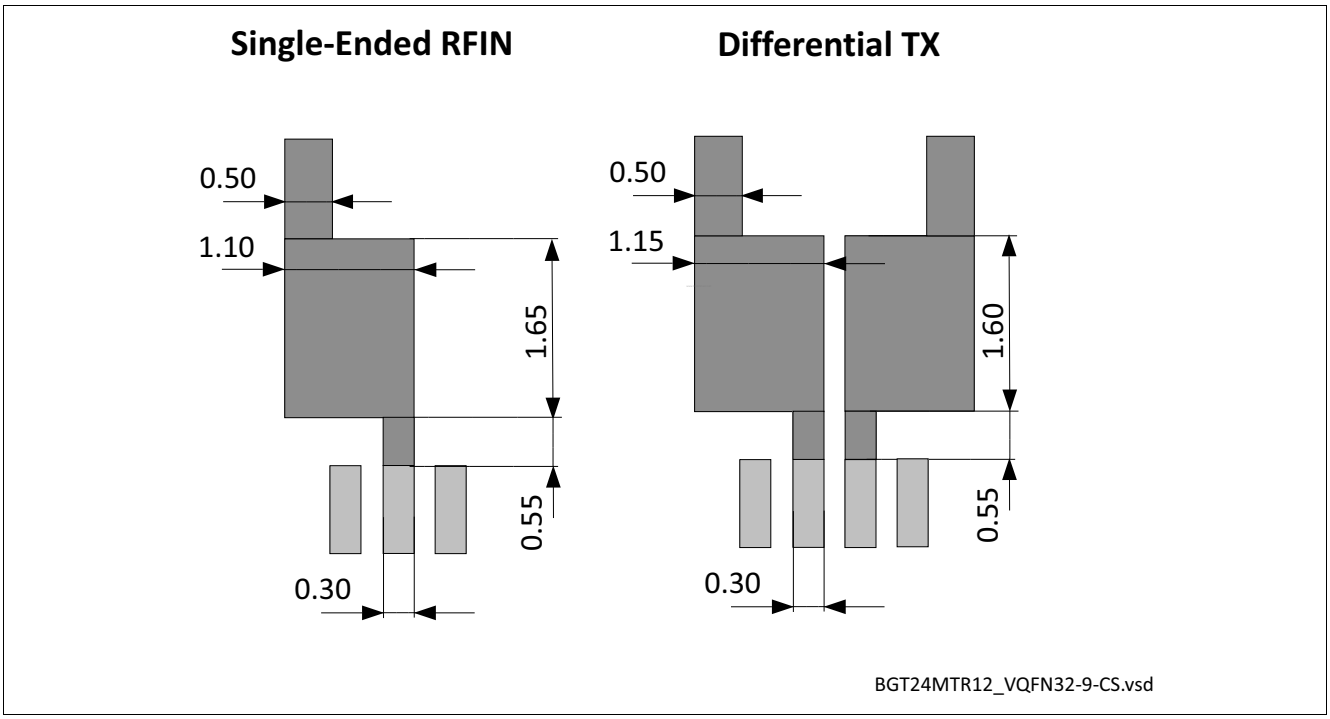

Figure 5 Detail of Compensation Structure

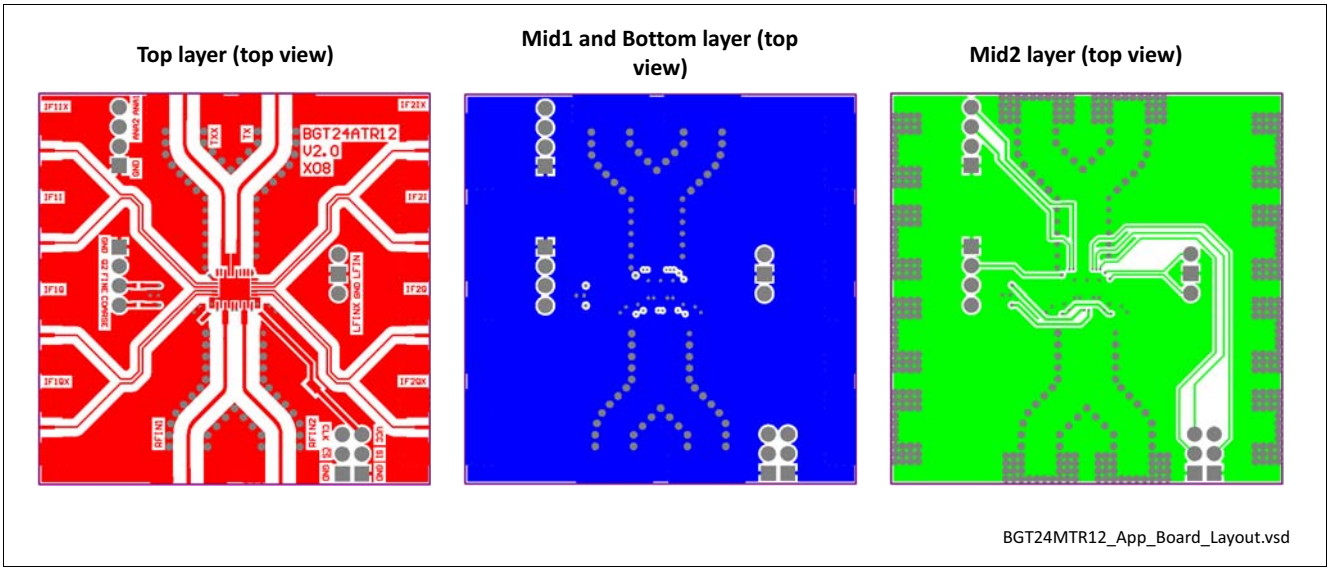

Figure 6 Application Board Layout

Note: In order to achieve the same performance as given in this datasheet please follow the suggested PCB-layout as closely as possible. The compensation structure is critical for RF performance. Via holes as recommended on next page (not shown above).

3.5 Equivalent Circuit Diagram of MMIC Interfaces

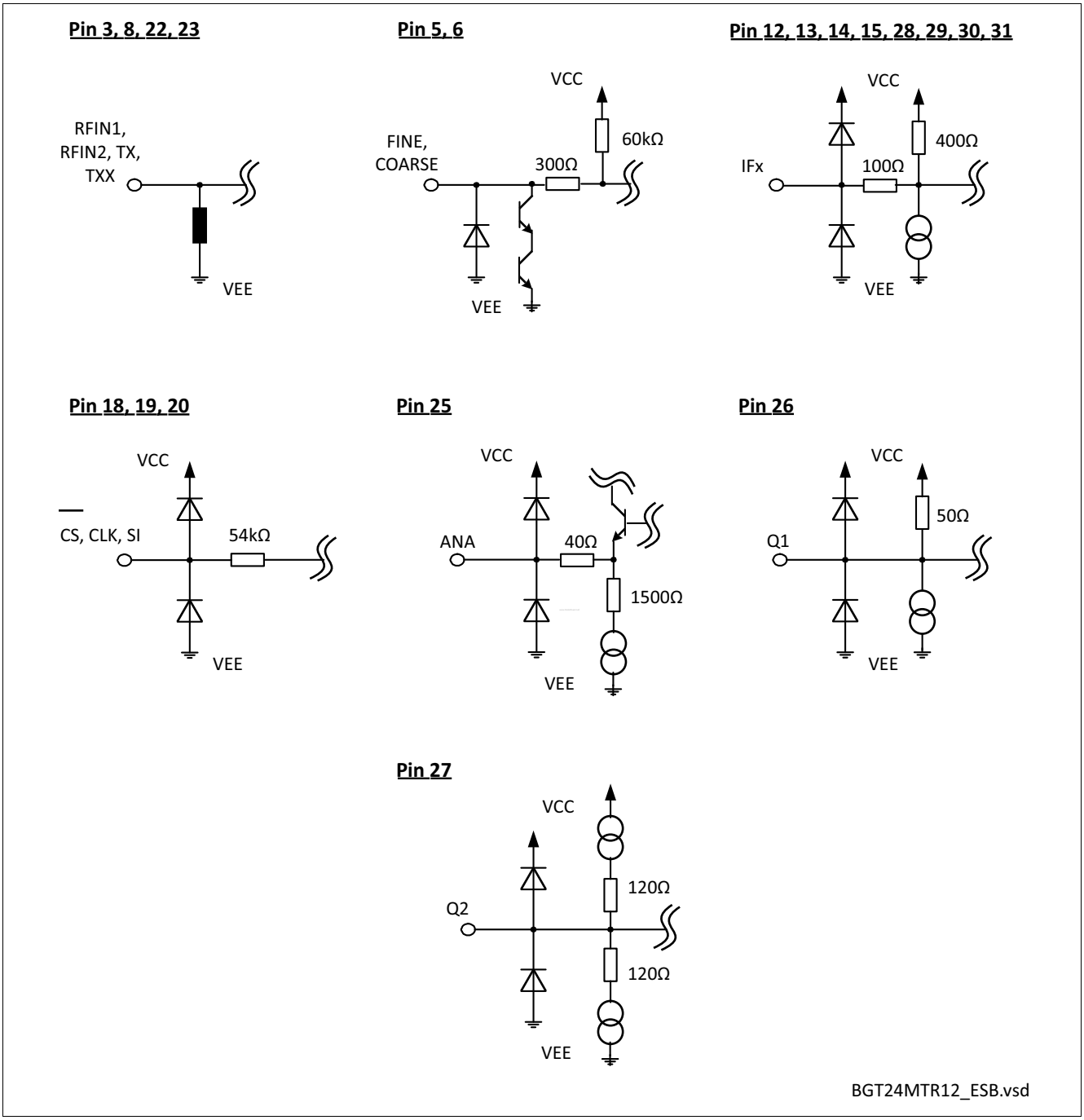

Figure 7 Equivalent Circuit Diagram of MMIC Interfaces

4 Physical Characteristics

4.1 Package Footprint

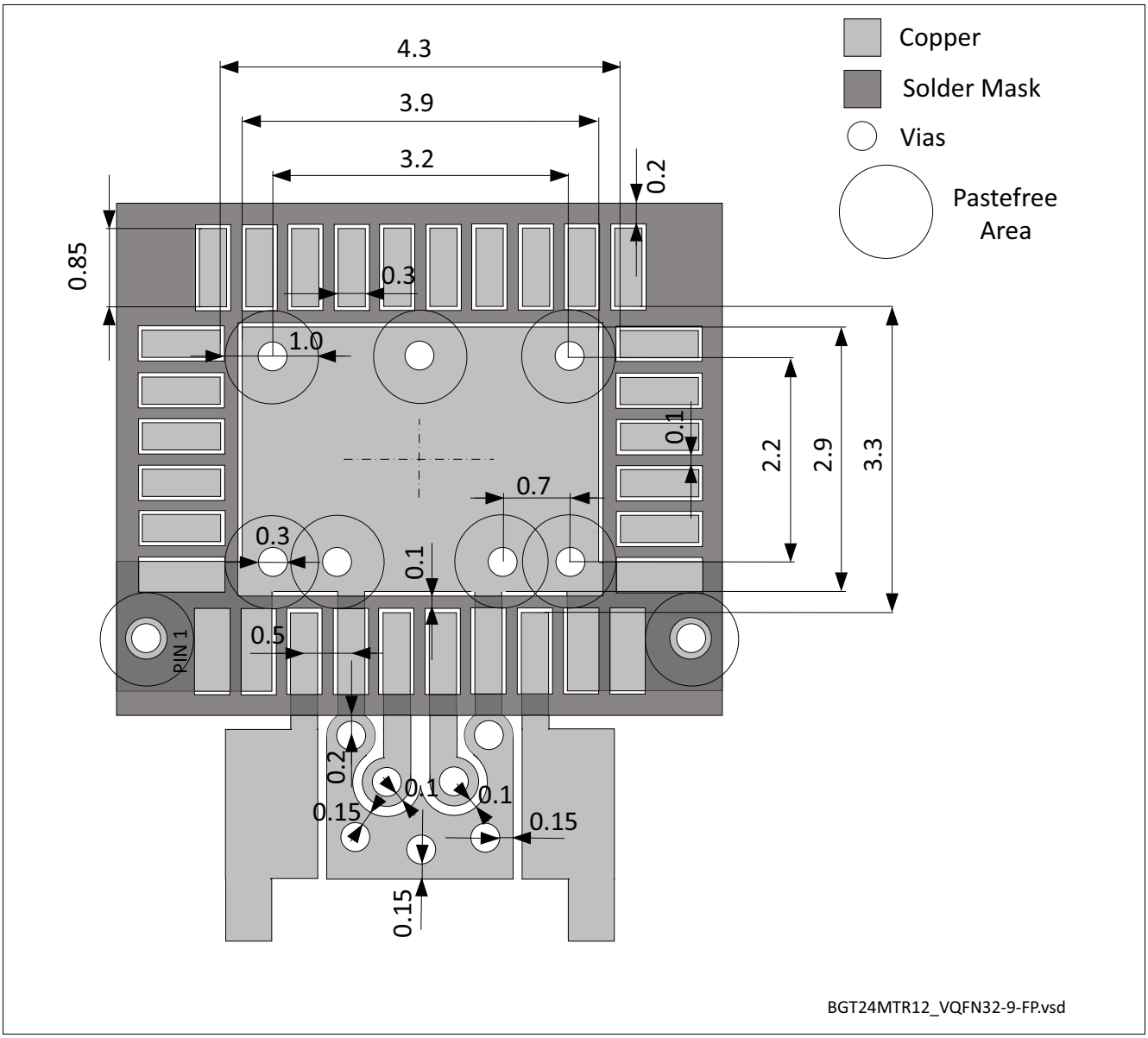

Figure 8 Recommended Footprint and Stencil Layout for the VQFN32-9 Package

4.2 Reflow Profile

Soldering process qualified during qualification with “Preconditioning MSL-3: 30°C. 60%r.h., 192h, according to JEDEC JSTD20”.

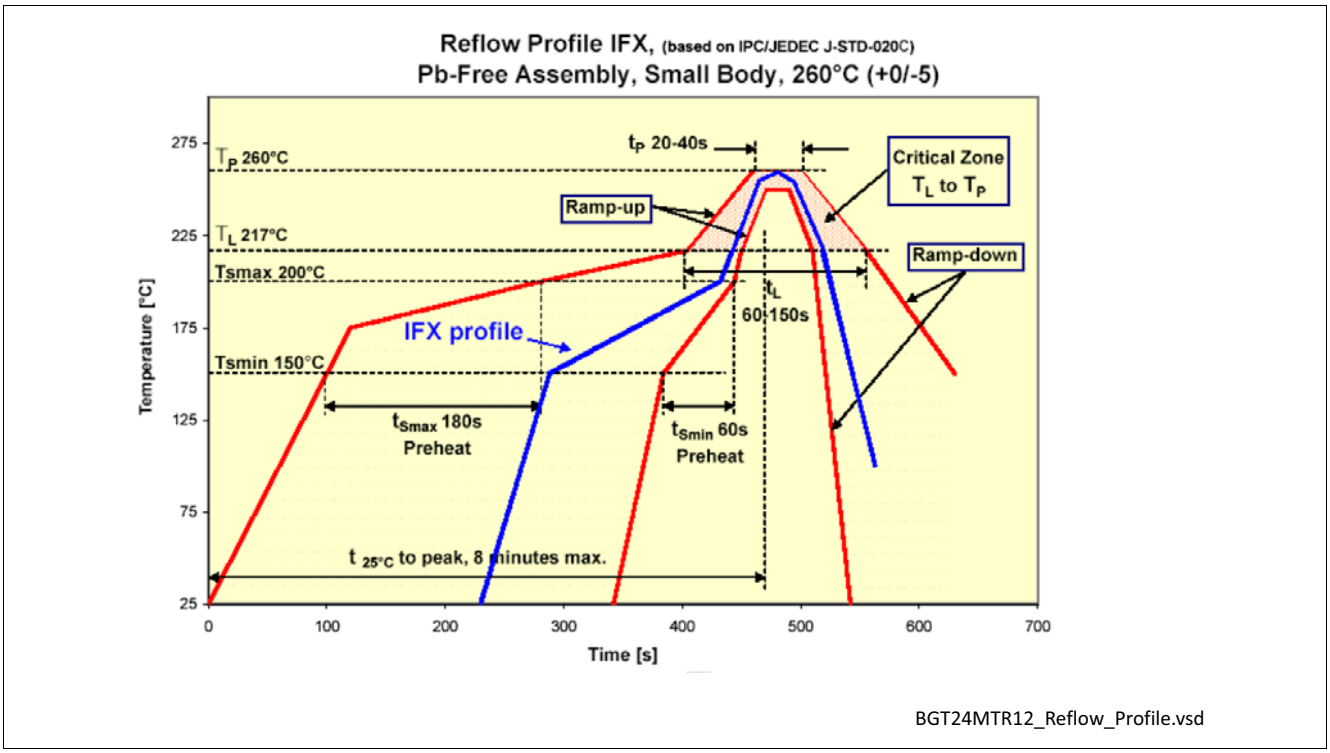

Figure 9 Reflow Profile for BGT24MTR12 (VQFN32-9)

4.3 Package Dimensions

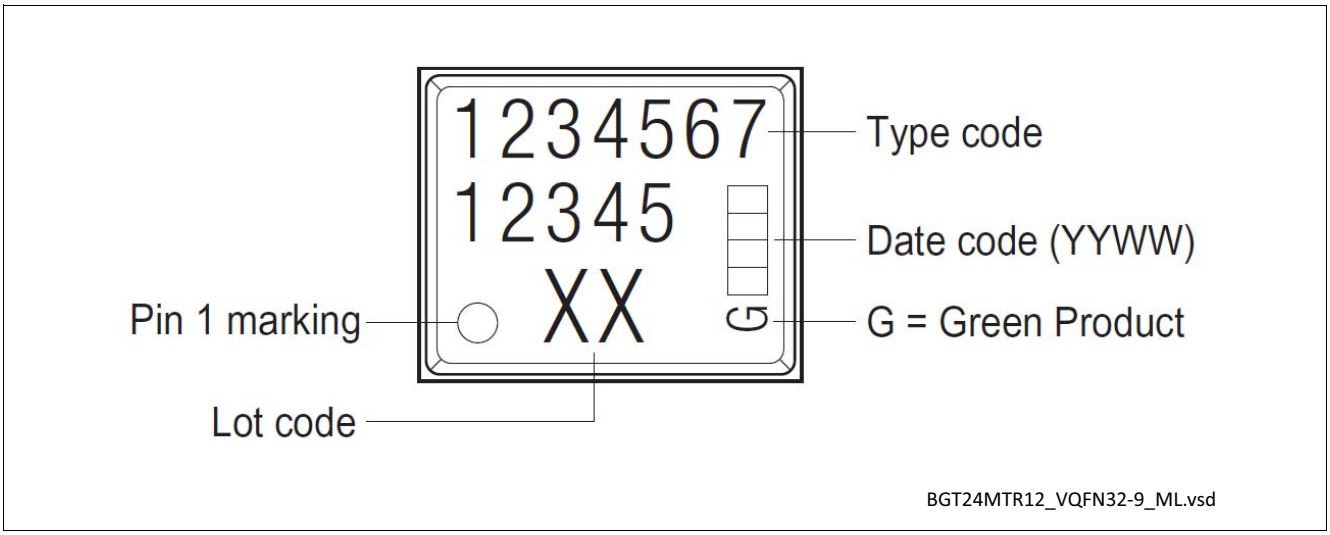

Figure 10 Marking Layout VQFN32-9

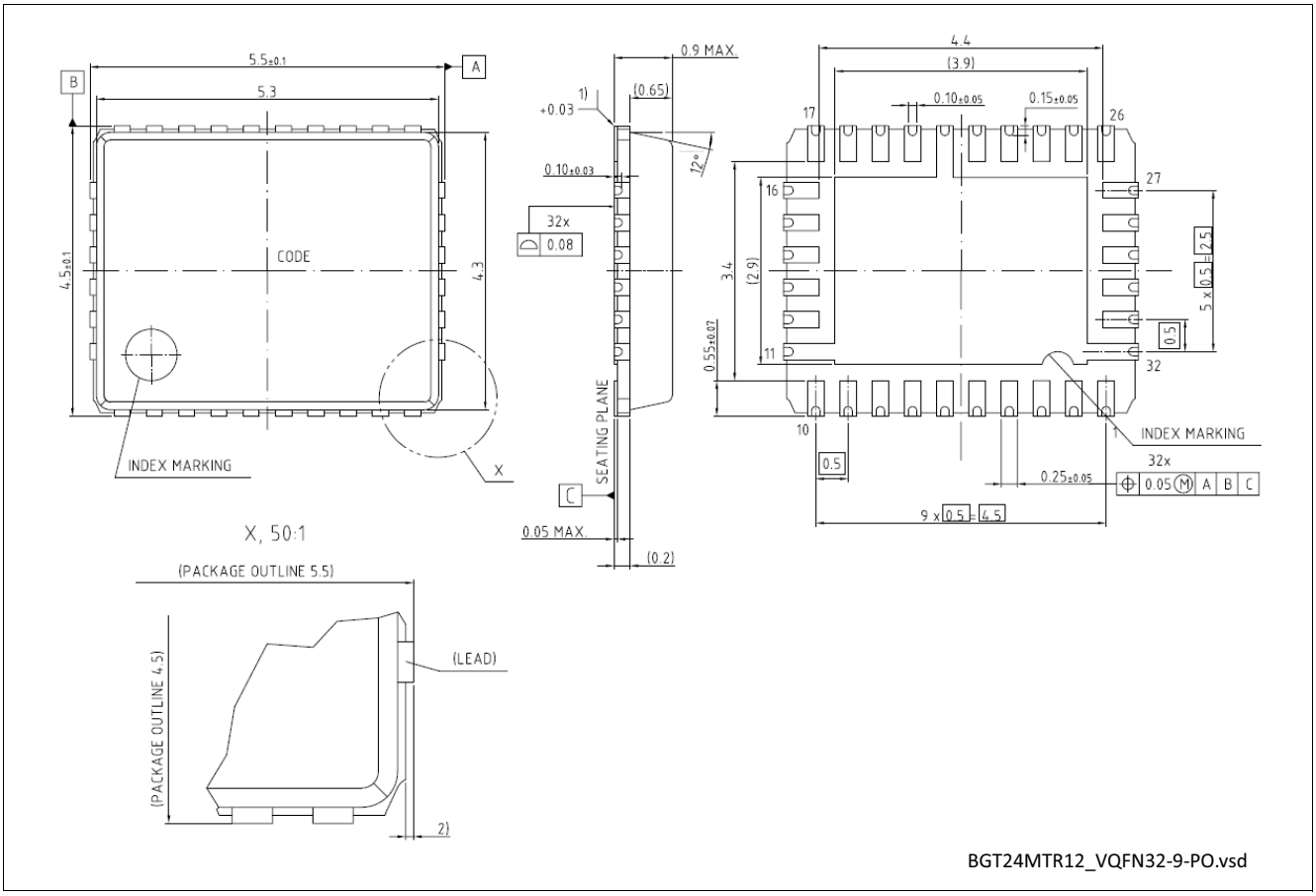

Figure 11 Package Outline (Top, Side and Bottom View)

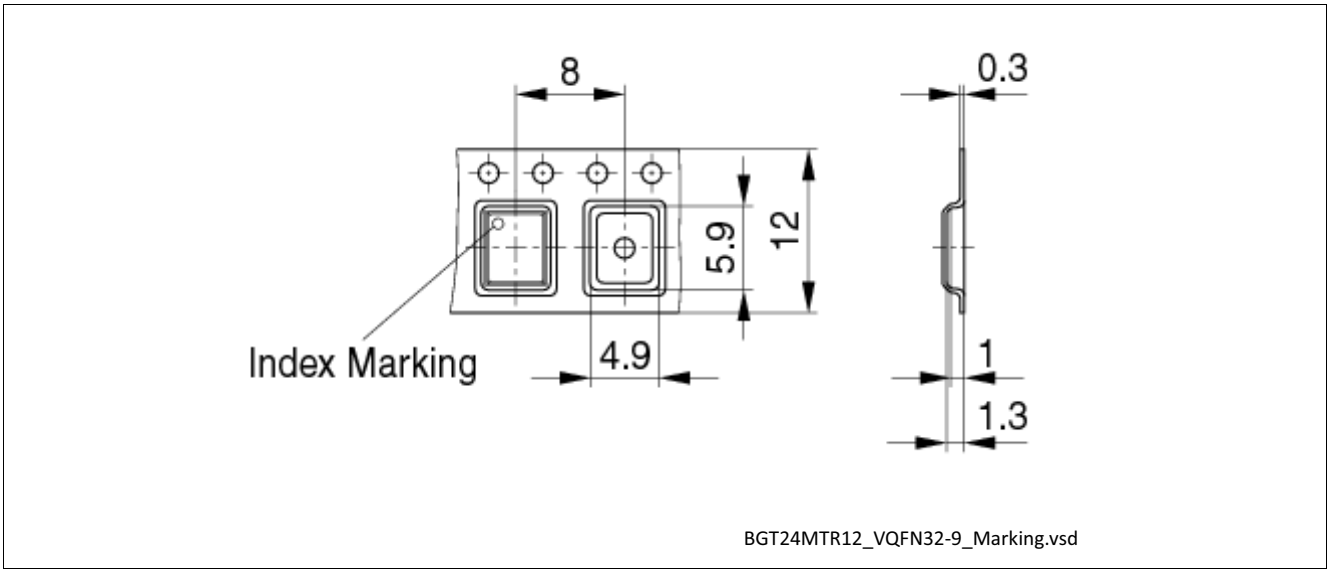

Figure 12 Tape of VQFN32-9

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