

4Mb Late Write LVTTTL High Speed Synchronous SRAM (128K x 36 Organization)

## Description

The CXK77B3641 is a high speed BiCMOS synchronous static RAM with common I/O pins, organized as 131,072-words by 36-bits. This synchronous SRAM integrates input registers, high speed RAM, output registers/latches, and a one-deep write buffer onto a single monolithic IC. Three different read protocols - Register-Register (R-R), Register-Latch (R-L), and Register-Flow Thru (R-FT), and an enhanced write protocol - Late (Delayed) Write (LW), are supported, providing a flexible, high-performance user interface.

All input signals except  $\overline{G}$  (Output Enable) and ZZ (Sleep Mode) are registered on the positive edge of K clock.

Read cycles can be controlled in one of three ways - with registered outputs in Register-Register mode, with latched outputs in Register-Latch mode, or with flow-through outputs in Register-Flow Thru mode. The read protocol is user-selectable through external mode pins M1 and M2.

Write cycles follow a Late Write protocol, where data is provided to the SRAM one clock cycle after the address and control signals, eliminating one dead cycle from Read-to-Write transitions. In this scheme, when a write cycle is initiated, the address and data stored in the SRAM's write buffer during the previous write cycle are directed to the SRAM's memory core, while, simultaneously, the address and data from the current write cycle are stored in the SRAM's write buffer. In both Register-Latch and Register-Flow Thru modes, when  $\overline{SW}$  (Global Write Enable) is driven active, the subsequent positive edge of K clock tristates the SRAM's output drivers immediately, allowing consecutive Read-Write-Read operations. The write cycle is internally self-timed, which eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

Sleep (power down) mode control is provided through the asynchronous ZZ input. 220 MHz operation is obtained from a single 3.3V power supply. JTAG boundary scan interface is provided using a subset of IEEE standard 1149.1 protocol.

## Features

	<u>R-R Mode</u>	<u>R-L, R-FT Modes</u>
• Fast Cycle/Access Time	$t_{KHKH} / t_{KHQV}$	$t_{KHKH} / t_{KHQV}$
CXK77B3641 -45	4.5ns / 2.4ns	5.5ns / 5.5ns
-5(*)	5.0ns / 2.5ns	5.7ns / 5.7ns
-6	6.0ns / 3.0ns	6.0ns / 6.0ns

Note (\*): Contact Sony Memory Marketing for availability of “-5” speed bin.

- 3 synchronous modes of operation, selectable by mode pins:  
Register-Register; Register-Latch; Register-Flow Thru;
- Single +3.3V power supply: 3.3V  $\pm$  5%
- Dedicated output supply voltage:  $V_{DDQ}$  (2.5V to 3.3V typical)
- Inputs and outputs are LVTTTL/LVCMOS compatible.
- Differential clock input (K/ $\overline{K}$ ). Clock levels are compatible to PECL, LVTTTL and LVCMOS.
- All inputs (except asynchronous  $\overline{G}$  and ZZ) and outputs are registered on a single clock edge.
- Byte Write capability.
- Late Write scheme to eliminate one dead cycle from Read-to-Write transitions.
- Self-timed write cycles.
- Sleep (power down) mode.
- JTAG boundary scan (subset of IEEE standard 1149.1).
- 119 pin (7x17) Plastic Ball Grid Array (PBGA) package.

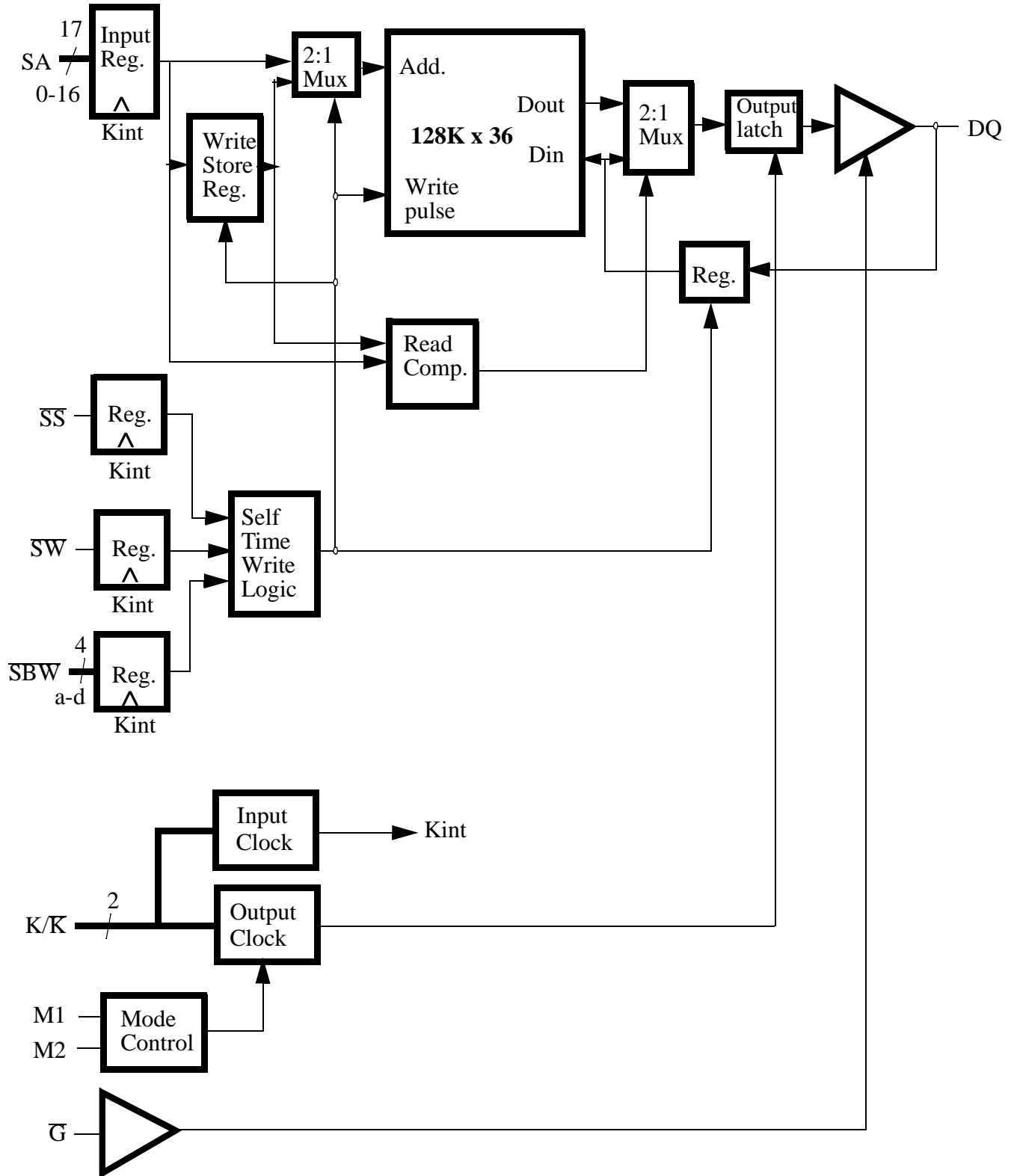
## Pin Configuration (Top View)

	1	2	3	4	5	6	7
A	V <sub>DDQ</sub>	SA6	SA7	NC	SA3	SA2	V <sub>DDQ</sub>
B	NC	NC	SA8	NC	SA4	NC	NC
C	NC	SA12	SA5	VDD	SA0	SA13	NC
D	DQ7c	DQ8c	V <sub>SS</sub>	NC	V <sub>SS</sub>	DQ8b	DQ7b
E	DQ5c	DQ6c	V <sub>SS</sub>	$\overline{SS}$	V <sub>SS</sub>	DQ6b	DQ5b
F	V <sub>DDQ</sub>	DQ4c	V <sub>SS</sub>	$\overline{G}$	V <sub>SS</sub>	DQ4b	V <sub>DDQ</sub>
G	DQ2c	DQ3c	$\overline{SBWc}$	$\overline{C}$	$\overline{SBWb}$	DQ3b	DQ2b
H	DQ0c	DQ1c	V <sub>SS</sub>	C	V <sub>SS</sub>	DQ1b	DQ0b
J	V <sub>DDQ</sub>	V <sub>DD</sub>	NC	V <sub>DD</sub>	NC	V <sub>DD</sub>	V <sub>DDQ</sub>
K	DQ0d	DQ1d	V <sub>SS</sub>	K	V <sub>SS</sub>	DQ1a	DQ0a
L	DQ2d	DQ3d	$\overline{SBWd}$	K	$\overline{SBWa}$	DQ3a	DQ2a
M	V <sub>DDQ</sub>	DQ4d	V <sub>SS</sub>	$\overline{SW}$	V <sub>SS</sub>	DQ4a	V <sub>DDQ</sub>
N	DQ5d	DQ6d	V <sub>SS</sub>	SA14	V <sub>SS</sub>	DQ6a	DQ5a
P	DQ7d	DQ8d	V <sub>SS</sub>	SA11	V <sub>SS</sub>	DQ8a	DQ7a
R	NC	SA10	M1	V <sub>DD</sub>	M2	SA15	NC
T	NC	NC	SA9	SA16	SA1	NC	ZZ
U	V <sub>DDQ</sub>	TMS	TDI	TCK	TDO	NC	V <sub>DDQ</sub>

## Pin Description

Symbol	Description	Symbol	Description	Symbol	Description
SA	Address Input (0-16)	$\overline{G}$	Async. Output Enable	V <sub>DDQ</sub>	Output Power Supply
DQ	Data I/O (0-8), Bytes a-d	ZZ	Async. Sleep Mode	V <sub>SS</sub>	Ground
K, $\overline{K}$	Differential Input Clocks	TCK	JTAG Clock (LVTTTL)	M1,M2	Mode Select
C, $\overline{C}$	Differential Output Control Clocks (for future use)	TMS	JTAG Mode Select (LVTTTL)	NC	No Connect
$\overline{SW}$	Write Enable, Global	TDI	JTAG Data In (LVTTTL)		
$\overline{SBWx}$	Write Enable, Bytes a-d	TDO	JTAG Data Out (LVTTTL)		
$\overline{SS}$	Synchronous Select	V <sub>DD</sub>	+3.3V Power Supply		

# BLOCK DIAGRAM



## •Truth Tables

**Register - Register Mode**

ZZ	SS (t <sub>n</sub> )	SW (t <sub>n</sub> )	SBW <sub>x</sub> (t <sub>n</sub> )	$\bar{G}$	Mode	DQ <sub>0-35</sub> (t <sub>n</sub> )	DQ <sub>0-35</sub> (t <sub>n+1</sub> )	V <sub>DD</sub> Current
H	X	X	X	X	Sleep Mode. Power Down	Hi - Z	Hi - Z	I <sub>SB</sub>
L	H	X	X	X	Deselect	X	Hi - Z	I <sub>DD</sub>
L	L	H	X	H	Read	Hi - Z	Hi - Z	I <sub>DD</sub>
L	L	H	X	L	Read	X	Q(t <sub>n</sub> )	I <sub>DD</sub>
L	L	L	L	X	Write All Bytes (Bits 0-35)	X	D(t <sub>n</sub> )	I <sub>DD</sub>
L	L	L	X	X	Write Bytes With SBW <sub>x</sub> =L	X	D(t <sub>n</sub> )	I <sub>DD</sub>
L	L	L	H	X	Abort Write	X	Hi - Z	I <sub>DD</sub>

**Register - Latch and Register - Flow Thru Mode**

ZZ	SS (t <sub>n</sub> )	SW (t <sub>n</sub> )	SBW <sub>x</sub> (t <sub>n</sub> )	$\bar{G}$	Mode	DQ <sub>0-35</sub> (t <sub>n</sub> )	DQ <sub>0-35</sub> (t <sub>n+1</sub> )	V <sub>DD</sub> Current
H	X	X	X	X	Sleep Mode. Power Down	Hi - Z	Hi - Z	I <sub>SB</sub>
L	H	X	X	X	Deselect	Hi - Z	X	I <sub>DD</sub>
L	L	H	X	H	Read	Hi - Z	Hi - Z	I <sub>DD</sub>
L	L	H	X	L	Read	Q(t <sub>n</sub> )	X	I <sub>DD</sub>
L	L	L	L	X	Write All Bytes (Bits 0-35)	Hi - Z	D(t <sub>n</sub> )	I <sub>DD</sub>
L	L	L	X	X	Write Bytes With SBW <sub>x</sub> =L	Hi - Z	D(t <sub>n</sub> )	I <sub>DD</sub>
L	L	L	H	X	Abort Write	Hi - Z	X	I <sub>DD</sub>

### •Mode Select

This device supports three different JEDEC standard read protocols via mode pins M1 and M2. The mode pins must be set during power-up and cannot change during SRAM operation.

**Mode Select Truth Table.**

	M1	M2
Register-Register	L	H
Register-Flow Thru	L	L
Register-Latch	H	L

### •Power-Up Sequence

Power supplies must power up in the following sequence:  $V_{SS}$ ,  $V_{DD}$ ,  $V_{DDQ}$ , and Inputs.  $V_{DDQ}$  must never exceed  $V_{DD}$ .

### •Absolute Maximum Ratings<sup>(1)</sup>

Item	Symbol	Rating	Unit
Supply Voltage	$V_{DD}$	-0.5 to +4.6	V
Output Supply Voltage	$V_{DDQ}$	-0.5 to +4.6	V
Input Voltage	$V_{IN}$	-0.5 to $V_{DD}+0.5$ (4.6V max.)	V
Output Voltage	$V_{OUT}$	-0.5 to $V_{DDQ}+0.5$ (4.6V max.)	V
Operating Temperature	$T_A$	0 to 70	°C
Junction Temperature	$T_J$	0 to 110	°C
Storage Temperature	$T_{stg}$	-55 to 150	°C

<sup>(1)</sup>Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions other than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## • DC Recommended Operating Conditions

(V<sub>SS</sub> = 0V, T<sub>A</sub> = 0 to 70°C)

Item		Symbol	Min	Typ	Max	Unit	
Supply Voltage		V <sub>DD</sub>	3.13	3.3	3.47	V	
Output Supply Voltage <sup>(1)</sup>		V <sub>DDQ</sub>	2.37	2.5, 3.3	3.47	V	
Address & Control	Input High Voltage <sup>(2)</sup>	V <sub>IHCA</sub>	1.65	---	V <sub>DD</sub> + 0.3	V	
	Input Low Voltage <sup>(4)</sup>	V <sub>ILCA</sub>	-0.3	---	1.15	V	
Data	Input High Voltage <sup>(3)</sup>	V <sub>IHD</sub>	1.65	---	V <sub>DDQ</sub> + 0.3	V	
	Input Low Voltage <sup>(4)</sup>	V <sub>ILD</sub>	-0.3	---	1.15	V	
Clock <sup>(5)</sup>	LVTTTL	Input Signal Voltage	V <sub>KIN</sub>	-0.3	---	V <sub>DD</sub> + 0.3	V
		Input Differential Voltage	V <sub>DIF</sub>	0.5	---	V <sub>DD</sub> + 0.6	V
		Input Common Mode Voltage	V <sub>CM</sub>	1.15	1.4	1.75	V
		Input Cross Point Voltage	V <sub>X</sub>	1.15	1.4	1.75	V
	PECL	Input High Voltage	V <sub>IH-PECL</sub>	2.135	---	2.420	V
		Input Low Voltage	V <sub>IL-PECL</sub>	1.480	---	1.825	V

(1) For V<sub>DDQ</sub> = 2.5V or V<sub>DDQ</sub> = 3.3V application.

(2) V<sub>IH</sub> (Max) AC = V<sub>DD</sub> + 1.5 V for pulse width less than 2.0 ns

(3) V<sub>IH</sub> (Max) AC = V<sub>DDQ</sub> + 1.5 V for pulse width less than 2.0 ns

(4) V<sub>IL</sub> (Min) AC = -1.5 V for pulse width less than 2.0 ns.

(5) This device supports three different input clocking schemes:

- a. LVTTTL Differential - In this scheme, both clock inputs (K and  $\bar{K}$ ) are driven differentially to the same voltage levels as the other inputs, i.e. from V<sub>SS</sub> to V<sub>DDQ</sub> nominally. V<sub>KIN</sub>, V<sub>DIF</sub> and V<sub>CM</sub> must all be considered when using this scheme.
- b. LVTTTL Single Ended - In this scheme, one of the two clock inputs (either K or  $\bar{K}$ ) is driven to the same voltage levels as the other inputs, i.e. from V<sub>SS</sub> to V<sub>DDQ</sub> nominally, while the other clock input (either  $\bar{K}$  or K) is tied to an external reference voltage (V<sub>X</sub>). V<sub>KIN</sub>, V<sub>DIF</sub> and V<sub>X</sub> must all be considered when using this scheme.
- c. PECL Differential - In this scheme, both clock inputs (K and  $\bar{K}$ ) are driven differentially according to PECL guidelines. Both V<sub>IH-PECL</sub> and V<sub>IL-PECL</sub> must be considered when using this scheme.

## • I/O Capacitance

(T<sub>A</sub> = 25°C, f = 1 MHz)

Item	Symbol	Test conditions	Min	Max	Unit
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0V	---	6	pF
Clock Input Capacitance	C <sub>CLK</sub>	V <sub>IN</sub> = 0V	---	6	pF
Output Capacitance	C <sub>OUT</sub>	V <sub>OUT</sub> = 0V	---	7	pF

Note: These parameters are sampled and are not 100% tested.

## •DC Electrical Characteristics

 $(V_{DD} = 3.3V \pm 5\%, V_{SS} = 0V, T_A = 0 \text{ to } 70^\circ\text{C})$ 

Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Leakage Current	$I_{LI}$	$V_{IN} = V_{SS} \text{ to } V_{DD}$	-1	---	1	$\mu\text{A}$
Output Leakage Current	$I_{LO}$	$V_{OUT} = V_{SS} \text{ to } V_{DD}$ $\bar{G} = V_{IH}$	-10	---	10	$\mu\text{A}$
Power Supply Operating Current	$I_{DD}^1$	Cycle = 6.0ns Duty = 100% $I_{OUT} = 0 \text{ mA}$	---	665	---	mA
Power Supply Operating Current	$I_{DD}^1$	Cycle = 5.5ns Duty = 100% $I_{OUT} = 0 \text{ mA}$	---	695	---	mA
Power Supply Operating Current	$I_{DD}^1$	Cycle = 4.5ns Duty = 100% $I_{OUT} = 0 \text{ mA}$	---	755	---	mA
Power Supply Standby Current	$I_{SB}$	$ZZ \geq V_{IH}$	---	60	---	mA
Output High Voltage $V_{DDQ} = 3.3V$	$V_{OH}$	$I_{OH} = -6.0 \text{ mA}$	2.4	---	---	V
Output Low Voltage $V_{DDQ} = 3.3V$	$V_{OL}$	$I_{OL} = 6.0 \text{ mA}$	---	---	0.4	V
Output High Voltage for $V_{DDQ} = 2.5V$	$V_{OH}$	$I_{OH} = -6.0 \text{ mA}$	2.0	---	---	V
Output Low Voltage for $V_{DDQ} = 2.5V$	$V_{OL}$	$I_{OL} = 6.0 \text{ mA}$	---	---	0.4	V

1. Typical  $I_{DD}$  values measured at  $V_{DD} = 3.3V$  and  $T_A = 25^\circ\text{C}$ , with a 75% read / 25% write operation distribution.

## •AC Electrical Characteristics (Register-Register Mode)

Item	Symbol	-45		-5		-6		Unit
		Min	Max	Min	Max	Min	Max	
Cycle Time	$t_{\text{KHKH}}$	4.5	---	5.0	---	6.0	---	ns
Clock High Pulse Width	$t_{\text{KHKL}}$	1.5	---	1.5	---	2.0	---	ns
Clock Low Pulse Width	$t_{\text{KLKH}}$	1.5	---	1.5	---	2.0	---	ns
Address Setup Time	$t_{\text{AVKH}}$	0.5	---	0.5	---	0.5	---	ns
Address Hold Time	$t_{\text{KHAX}}$	1.0	---	1.0	---	1.0	---	ns
Write Enables Setup Time	$t_{\text{WVKH}}$	0.5	---	0.5	---	0.5	---	ns
Write Enables Hold Time	$t_{\text{KH WX}}$	1.0	---	1.0	---	1.0	---	ns
Synchronous Select Setup Time	$t_{\text{SVKH}}$	0.5	---	0.5	---	0.5	---	ns
Synchronous Select Hold Time	$t_{\text{KHSX}}$	1.0	---	1.0	---	1.0	---	ns
Data Input Setup Time	$t_{\text{DVKH}}$	0.5	---	0.5	---	0.5	---	ns
Data Input Hold Time	$t_{\text{KHDX}}$	1.0	---	1.0	---	1.0	---	ns
Clock High to Output Valid	$t_{\text{KHQV}}$	---	2.4	---	2.5	---	3.0	ns
Clock High to Output Hold	$t_{\text{KHQX}}^{*2}$	0.7	---	0.7	---	0.7	---	ns
Clock High to Output Low-Z	$t_{\text{KHQX1}}^{*2}$	0.7	---	0.7	---	0.7	---	ns
Clock High to Output High-Z (SS Deselect Cycle)	$t_{\text{KHQZ}}^{*2}$	---	2.0	---	2.0	---	2.0	ns
Output Enable Low to Output Valid	$t_{\text{GLQV}}$	---	2.3	---	2.5	---	3.0	ns
Output Enable Low to Output Low-Z	$t_{\text{GLQX}}^{*2}$	0.5	---	0.5	---	0.5	---	ns
Output Enable High to Output High-Z	$t_{\text{GHQZ}}^{*2}$	---	2.3	---	2.5	---	3.0	ns
Sleep Mode Enable Time	$t_{\text{ZZE}}^{*2}$	---	20.0	---	20.0	---	20.0	ns
Sleep Mode Recovery Time	$t_{\text{ZZR}}^{*2}$	20.0	---	20.0	---	20.0		ns

1. All parameters are specified over the range  $T_A = 0$  to  $70^\circ\text{C}$ .
2. These parameters are sampled and are not 100% tested.



## •AC Electrical Characteristics (Register-Latch &amp; Register-Flow Thru Modes)

Item	Symbol	-45		-5		-6		Unit
		Min	Max	Min	Max	Min	Max	
Cycle Time	$t_{KHKH}$	5.5	---	5.7	---	6.0	---	ns
Clock High Pulse Width	$t_{KHKL}$	1.5	---	1.5	---	2.0	---	ns
Clock Low Pulse Width	$t_{KLKH}$	1.5	---	1.5	---	2.0	---	ns
Address Setup Time	$t_{AVKH}$	0.5	---	0.5	---	0.5	---	ns
Address Hold Time	$t_{KHAX}$	1.0	---	1.0	---	1.0	---	ns
Write Enables Setup Time	$t_{WVKH}$	0.5	---	0.5	---	0.5	---	ns
Write Enables Hold Time	$t_{KH WX}$	1.0	---	1.0	---	1.0	---	ns
Synchronous Select Setup Time	$t_{SVKH}$	0.5	---	0.5	---	0.5	---	ns
Synchronous Select Hold Time	$t_{KHSX}$	1.0	---	1.0	---	1.0	---	ns
Data Input Setup Time	$t_{DVKH}$	0.5	---	0.5	---	0.5	---	ns
Data Input Hold Time	$t_{KHDX}$	1.0	---	1.0	---	1.0	---	ns
Clock High to Output Valid	$t_{KHQV}$	---	5.5	---	5.7	---	6.0	ns
Clock High to Output Hold (Flow Thru mode only)	$t_{KHQX}^{*2}$	2.0	---	2.0	---	2.0	---	ns
Clock High to Output Low-Z (Flow Thru mode only)	$t_{KHQX1}^{*2}$	2.0	---	2.0	---	3.0	---	ns
Clock Low to Output Valid (Latch mode only)	$t_{KLQV}$	---	2.3	---	2.5	---	2.5	ns
Clock Low to Output Hold (Latch mode only)	$t_{KLQX}^{*2}$	0.7	---	0.7	---	0.7	---	ns
Clock Low to Output Low-Z (Latch mode only)	$t_{KLQX1}^{*2}$	0.7	---	0.7	---	0.7	---	ns
Clock High to Output High-Z (SS Deselect Cycle)	$t_{KHQZ}^{*2}$	---	2.0	---	2.0	---	2.0	ns
Clock High to Output High-Z (SW Write Cycle)	$t_{KHQZ1}^{*2}$	---	2.0	---	2.0	---	2.0	ns
Output Enable Low to Output Valid	$t_{GLQV}$	---	2.3	---	2.5	---	2.5	ns
Output Enable Low to Output Low-Z	$t_{GLQX}^{*2}$	0.5	---	0.5	---	0.5	---	ns
Output Enable High to Output High-Z	$t_{GHQZ}^{*2}$	---	2.3	---	2.5	---	2.5	ns
Sleep Mode Enable Time	$t_{ZZE}^{*2}$	---	20.0	---	20.0	---	20.0	ns
Sleep Mode Recovery Time	$t_{ZZR}^{*2}$	20.0	---	20.0	---	20.0		ns

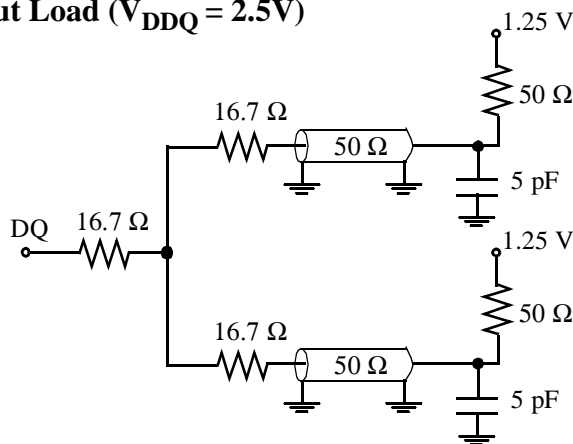
1. All parameters are specified over the range  $T_A = 0$  to  $70^\circ\text{C}$ .
2. These parameters are sampled and are not 100% tested.

•AC Test Conditions ( $V_{DDQ} = 2.5V$ )

( $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDQ} = 2.5V -5\%/+10\%$ ,  $T_A = 0$  to  $70^\circ C$ )

Item		Conditions	Notes
Address / Control / Data Input High Level		$V_{IHCA}, V_{IHD} = 2.0V$	@ Set up time $\geq 1ns$
Address / Control / Data Input Low Level		$V_{ILCA}, V_{ILD} = 0.8V$	@ Set up time $\geq 1ns$
Input Rise & Fall Time		1.0V/ns	Other than Clock
Input Reference Level		1.4V	Other than Clock
Clock	LVTTL Input High Voltage	2.2V	$V_{DIF} \geq 0.8V$
	LVTTL Input Low Voltage	0.6V	$V_{DIF} \geq 0.8V$
	LVTTL Input Common Mode Voltage	1.4V	
	PECL Input High Voltage	$V_{IH-PECL} = 2.3V$	
	PECL Input Low Voltage	$V_{IL-PECL} = 1.6V$	
Clock Input Rise & Fall Time		1.0V/ns	
Clock Input Reference Level		K/ $\bar{K}$ cross	
Output Reference Level		1.25V	
Output Load Conditions			Fig.1

Fig. 1: AC Test Output Load ( $V_{DDQ} = 2.5V$ )

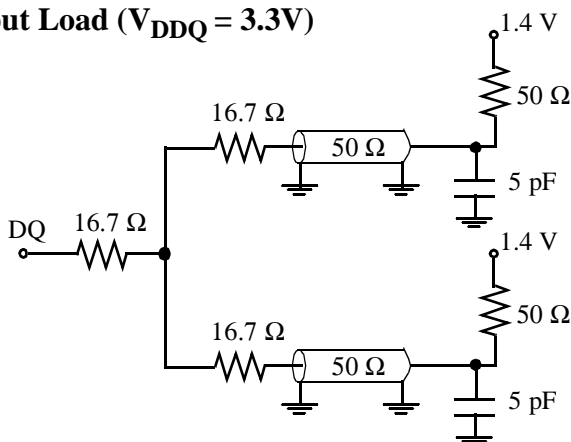


•AC Test Conditions ( $V_{DDQ} = 3.3V$ )

( $V_{DD} = V_{DDQ} = 3.3V \pm 5\%$ ,  $T_A = 0$  to  $70^\circ C$ )

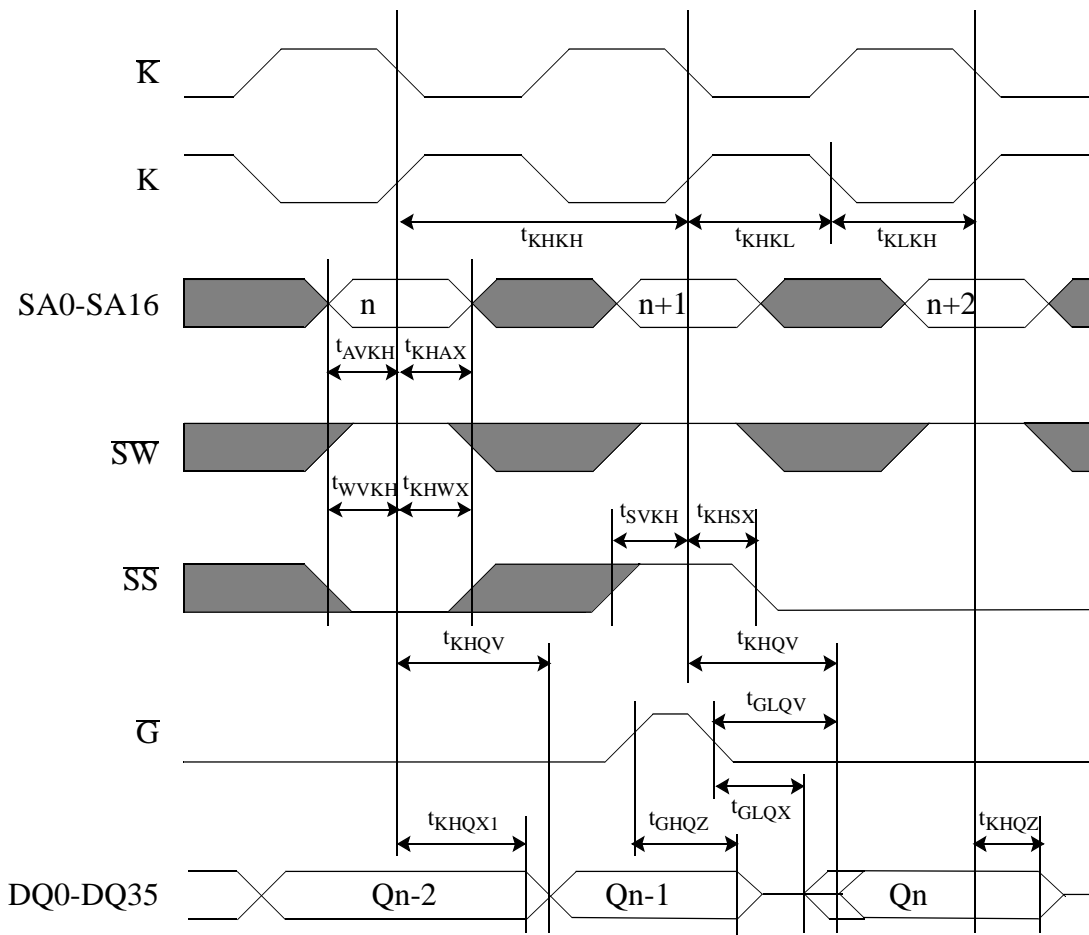
Item		Conditions	Notes
Address / Control / Data Input High Level		$V_{IHCA}, V_{IHD} = 2.4V$	@ Set up time $\geq 1ns$
Address / Control / Data Input Low Level		$V_{ILCA}, V_{ILD} = 0.4V$	@ Set up time $\geq 1ns$
Input Rise & Fall Time		1.0V/ns	Other than Clock
Input Reference Level		1.4V	Other than Clock
Clock	LVTTL Input High Voltage	2.4V	$V_{DIF} \geq 1.0V$
	LVTTL Input Low Voltage	0.4V	$V_{DIF} \geq 1.0V$
	LVTTL Input Common Mode Voltage	1.4V	
	PECL Input High Voltage	$V_{IH-PECL} = 2.3V$	
	PECL Input Low Voltage	$V_{IL-PECL} = 1.6V$	
Clock Input Rise & Fall Time		1.0V/ns	
Clock Input Reference Level		K/ $\bar{K}$ cross	
Output Reference Level		1.4V	
Output Load Conditions			Fig.2

Fig. 2: AC Test Output Load ( $V_{DDQ} = 3.3V$ )

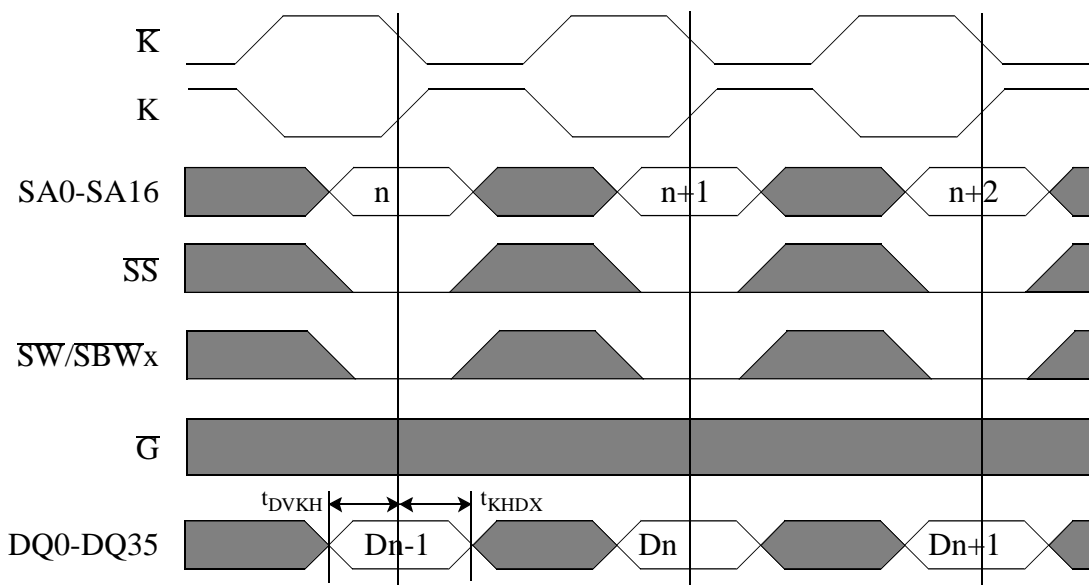


**Register - Register Mode**

**TIMING WAVEFORM OF READ CYCLE**

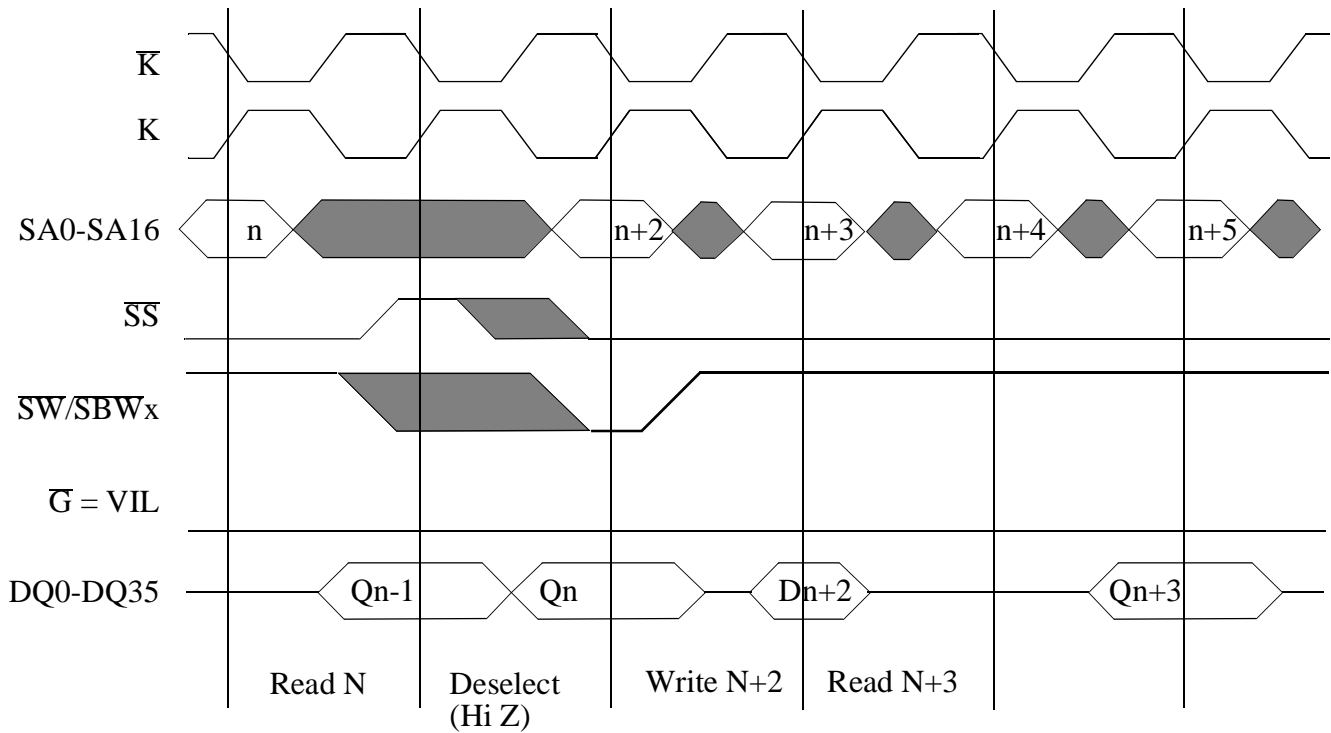


**TIMING WAVEFORM OF WRITE CYCLE**

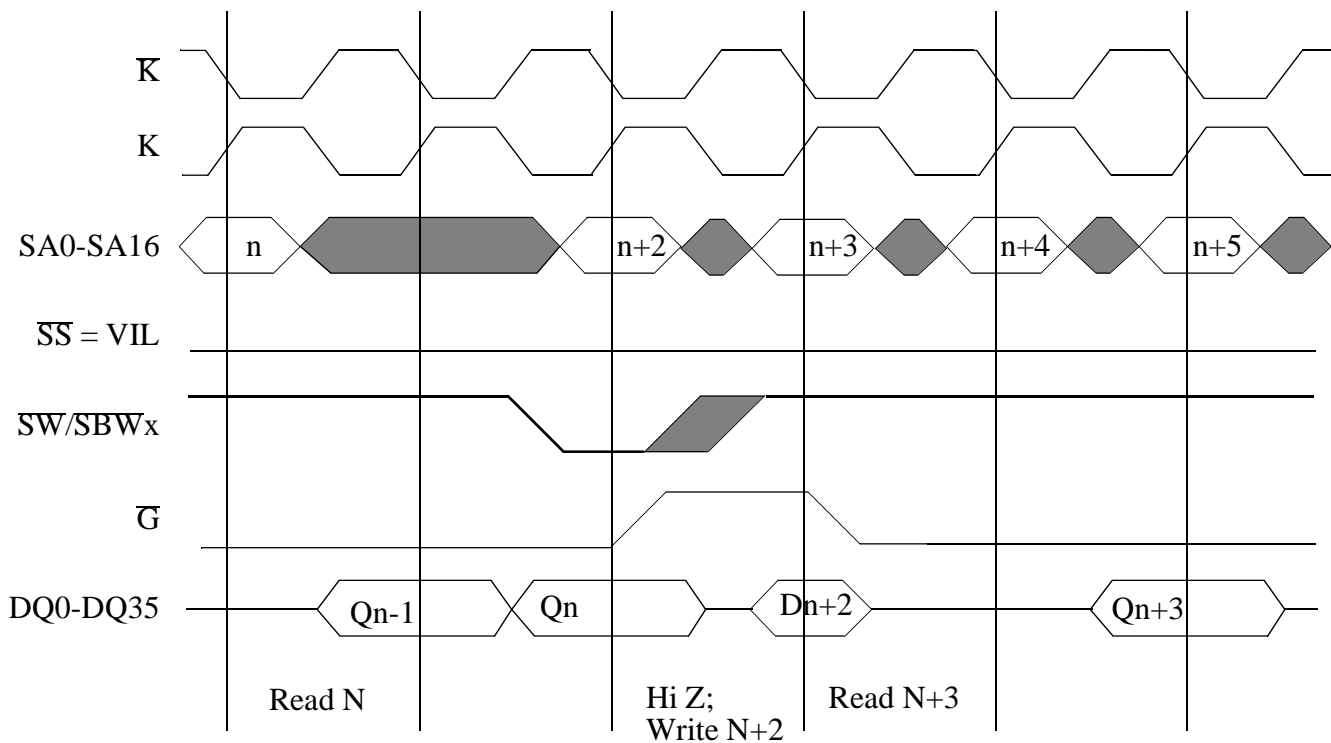


**Register - Register Mode**

**TIMING WAVEFORM OF READ-WRITE-READ CYCLE I (SS controlled)**

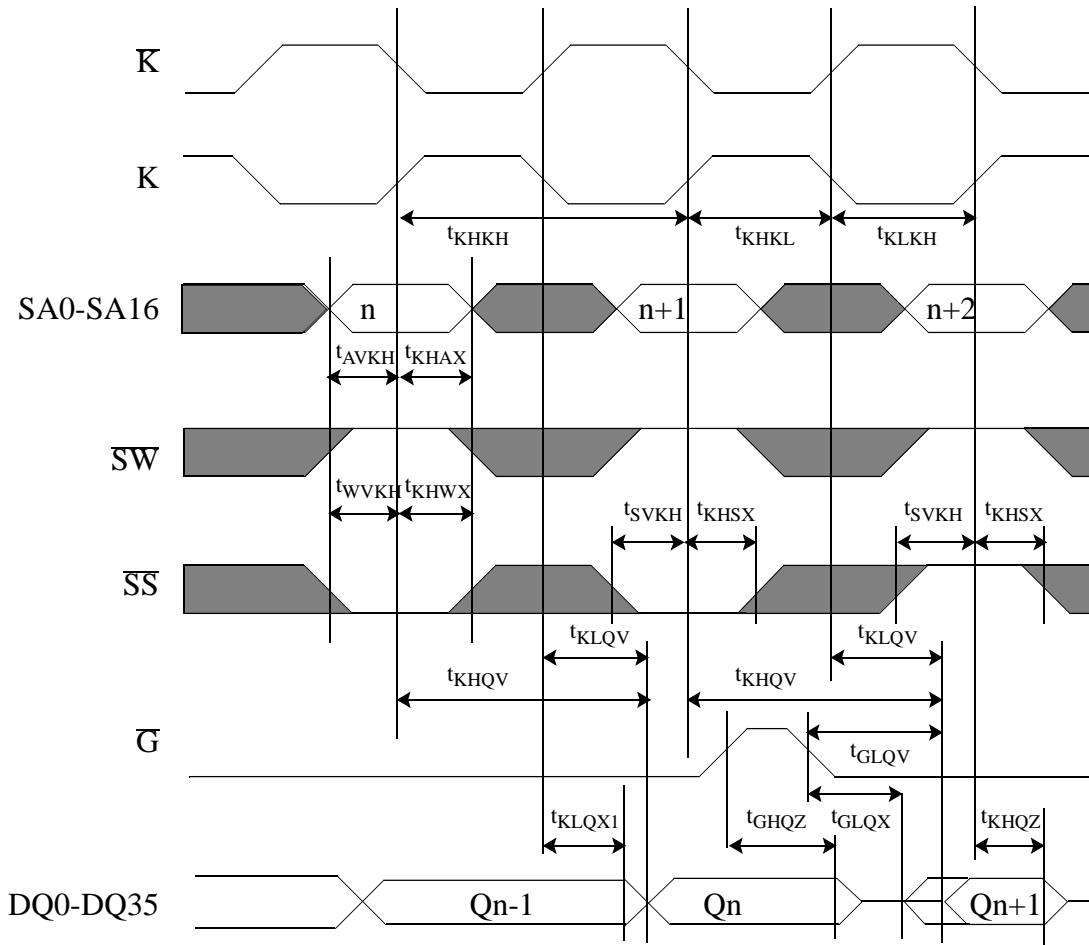


**TIMING WAVEFORM OF READ-WRITE-READ CYCLE II ( $\bar{G}$  controlled)**

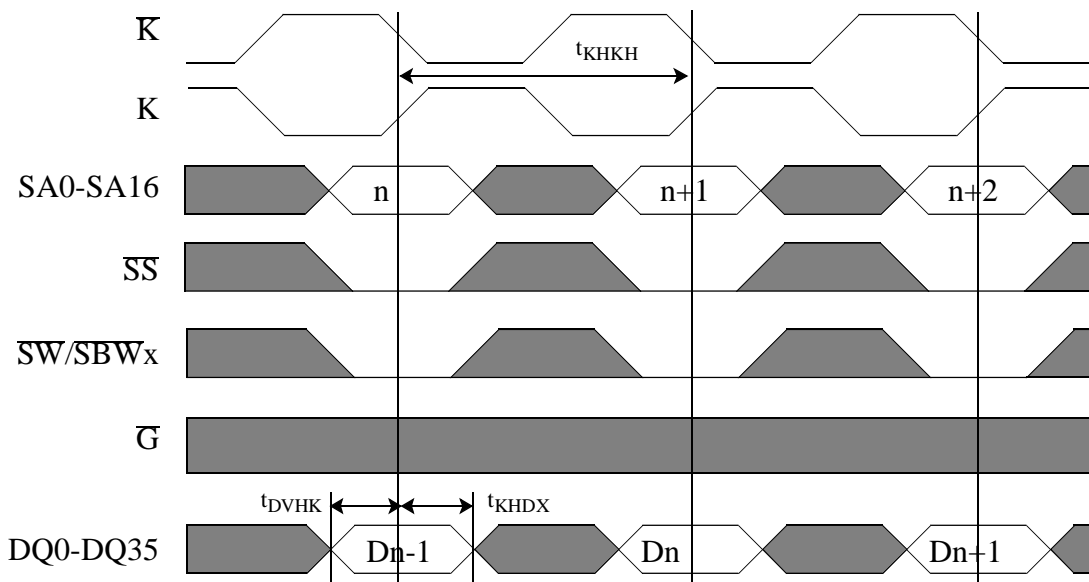


**Register - Latch Mode**

**TIMING WAVEFORM OF READ CYCLE**

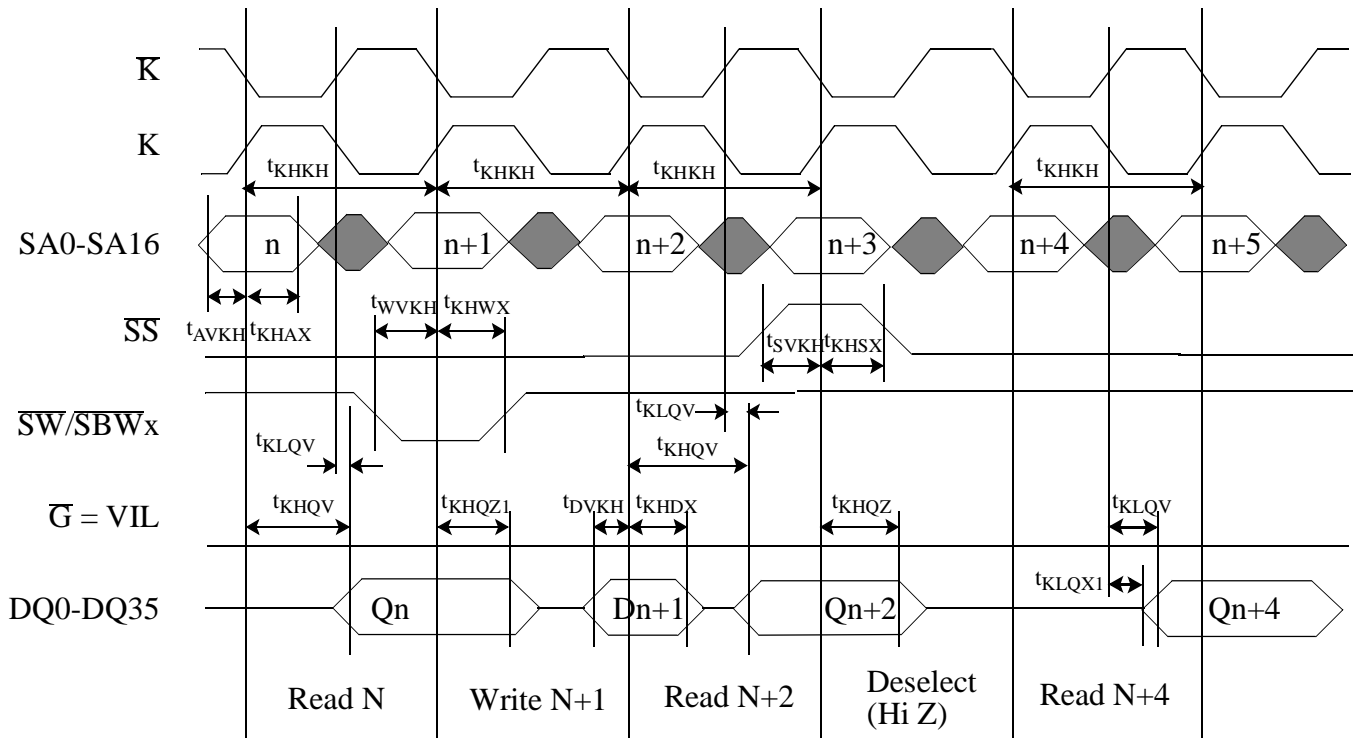


**TIMING WAVEFORM OF WRITE CYCLE**



**Register - Latch Mode**

**TIMING WAVEFORM OF READ-WRITE-READ CYCLE**

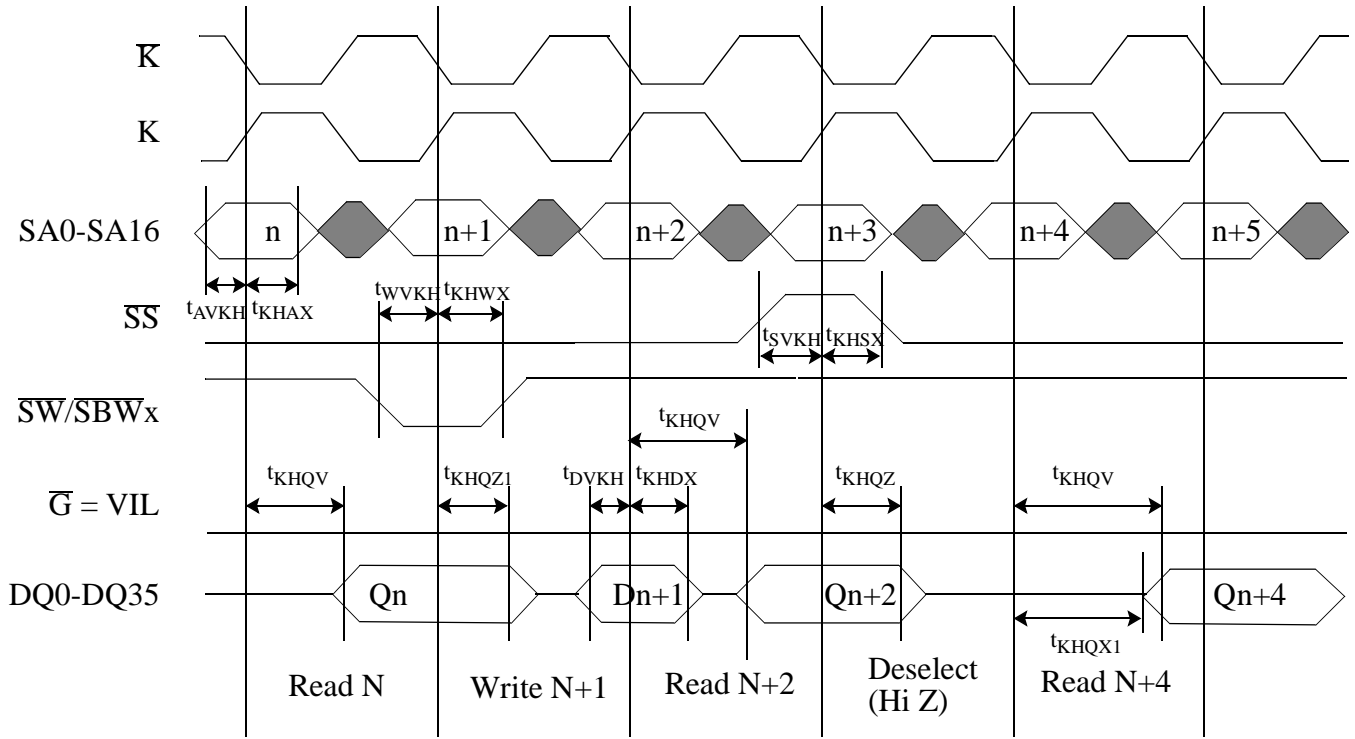






**Register - Flow Thru Mode**

**TIMING WAVEFORM OF READ-WRITE-READ CYCLE**



## Test Mode Description

### Functional Description

The CXK77B3641 provides a JTAG boundary scan interface using a limited set of IEEE std. 1149.1 functions. The test mode is intended to provide a mechanism for testing the interconnect between master (processor, controller, etc.), SRAMs, other components and the printed circuit board.

In conformance with a subset of IEEE std. 1149.1, the CXK77B3641 contains a TAP controller, Instruction register, Boundary scan register and Bypass register.

JTAG Inputs/Outputs are LVTTTL compatible only.

### Test Access Port (TAP)

4 pins as defined in the Pin Description table are used to perform JTAG functions. The TDI input pin is used to scan test data serially into one of three registers (Instruction register, Boundary Scan register and Bypass register). TDO is the output pin used to scan test data serially out. The TDI pin sends the data into LSB of the selected register and the MSB of the selected register feeds the data to TDO. The TMS input pin controls the state transition of 16 state TAP controller as specified in IEEE std. 1149.1. Inputs on TDI and TMS are registered on the rising edge of TCK clock. The output data on TDO is presented on the falling edge of TCK. TDO driver is in active state only when TAP controller is in Shift-IR state or in Shift-DR state.

TCK, TMS, TDI must be tied low when JTAG is not used.

### TAP Controller

16 state controller is implemented as specified in IEEE std. 1149.1.

The controller enters reset state in one of two ways:

1. Power up.
2. Apply a logic 1 on TMS input pin on 5 consecutive TCK rising edges.

### Instruction Register (3 bits)

The JTAG Instruction register consists of a shift register stage and parallel output latch. The register is 3 bits wide and is encoded as follow:

<u>Octal</u>	<u>MSB.....LSB</u>			<u>Instruction</u>
0	0	0	0	Bypass
1	0	0	1	IDCODE. Read device ID
2	0	1	0	Sample-Z. Sample Inputs and tri-state DQs
3	0	1	1	Bypass
4	1	0	0	Sample. Sample Inputs.
5	1	0	1	Private. Manufacturer use only.
6	1	1	0	Bypass
7	1	1	1	Bypass

**Bypass Register (1 bit)**

The Bypass Register is one bit wide and is connected electrically between TDI and TDO and provides the minimum length serial path between TDI and TDO.

**ID Registers (32 bits)**

The ID Register is 32 bits wide and is encoded as follows:

	ID[0}	1
Sony ID	ID[11:1]	0000 1110 001
Part Number	ID[27:12]	0000 0000 0001 1001
Revision Number	ID[31:28]	xxxx

**Boundary Scan Register (70 bits)**

The Boundary Scan Registers are 70 bits wide and are listed as follows:

DQ	36
SA	17
SW, SBW <sub>x</sub>	5
SS, $\bar{G}$	2
K, $\bar{K}$ , C, $\bar{C}$	4
ZZ	1
M1, M2	2
Place Holder	2
TNC	1

$K/\bar{K}$ ,  $C/\bar{C}$  inputs are sampled through one differential stage and internally inverted to generate internal  $K/\bar{K}$ ,  $C/\bar{C}$  signals for scan registers. Place Holder are required for some NC pins to maintain 70 bits Scan Register for different types of the same family SRAM and for density upgrades. All Place Holder Registers are connected to  $V_{SS}$  internally regardless of pin connection externally. TNC register is True No Connect i.e. not connected internally. TNC register information should be ignored during BSCAN testing.

**Scan Order (Order by exit sequence)**

36	3B	SA		SA	5B	35
37	-	V <sub>SS</sub>		V <sub>SS</sub>	-	34
38	3A	SA		SA	5A	33
39	3C	SA		SA	5C	32
40	2C	SA		SA	6C	31
41	2A	SA		SA	6A	30
42	2D	DQc		DQb	6D	29
43	1D	DQc		DQb	7D	28
44	2E	DQc		DQb	6E	27
45	1E	DQc		DQb	7E	26
46	2F	DQc		DQb	6F	25
47	2G	DQc		DQb	6G	24
48	1G	DQc		DQb	7G	23
49	2H	DQc		DQb	6H	22
50	1H	DQc		DQb	7H	21
51	3G	$\overline{\text{SBWc}}$		$\overline{\text{SBWb}}$	5G	20
52	4D	TNC(*)		$\overline{\text{C}}$	4F	19
53	4E	$\overline{\text{SS}}$		K	4K	18
54	4G	$\overline{\text{C}}$		K	4L	17
55	4H	C		$\overline{\text{SBWa}}$	5L	16
56	4M	$\overline{\text{SW}}$		DQa	7K	15
57	3L	$\overline{\text{SBWd}}$		DQa	6K	14
58	1K	DQd		DQa	7L	13
59	2K	DQd		DQa	6L	12
60	1L	DQd		DQa	6M	11
61	2L	DQd		DQa	7N	10
62	2M	DQd		DQa	6N	9
63	1N	DQd		DQa	7P	8
64	2N	DQd		DQa	6P	7
65	1P	DQd		ZZ	7T	6
66	2P	DQd		SA	5T	5
67	3T	SA		SA	6R	4
68	2R	SA		SA	4T	3
69	4N	SA		SA	4P	2
70	3R	M1		M2	5R	1

(\*) TNC means that the voltage polarity of this bit should be ignored during boundary scan testing.

**Ordering Information.**

Part Number	Speed	
	Register - Register	Register - Latch/ Register - Flow Thru
CXK77B3641GB-45	4.5ns Cycle / 2.4ns Access	5.5ns Cycle / 5.5ns Access
CXK77B3641GB-5 (*)	5.0ns Cycle / 2.5ns Access	5.7ns Cycle / 5.7ns Access
CXK77B3641GB-6	6.0ns Cycle / 3.0ns Access	6.0ns Cycle / 6.0ns Access

Note (\*): Contact Sony Memory Marketing for availability of “-5” speed bin.

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**Revision History**

Rev. #	Rev. date	Changes / Modifications to Data-Sheet									
rev 4.0	8/22/97	Initial version, based on TS-2 evaluation									
rev 4.2 (Unreleased)	11/21/97	<p>Modified AC Electrical Characteristics: R-L, R-FT Modes:</p> <table> <tr> <td>-6</td> <td><math>T_{KLQV}</math>, <math>T_{GLQV}</math>, <math>T_{GHQZ}</math></td> <td>3.0ns to 2.5ns</td> </tr> <tr> <td></td> <td><math>T_{KHQZ}</math>, <math>T_{KHQZ1}</math></td> <td>3.0ns to 2.0ns</td> </tr> <tr> <td></td> <td><math>T_{KHQX1}</math></td> <td>2.0ns to 3.0ns</td> </tr> </table> <p>Renamed “-4.5” bin to “-45” bin in all modes. Renamed “-5” bin to “-50” bin in all modes. Renamed “-6” bin to “-60” bin in all modes. Added “-65” bin to all modes.</p> <p>Provided IDD &amp; ISB typical values (page-7) Provided PECL DC electrical characteristic (page-6) Provided PECL AC test conditions (page-10, -11)</p>	-6	$T_{KLQV}$ , $T_{GLQV}$ , $T_{GHQZ}$	3.0ns to 2.5ns		$T_{KHQZ}$ , $T_{KHQZ1}$	3.0ns to 2.0ns		$T_{KHQX1}$	2.0ns to 3.0ns
-6	$T_{KLQV}$ , $T_{GLQV}$ , $T_{GHQZ}$	3.0ns to 2.5ns									
	$T_{KHQZ}$ , $T_{KHQZ1}$	3.0ns to 2.0ns									
	$T_{KHQX1}$	2.0ns to 3.0ns									
rev 4.3	01/05/98	Updated DC Recommended Operating Conditions (page-6) Updated AC Test Conditions for $V_{DDQ} = 2.5V$ (page-10)									
rev 4.4	01/15/98	Deleted “-65” bins.									
rev 4.5	03/12/98	<p>Renamed “-50” bin to “-5” bin in all modes. Renamed “-60” bin to “-6” bin in all modes.</p> <p>Changed BSCAN register # 52 from <math>V_{SS}</math> to TNC (page-20) Modified BSCAN register table to include TNC (page-19)</p> <p><math>T_{KHQZ}</math> &amp; <math>T_{KHQZ1}</math> AC timing changed to 2.0ns for all bins (page-8 &amp;-9)</p> <p>Changed <math>V_{DIF}</math> (min) DC parameter from 0.4V to 0.5V (page-6) Changed <math>V_{CM}</math> (min) DC parameter from 1.2V to 1.15V (page-6) Changed <math>V_{CM}</math> (typ) DC parameter from <math>V_{DDQ}/2</math> to 1.4V (page-6) Deleted LVTTTL Clock <math>V_{IH}</math> and <math>V_{IL}</math> DC parameters (page-6) Added LVTTTL Clock <math>V_{KIN}</math> DC parameter (page-6) Added LVTTTL Clock <math>V_X</math> DC parameter (page-6) Added Note 5 (Clock description) to DC Recommendations (page-6)</p> <p>Rearranged AC Test Conditions (page-10 &amp; Page-11) Removed “Preliminary” from the spec.</p>									
rev 4.6	08/12/98	<p>Modified AC Electrical Characteristics: R-R Mode:</p> <table> <tr> <td>-45</td> <td><math>T_{KHQV}</math></td> <td>2.3ns to 2.4ns</td> </tr> </table>	-45	$T_{KHQV}$	2.3ns to 2.4ns						
-45	$T_{KHQV}$	2.3ns to 2.4ns									