

## Features

- Temperature ranges
  - Automotive-A: -40 °C to 85 °C
  - Automotive-E: -40 °C to 125 °C
- Pin and function compatible with CY7C1041BNV33
- High speed
  - $t_{AA}$  = 10 ns (Automotive-A)
  - $t_{AA}$  = 12 ns (Automotive-E)
- Low active power
  - 432 mW (max)
- 2.0 V data retention
- Automatic power down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features
- Available in Pb-free and non Pb-free 44-pin 400 Mil SOJ, 44-pin TSOP II and 48-ball FBGA packages

## Functional Description

The CY7C1041CV33 Automotive is a high performance CMOS static RAM organized as 262,144 words by 16 bits.

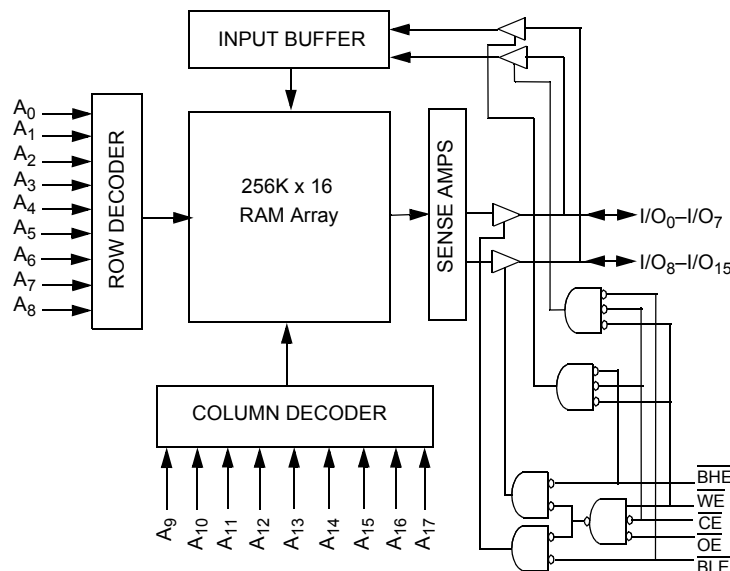
To write to the device, take Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from I/O pins ( $I/O_0$  through  $I/O_7$ ), is written into the location specified on the address pins ( $A_0$  through  $A_{17}$ ). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from I/O pins ( $I/O_8$  through  $I/O_{15}$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{17}$ ).

To read from the device, take Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins appear on  $I/O_0$  to  $I/O_7$ . If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory appears on  $I/O_8$  to  $I/O_{15}$ . For more information, see the [Truth Table on page 10](#) for a complete description of Read and Write modes.

The input and output pins ( $I/O_0$  through  $I/O_{15}$ ) are placed in a high impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), the  $\overline{BHE}$  and  $\overline{BLE}$  are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH), or during a write operation ( $\overline{CE}$  LOW and  $\overline{WE}$  LOW).

For best practice recommendations, refer to the Cypress application note [AN1064, SRAM System Guidelines](#).

## Logic Block Diagram



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## Selection Guide

| Description                  |              | -10 | -12 | -20 | Unit |
|------------------------------|--------------|-----|-----|-----|------|
| Maximum Access Time          |              | 10  | 12  | 20  | ns   |
| Maximum Operating Current    | Automotive-A | 100 | –   | 85  | mA   |
|                              | Automotive-E | –   | 120 | 90  | mA   |
| Maximum CMOS Standby Current | Automotive-A | 10  | –   | 10  | mA   |
|                              | Automotive-E | –   | 15  | 15  | mA   |

## Pin Configuration

Figure 1. 44-pin SOJ/T SOP II (Top View) <sup>[1]</sup>

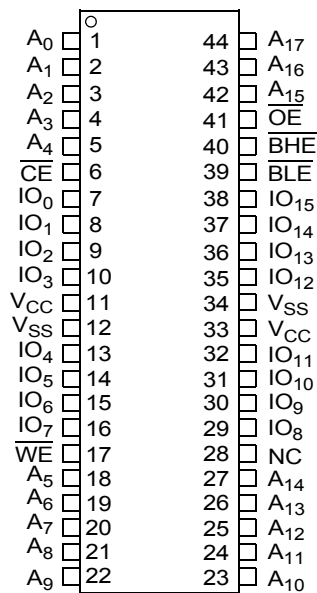
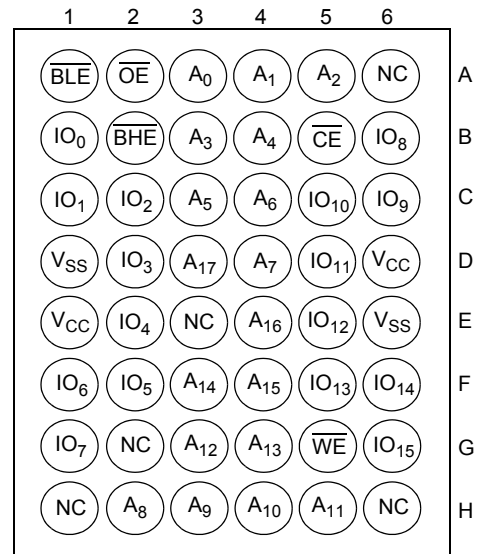


Figure 2. 48-ball FBGA Pinout (Top View) <sup>[1]</sup>



### Note

1. NC pins are not connected on the die.

## Pin Definitions

| Pin Name                            | SOJ, TSOP Pin Number      | BGA Pin Number   | I/O Type         | Description  |
|-------------------------------------|---------------------------|--|------------------|--|
| A <sub>0</sub> –A <sub>17</sub>     | 1–5, 18–27, 42–44         | A3, A4, A5, B3, B4, C3, C4, D4, H2, H3, H4, H5, G3, G4, F3, F4, E4, D3 | Input            | <b>Address Inputs.</b> Used to select one of the address locations.  |
| I/O <sub>0</sub> –I/O <sub>15</sub> | 7–10, 13–16, 29–32, 35–38 | B1, C1, C2, D2, E2, F2, F1, G1, B6, C6, C5, D5, E5, F5, F6, G6         | Input or Output  | <b>Bidirectional Data I/O lines.</b> Used as input or output lines depending on operation.   |
| NC                                  | 28                        | A6, E3, G2, H1, H6   | No Connect       | <b>No Connects.</b> Not connected to the die.  |
| $\overline{WE}$                     | 17                        | G5   | Input or Control | <b>Write Enable Input, Active LOW.</b> When selected LOW, a write is conducted. When deselected HIGH, a read is conducted.   |
| $\overline{CE}$                     | 6                         | B5   | Input or Control | <b>Chip Enable Input, Active LOW.</b> When LOW, selects the chip. When HIGH, deselects the chip.   |
| $\overline{BHE}$ , $\overline{BLE}$ | 40, 39                    | B2, A1   | Input or Control | <b>Byte Write Select Inputs, Active LOW.</b> $\overline{BHE}$ controls I/O <sub>15</sub> – I/O <sub>8</sub> , $\overline{BLE}$ controls I/O <sub>7</sub> – I/O <sub>0</sub> .                                    |
| $\overline{OE}$                     | 41                        | A2   | Input or Control | <b>Output Enable, Active LOW.</b> Controls the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, the I/O pins are tri-stated and act as input data pins. |
| V <sub>SS</sub>                     | 12, 34                    | D1, E6   | Ground           | <b>Ground for the Device.</b> Connected to ground of the system.   |
| V <sub>CC</sub>                     | 11, 33                    | D6, E1   | Power Supply     | <b>Power Supply Inputs to the Device.</b>  |

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... -65 °C to +150 °C  
 Ambient Temperature with Power Applied ..... -55 °C to +125 °C  
 Supply Voltage on V<sub>CC</sub> Relative to GND<sup>[2]</sup> ... -0.5 V to +4.6 V  
 DC Voltage Applied to Outputs in High Z State<sup>[2]</sup> ..... -0.5 V to V<sub>CC</sub> + 0.5 V  
 DC Input Voltage<sup>[2]</sup> ..... -0.5 V to V<sub>CC</sub> + 0.5 V

Current into Outputs (LOW)..... 20 mA  
 Static Discharge Voltage..... > 2001 V (MIL-STD-883, Method 3015)  
 Latch Up Current ..... > 200 mA

## Operating Range

| Range        | Ambient Temperature (T <sub>A</sub> ) | V <sub>CC</sub> |
|--------------|---------------------------------------|-----------------|
| Automotive-A | -40 °C to +85 °C                      | 3.3 V ± 10%     |
| Automotive-E | -40 °C to +125 °C                     |                 |

## Electrical Characteristics

Over the Operating Range

| Parameter                      | Description                                   | Test Conditions  | -10    |                       | -12  |                       | -20  |                       | Unit |    |
|--------------------------------|---|--|--------|-----------------------|------|-----------------------|------|-----------------------|------|----|
|                                |   |  | Min    | Max                   | Min  | Max                   | Min  | Max                   |      |    |
| V <sub>OH</sub>                | Output HIGH Voltage                           | V <sub>CC</sub> = Min, I <sub>OH</sub> = -4.0 mA   | 2.4    | -                     | 2.4  | -                     | 2.4  | -                     | V    |    |
| V <sub>OL</sub>                | Output LOW Voltage                            | V <sub>CC</sub> = Min, I <sub>OL</sub> = 8.0 mA  | -      | 0.4                   | -    | 0.4                   | -    | 0.4                   | V    |    |
| V <sub>IH</sub>                | Input HIGH Voltage                            |  | 2.0    | V <sub>CC</sub> + 0.3 | 2.0  | V <sub>CC</sub> + 0.3 | 2.0  | V <sub>CC</sub> + 0.3 | V    |    |
| V <sub>IL</sub> <sup>[2]</sup> | Input LOW Voltage                             |  | -0.3   | 0.8                   | -0.3 | 0.8                   | -0.3 | 0.8                   | V    |    |
| I <sub>IX</sub>                | Input Leakage Current                         | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>   | Auto-A | -1                    | +1   | -                     | -    | -1                    | +1   | μA |
|                                |   |  | Auto-E | -                     | -    | -20                   | +20  | -20                   | +20  |    |
| I <sub>OZ</sub>                | Output Leakage Current                        | GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Output disabled   | Auto-A | -1                    | +1   | -                     | -    | -1                    | +1   | μA |
|                                |   |  | Auto-E | -                     | -    | -20                   | +20  | -20                   | +20  |    |
| I <sub>CC</sub>                | V <sub>CC</sub> Operating Supply Current      | V <sub>CC</sub> = Max, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>  | Auto-A | -                     | 100  | -                     | -    | -                     | 85   | mA |
|                                |   |  | Auto-E | -                     | -    | -                     | 120  | -                     | 90   |    |
| I <sub>SB1</sub>               | Automatic CE Power Down Current — TTL Inputs  | Max V <sub>CC</sub> , CE ≥ V <sub>IH</sub> , V <sub>IN</sub> ≥ V <sub>IH</sub> , or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub> | Auto-A | -                     | 40   | -                     | -    | -                     | 40   | mA |
|                                |   |  | Auto-E | -                     | -    | -                     | 45   | -                     | 45   |    |
| I <sub>SB2</sub>               | Automatic CE Power Down Current — CMOS Inputs | Max V <sub>CC</sub> , CE ≥ V <sub>CC</sub> - 0.3 V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3 V, or V <sub>IN</sub> ≤ 0.3 V, f = 0             | Auto-A | -                     | 10   | -                     | -    | -                     | 10   | mA |
|                                |   |  | Auto-E | -                     | -    | -                     | 15   | -                     | 15   |    |

**Note**

2. V<sub>IL</sub> (min) = -2.0 V and V<sub>IH</sub>(max) = V<sub>CC</sub> + 0.5 V for pulse durations of less than 20 ns.

### Capacitance

Tested initially and after any design or process changes that may affect these parameters.

| Parameter        | Description        | Test Conditions  | Max | Unit |
|------------------|--------------------|--|-----|------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = 3.3 V | 8   | pF   |
| C <sub>OUT</sub> | Output Capacitance |  | 8   | pF   |

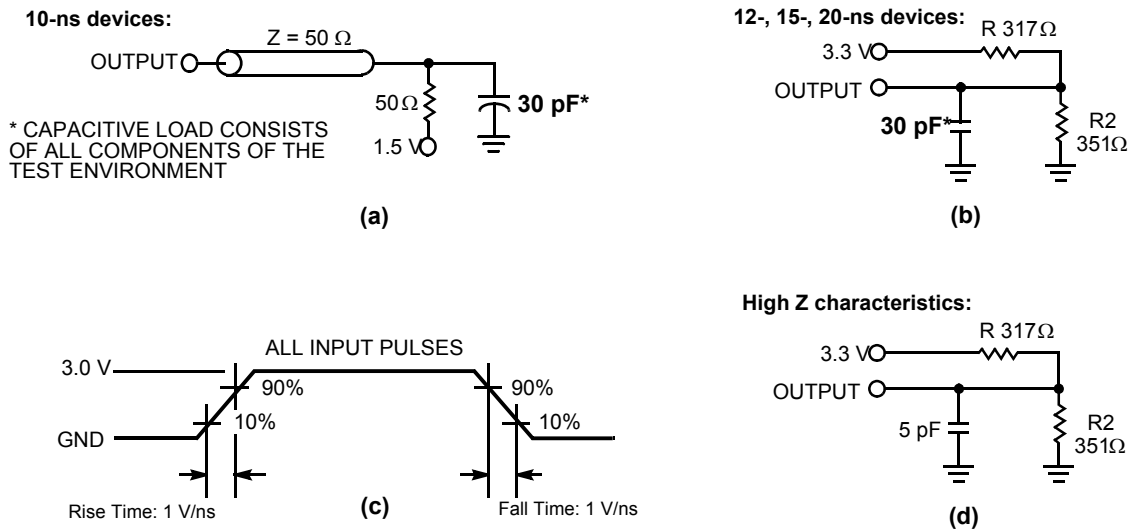
### Thermal Resistance

Tested initially and after any design or process changes that may affect these parameters.

| Parameter       | Description                              | Test Conditions   | SOJ   | TSOP II | FBGA  | Unit |
|-----------------|--|---|-------|---------|-------|------|
| Θ <sub>JA</sub> | Thermal Resistance (Junction to Ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51 | 25.99 | 42.96   | 38.15 | °C/W |
| Θ <sub>JC</sub> | Thermal Resistance (Junction to Case)    |   | 18.8  | 10.75   | 9.15  | °C/W |

### AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms [3]



**Note**

3. AC characteristics (except High Z) for 10 ns parts are tested using the load conditions shown in Figure 3 (a). All other speeds are tested using the Thevenin load shown in Figure 3 (b). High Z characteristics are tested for all speeds using the test load shown in Figure 3 (d).

## Switching Characteristics

Over the Operating Range <sup>[4]</sup>

| Parameter                           | Description                                      | -10    |     | -12 |     | -20 |     | Unit    |    |
|-------------------------------------|--|--------|-----|-----|-----|-----|-----|---------|----|
|                                     |  | Min    | Max | Min | Max | Min | Max |         |    |
| <b>Read Cycle</b>                   |  |        |     |     |     |     |     |         |    |
| $t_{power}^{[5]}$                   | $V_{CC}$ (Typical) to the First Access           | 100    | –   | 100 | –   | 100 | –   | $\mu s$ |    |
| $t_{RC}$                            | Read Cycle Time                                  | 10     | –   | 12  | –   | 20  | –   | ns      |    |
| $t_{AA}$                            | Address to Data Valid                            | –      | 10  | –   | 12  | –   | 20  | ns      |    |
| $t_{OHA}$                           | Data Hold from Address Change                    | 3      | –   | 3   | –   | 3   | –   | ns      |    |
| $t_{ACE}$                           | $\overline{CE}$ LOW to Data Valid                | –      | 10  | –   | 12  | –   | 20  | ns      |    |
| $t_{DOE}$                           | $\overline{OE}$ LOW to Data Valid                | Auto-A | –   | 5   | –   | 6   | –   | 8       | ns |
|                                     |  | Auto-E | –   | –   | –   | 7   | –   | 8       |    |
| $t_{LZOE}$                          | $\overline{OE}$ LOW to Low Z <sup>[6]</sup>      | 0      | –   | 0   | –   | 0   | –   | ns      |    |
| $t_{HZOE}$                          | $\overline{OE}$ HIGH to High Z <sup>[6, 7]</sup> | –      | 5   | –   | 6   | –   | 8   | ns      |    |
| $t_{LZCE}$                          | $\overline{CE}$ LOW to Low Z <sup>[6]</sup>      | 3      | –   | 3   | –   | 3   | –   | ns      |    |
| $t_{HZCE}$                          | $\overline{CE}$ HIGH to High Z <sup>[6, 7]</sup> | –      | 5   | –   | 6   | –   | 8   | ns      |    |
| $t_{PU}$                            | $\overline{CE}$ LOW to Power Up                  | 0      | –   | 0   | –   | 0   | –   | ns      |    |
| $t_{PD}$                            | $\overline{CE}$ HIGH to Power Down               | –      | 10  | –   | 12  | –   | 20  | ns      |    |
| $t_{DBE}$                           | Byte Enable to Data Valid                        | Auto-A | –   | 5   | –   | 6   | –   | 8       | ns |
|                                     |  | Auto-E | –   | –   | –   | 7   | –   | 8       |    |
| $t_{LZBE}$                          | Byte Enable to Low Z                             | 0      | –   | 0   | –   | 0   | –   | ns      |    |
| $t_{HZBE}$                          | Byte Disable to High Z                           | –      | 6   | –   | 6   | –   | 8   | ns      |    |
| <b>Write Cycle<sup>[8, 9]</sup></b> |  |        |     |     |     |     |     |         |    |
| $t_{WC}$                            | Write Cycle Time                                 | 10     | –   | 12  | –   | 20  | –   | ns      |    |
| $t_{SCE}$                           | $\overline{CE}$ LOW to Write End                 | 7      | –   | 8   | –   | 10  | –   | ns      |    |
| $t_{AW}$                            | Address Setup to Write End                       | 7      | –   | 8   | –   | 10  | –   | ns      |    |
| $t_{HA}$                            | Address Hold from Write End                      | 0      | –   | 0   | –   | 0   | –   | ns      |    |
| $t_{SA}$                            | Address Setup to Write Start                     | 0      | –   | 0   | –   | 0   | –   | ns      |    |
| $t_{PWE}$                           | $\overline{WE}$ Pulse Width                      | 7      | –   | 8   | –   | 10  | –   | ns      |    |
| $t_{SD}$                            | Data Setup to Write End                          | 5      | –   | 6   | –   | 8   | –   | ns      |    |
| $t_{HD}$                            | Data Hold from Write End                         | 0      | –   | 0   | –   | 0   | –   | ns      |    |
| $t_{LZWE}$                          | $\overline{WE}$ HIGH to Low Z <sup>[6]</sup>     | 3      | –   | 3   | –   | 3   | –   | ns      |    |
| $t_{HZWE}$                          | $\overline{WE}$ LOW to High Z <sup>[6, 7]</sup>  | –      | 5   | –   | 6   | –   | 8   | ns      |    |
| $t_{BW}$                            | Byte Enable to End of Write                      | 7      | –   | 8   | –   | 10  | –   | ns      |    |

### Notes

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V.
- $t_{POWER}$  gives the minimum amount of time that the power supply is at typical  $V_{CC}$  values until the first memory access is performed.
- At any temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZBE}$  is less than  $t_{LZBE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any device.
- $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZBE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in part (d) of Figure 3 on page 6. Transition is measured  $\pm 500$  mV from steady state voltage.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW,  $\overline{WE}$  LOW, and  $\overline{BHE}/\overline{BLE}$  LOW.  $\overline{CE}$ ,  $\overline{WE}$ , and  $\overline{BHE}/\overline{BLE}$  must be LOW to initiate a write. The transition of these signals terminate the write. The input data setup and hold timing is referenced to the leading edge of the signal that terminates the write.
- The minimum Write cycle time for Write Cycle No. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

### Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled)<sup>[10, 11]</sup>

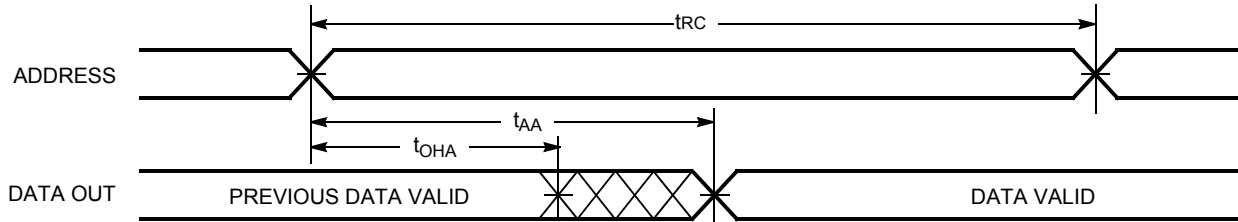
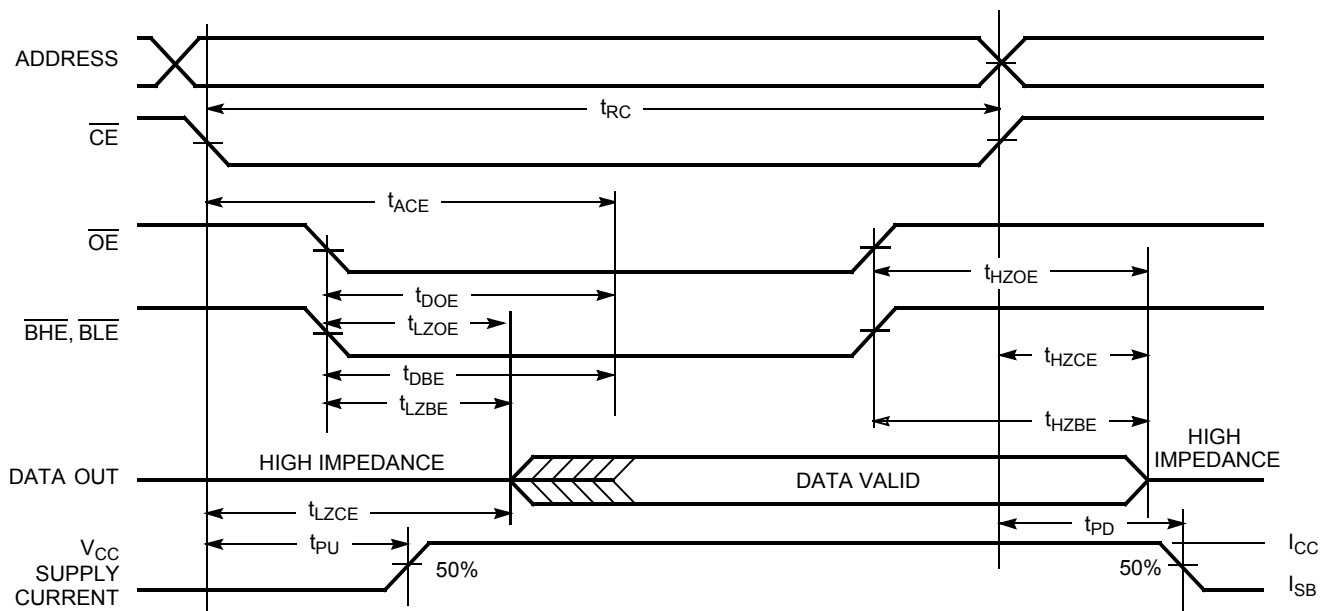


Figure 5. Read Cycle No. 2 ( $\overline{OE}$  Controlled)<sup>[11, 12]</sup>



**Notes**

- 10. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$ ,  $\overline{BHE}$ , and/or  $\overline{BLE} = V_{IL}$ .
- 11.  $\overline{WE}$  is HIGH for read cycle.
- 12. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.



Switching Waveforms (continued)

Figure 6. Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled)<sup>[13, 14]</sup>

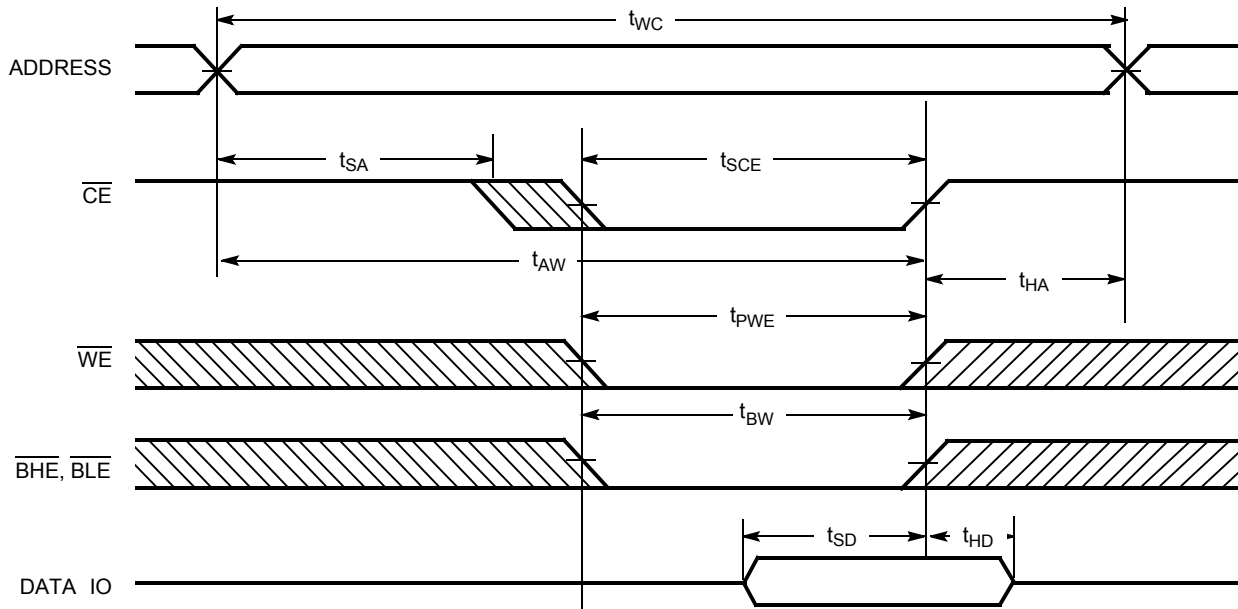
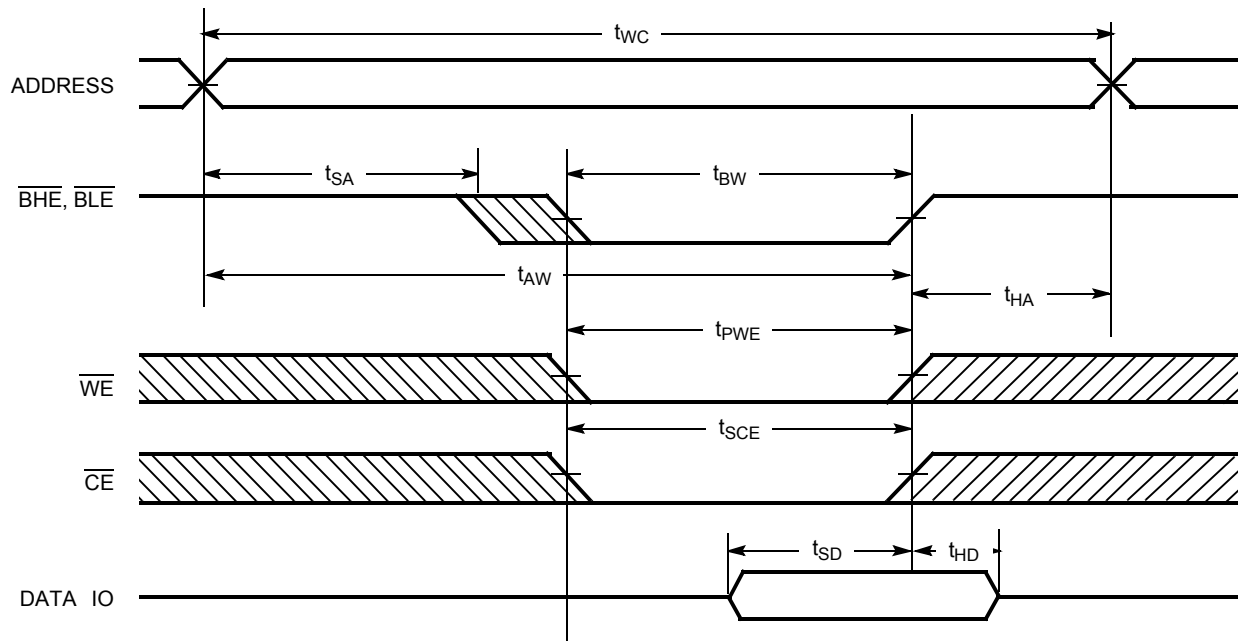


Figure 7. Write Cycle No. 2 ( $\overline{\text{BLE}}$  or  $\overline{\text{BHE}}$  Controlled)



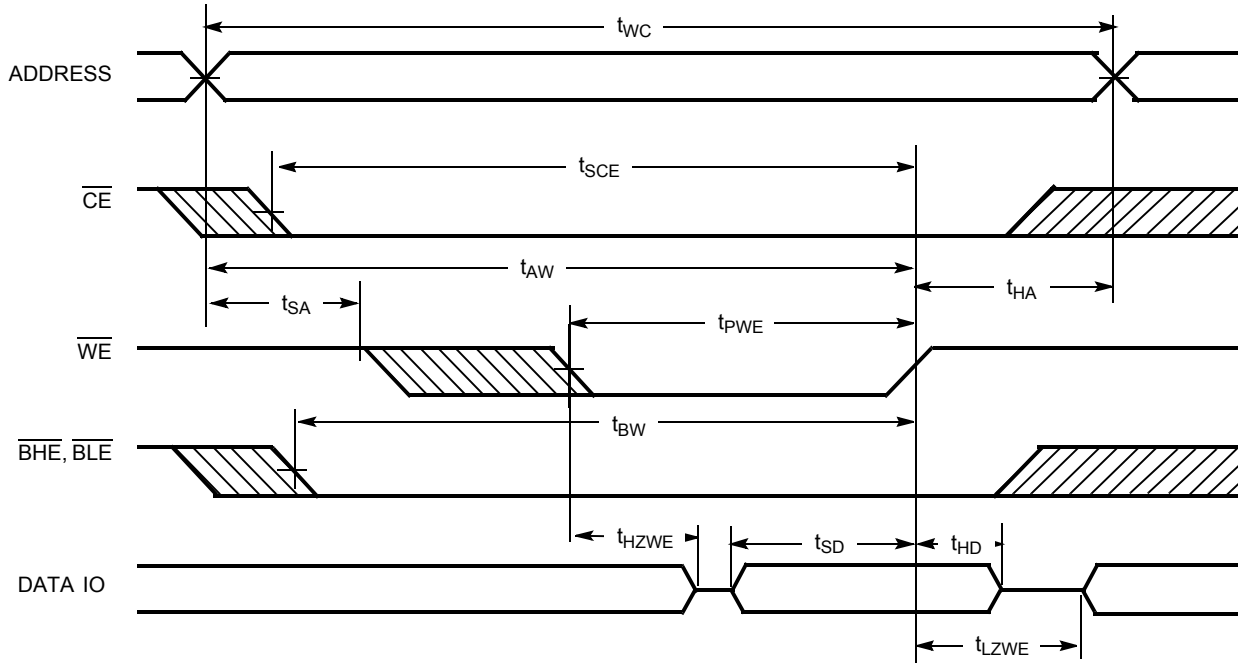
Notes

13. Data IO is high impedance if  $\overline{\text{OE}}$ ,  $\overline{\text{BHE}}$ , and/or  $\overline{\text{BLE}} = V_{IH}$ .

14. If  $\overline{\text{CE}}$  goes HIGH simultaneously with WE going HIGH, the output remains in a high impedance state.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)



Truth Table

| $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | $\overline{BLE}$ | $\overline{BHE}$ | I/O <sub>0</sub> - I/O <sub>7</sub> | I/O <sub>8</sub> - I/O <sub>15</sub> | Mode                       | Power                      |
|-----------------|-----------------|-----------------|------------------|------------------|-------------------------------------|--------------------------------------|----------------------------|----------------------------|
| H               | X               | X               | X                | X                | High Z                              | High Z                               | Power Down                 | Standby (I <sub>SB</sub> ) |
| L               | L               | H               | L                | L                | Data Out                            | Data Out                             | Read - All Bits            | Active (I <sub>CC</sub> )  |
|                 |                 |                 | L                | H                | Data Out                            | High Z                               | Read - Lower Bits Only     | Active (I <sub>CC</sub> )  |
|                 |                 |                 | H                | L                | High Z                              | Data Out                             | Read - Upper Bits Only     | Active (I <sub>CC</sub> )  |
| L               | X               | L               | L                | L                | Data In                             | Data In                              | Write - All Bits           | Active (I <sub>CC</sub> )  |
|                 |                 |                 | L                | H                | Data In                             | High Z                               | Write - Lower Bits Only    | Active (I <sub>CC</sub> )  |
|                 |                 |                 | H                | L                | High Z                              | Data In                              | Write - Upper Bits Only    | Active (I <sub>CC</sub> )  |
| L               | H               | H               | X                | X                | High Z                              | High Z                               | Selected, Outputs Disabled | Active (I <sub>CC</sub> )  |
| L               | X               | X               | H                | H                | High Z                              | High Z                               | Selected, Outputs Disabled | Active (I <sub>CC</sub> )  |

## Ordering Information

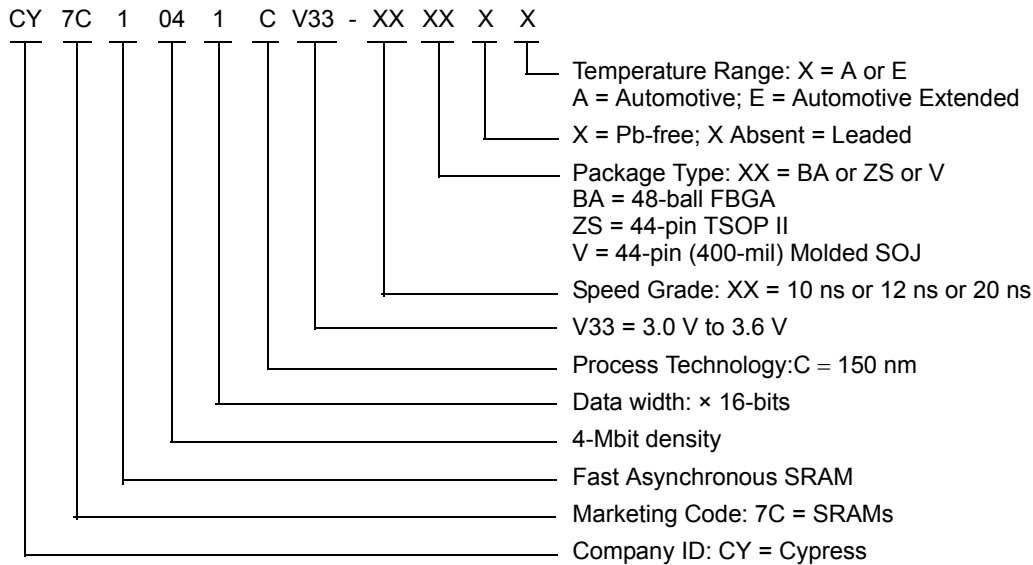
Cypress offers other versions of this type of product in many different configurations and features. The below table contains only the list of parts that are currently available. For a complete listing of all options, visit the Cypress website at [www.cypress.com](http://www.cypress.com) and refer to the product summary page at <http://www.cypress.com/products> or contact your local sales representative.

Cypress maintains a worldwide network of offices, solution centers, manufacturer’s representatives and distributors. To find the office closest to you, visit us at <http://www.cypress.com/go/datasheet/offices>.

| Speed (ns) | Ordering Code       | Package Diagram | Package Type                          | Operating Range |
|------------|---------------------|-----------------|---------------------------------------|-----------------|
| 10         | CY7C1041CV33-10BAXA | 51-85106        | 48-ball FBGA (Pb-free)                | Automotive-A    |
|            | CY7C1041CV33-10ZSXA | 51-85087        | 44-pin TSOP II (Pb-free)              |                 |
| 12         | CY7C1041CV33-12BAXE | 51-85106        | 48-ball FBGA (Pb-free)                | Automotive-E    |
|            | CY7C1041CV33-12ZSXE | 51-85087        | 44-pin TSOP II (Pb-free)              |                 |
| 20         | CY7C1041CV33-20ZSXA | 51-85087        | 44-pin TSOP II (Pb-free)              | Automotive-A    |
|            | CY7C1041CV33-20VXE  |                 | 44-pin (400-mil) Molded SOJ (Pb-free) | Automotive-E    |
|            | CY7C1041CV33-20ZSXE |                 | 44-pin TSOP II (Pb-free)              |                 |

Please contact your local Cypress sales representative for availability of these parts

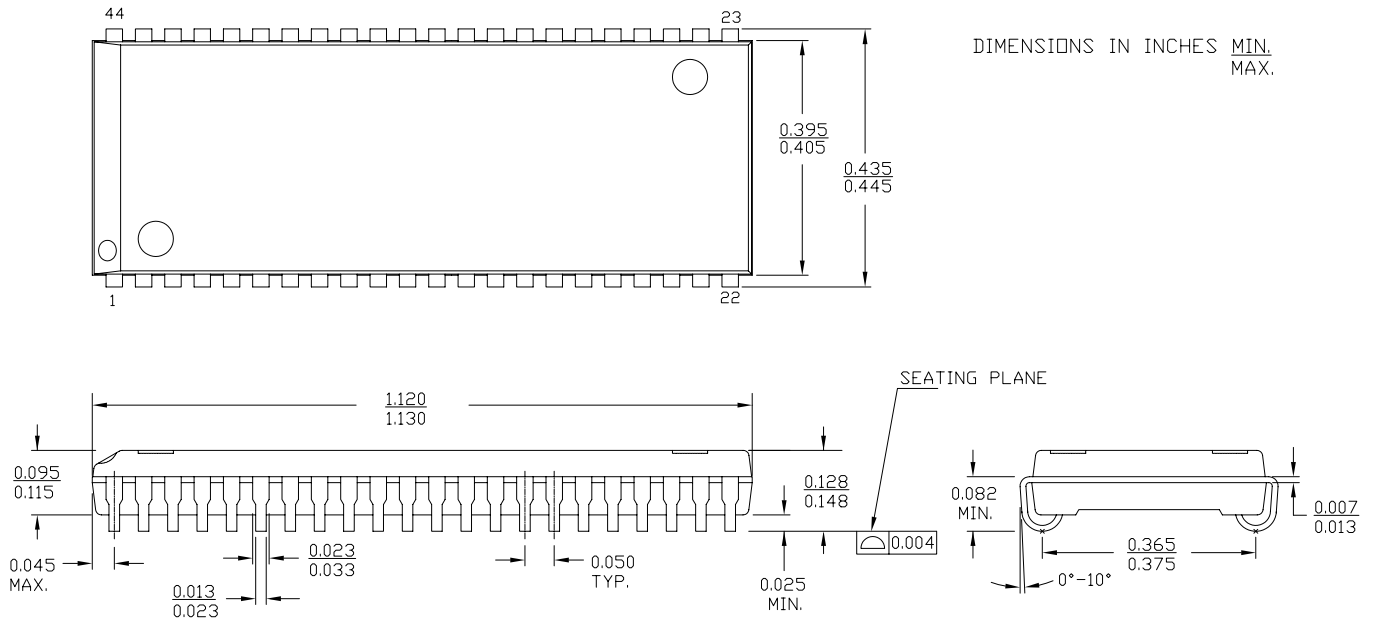
## Ordering Code Definitions



**Package Diagrams**

**Figure 9. 44-pin (400 Mil) Molded SOJ, 51-85082**

**44 Lead (400 MIL) MOLDED SOJ**

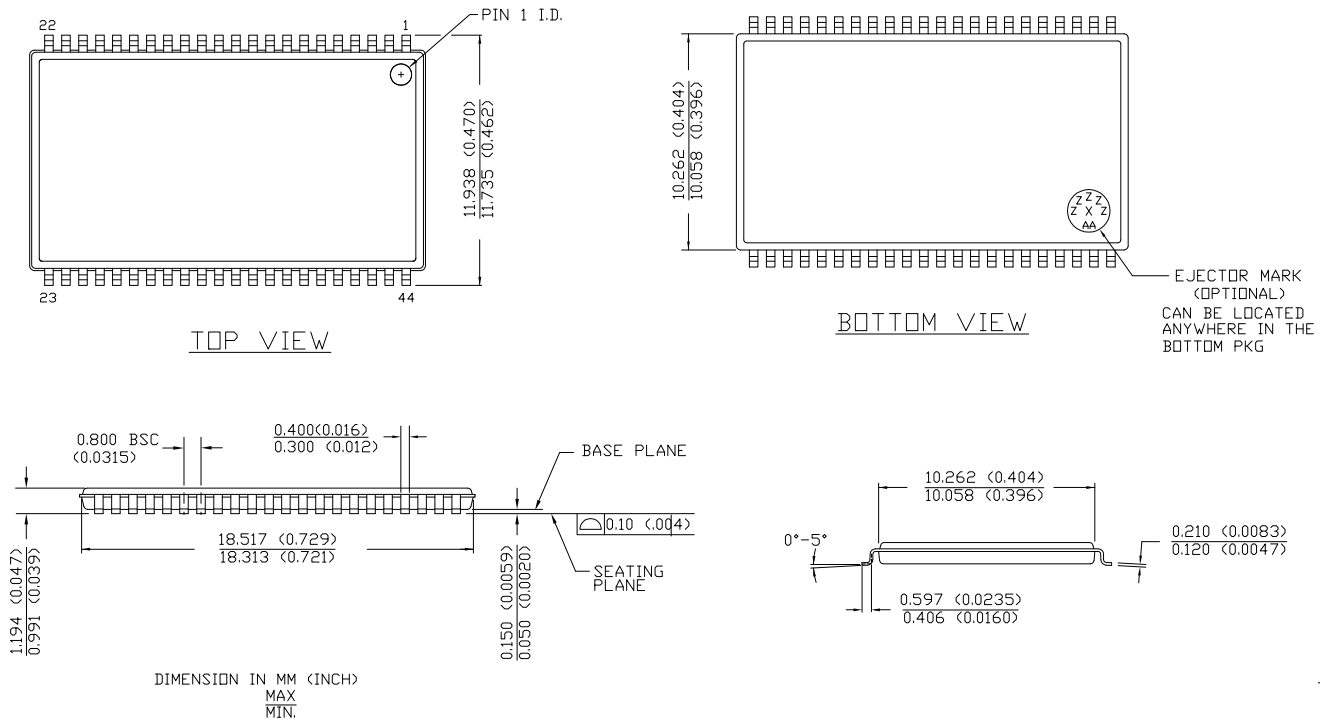


51-85082 °C

**Package Diagrams** (continued)

**Figure 10. 44-pin Thin Small Outline Package Type II, 51-85087**

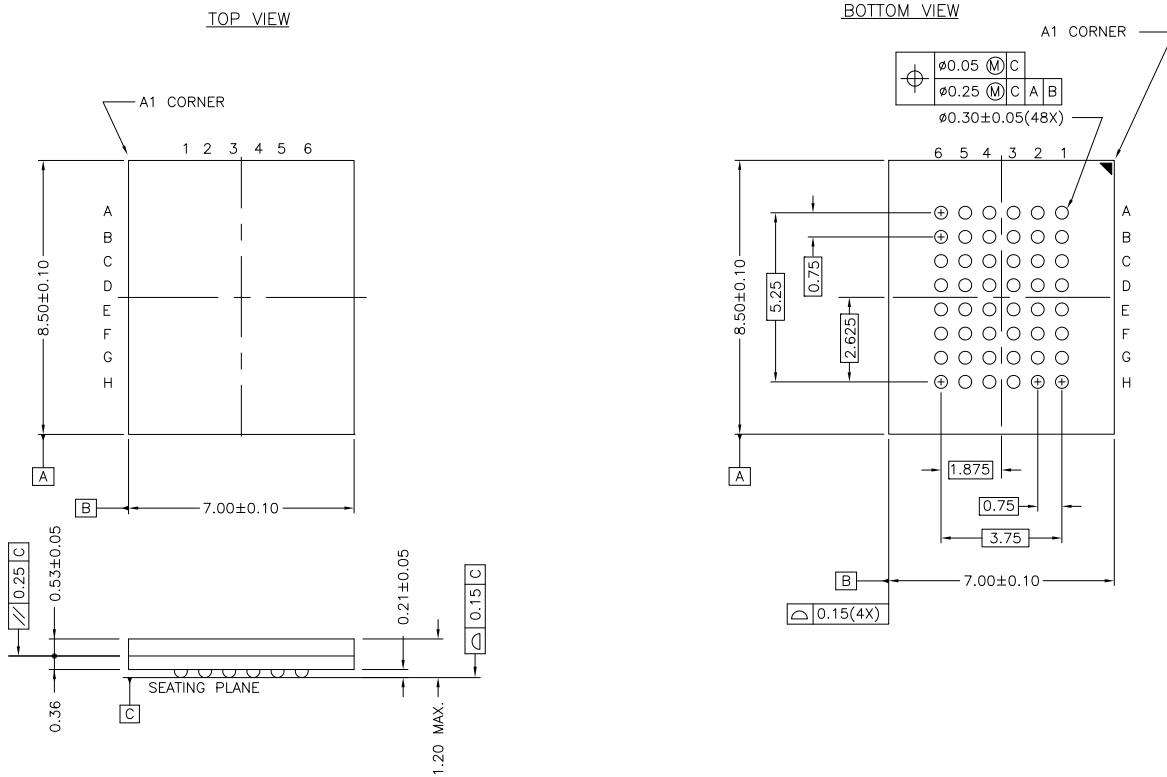
44 Lead TSOP TYPE II – STANDARD



51-85087 °C

**Package Diagrams** (continued)

**Figure 11. 48-ball FBGA (7 × 8.5 × 1.2 mm), 51-85106**



51-85106 \*F

**Acronyms**

| Acronym | Description                             |
|---------|---|
| CE      | Chip Enable                             |
| CMOS    | complementary metal oxide semiconductor |
| FBGA    | fine-pitch ball grid array              |
| I/O     | input/output                            |
| OE      | Output Enable                           |
| PLL     | phase locked loop                       |
| SOJ     | Small Outline J-lead                    |
| SRAM    | static random access memory             |
| TSOP    | thin small outline package              |
| TTL     | transistor-transistor logic             |
| WE      | Write Enable                            |

**Document Conventions**

**Units of Measure**

| Symbol       | Unit of Measure |
|--------------|-----------------|
| $\Omega$     | ohms            |
| ns           | nano seconds    |
| V            | Volts           |
| $\mu$ s      | micro seconds   |
| $\mu$ A      | micro Amperes   |
| mA           | milli Amperes   |
| mm           | milli meter     |
| ms           | milli seconds   |
| MHz          | Mega Hertz      |
| pF           | pico Farad      |
| %            | percent         |
| mW           | milli Watts     |
| W            | Watts           |
| $^{\circ}$ C | degree Celcius  |

## Document History Page

| Document Title: CY7C1041CV33 Automotive, 4-Mbit (256 K × 16) Static RAM<br>Document Number: 001-67307 |         |            |                 |   |
|---|---------|------------|-----------------|---|
| REV.  | ECN NO. | Issue Date | Orig. of Change | Description of Change   |
| **  | 3187164 | 03/03/2011 | PRAS            | Separation of the automotive datasheet from CY7C1041CV33 spec no. 38-05134 Rev. *K. Further rev of 38-05134 would include only industrial / commercial parts. |



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