

C3D1P7060QSilicon Carbide Schottky Diode

Z-RECTM RECTIFIER

 $V_{RRM} = 600 \text{ V}$ $I_{F;} T_{c} < 150 \text{ °C} = 1.7 \text{ A}$ $Q_{c} = 5.6 \text{ nC}$

Features

- 600-Volt Schottky Rectifier
- Optimized for PFC Boost Diode Application
- Zero Reverse Recovery Current
- High-Frequency Operation
- Temperature-Independent Switching Behavior
- Extremely Fast Switching
- Positive Temperature Coefficient on V_E

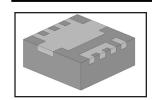
Benefits

- Small compact surface mount package
- Essentially No Switching Losses
- Higher Efficiency
- Reduction of Heat Sink Requirements
- Parallel Devices Without Thermal Runaway

Applications

- Switch Mode Power Supplies
- LED Lighting

Package



PowerQFN 3.3x3.3





| Part Number | Package | Marking | | |
|-------------|---------|-----------|--|--|
| C3D1P7060Q | QFN 3.3 | C3D1P7060 | | |

Maximum Ratings

| Symbol | Parameter | Value | Unit | Test Conditions | Note |
|---|--|----------------|--------|--|--------------|
| V _{RRM} | Repetitive Peak Reverse Voltage | 600 | V | | |
| V_{RSM} | Surge Peak Reverse Voltage | 600 | V | | |
| V _{DC} | DC Blocking Voltage | 600 | V | | |
| $I_{\scriptscriptstyle \sf F}$ | Continuous Forward Current | 1.7 3 | A A | T _c <150°C, No AC Component T _c <135°C, No AC Component | See Fig 3 |
| \mathbf{I}_{FRM} | Repetitive Peak Forward Surge Current | 7 4.4 | А | T_c =25°C, t_p =10 ms, Half Sine pulse T_c =110°C, t_p =10 ms, Half Sine pulse | |
| $\boldsymbol{I}_{\text{FSM}}$ | Non-Repetitive Peak Forward Surge Current | 15 12 | А | T_c =25°C, t_p =10 ms, Half Sine pulse T_c =110°C, t_p =10 ms, Half Sine pulse | |
| P_{tot} | Power Dissipation | 39 17 | W | T _c =25°C T _c =110°C | |
| $T_{_{\mathtt{J}}}$, $T_{_{\mathtt{stg}}}$ | Operating Junction and Storage Temperature | -55 to +175 | °C | | |
| T_{c} | Maximum Case Temperature | 150 | °C | | |



Electrical Characteristics

| Symbol | Parameter | Тур. | Max. | Unit | Test Conditions | Note |
|----------------|-------------------------|---------------|------------|------|--|------|
| V _F | Forward Voltage | 1.5 1.8 | 1.7 2.4 | V | $I_F = 1.7 \text{ A } T_J = 25^{\circ}\text{C}$ $I_F = 1.7 \text{ A } T_J = 175^{\circ}\text{C}$ | |
| I _R | Reverse Current | 10 20 | 50 100 | μΑ | $V_R = 600 \text{ V } T_J = 25^{\circ}\text{C}$ $V_R = 600 \text{ V } T_J = 175^{\circ}\text{C}$ | |
| Q _c | Total Capacitive Charge | 5.6 | | nC | $V_R = 600 \text{ V, } I_F = 1.7\text{A}$ $di/dt = 500 \text{ A/}\mu\text{s}$ $T_J = 25^{\circ}\text{C}$ | |
| С | Total Capacitance | 100 7 6 | | pF | $V_R = 0 \text{ V, } T_J = 25^{\circ}\text{C, } f = 1 \text{ MHz}$ $V_R = 200 \text{ V, } T_J = 25^{\circ}\text{C, } f = 1 \text{ MHz}$ $V_R = 400 \text{ V, } T_J = 25^{\circ}\text{C, } f = 1 \text{ MHz}$ | |

Note:

Thermal Characteristics

| Symbol | Parameter | | Unit |
|-----------------|--|-----|------|
| $R_{\theta JC}$ | Package Thermal Resistance from Junction to Case | 3.8 | °C/W |

Typical Performance

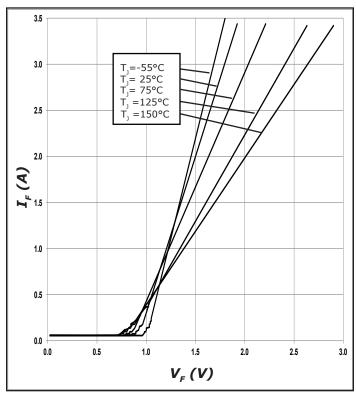


Figure 1. Forward Characteristics

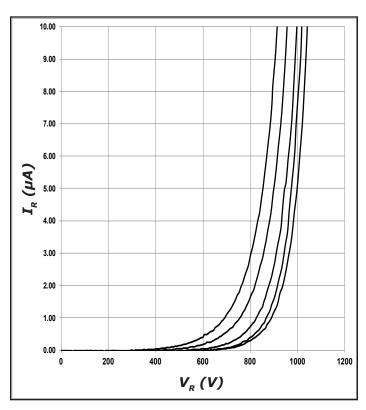
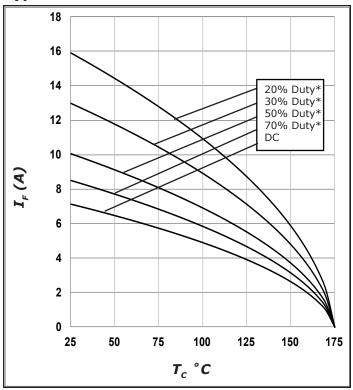


Figure 2. Reverse Characteristics

^{1.} This is a majority carrier diode, so there is no reverse recovery charge.



Typical Performance



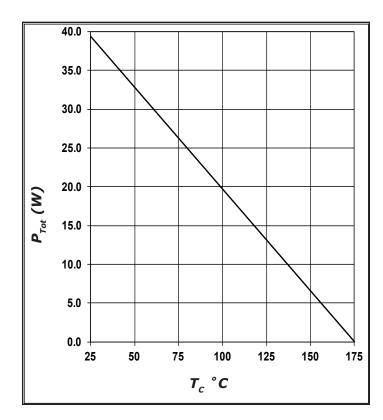


Figure 3. Current Derating

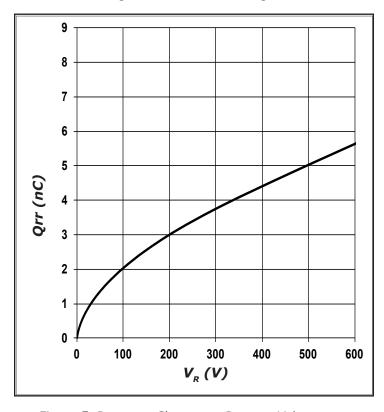


Figure 5. Recovery Charge vs. Reverse Voltage

Figure 4. Power Derating

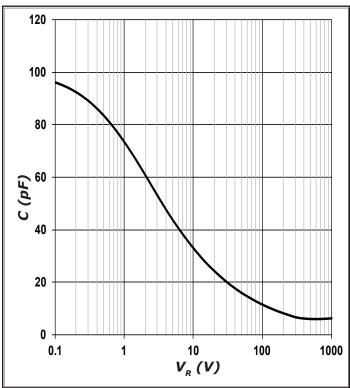


Figure 6. Capacitance vs. Reverse Voltage



Typical Performance

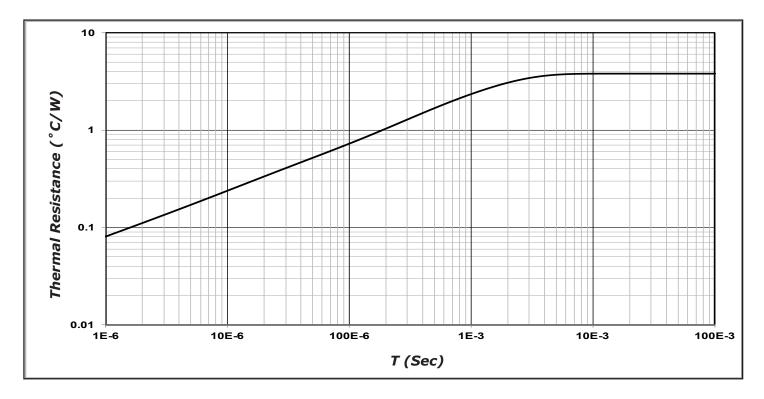


Figure 7. Transient Thermal Impedance

Diode Model

$$\begin{array}{c|c} - & & \\ \hline - & & \\ - & & \\ \hline - & & \\ - & & \\ \hline - & & \\ - & & \\ \hline - & & \\ - & & \\ \hline - & & \\ - & & \\ \hline - & & \\ - & & \\ \hline - & & \\ - & & \\ \hline - & & \\ - & & \\ \hline - & & \\ - & & \\ \hline - & &$$

$$Vf_T = V_T + If * R_T$$

$$V_T = 0.99 + (T_J^* -1.5*10^{-3})$$

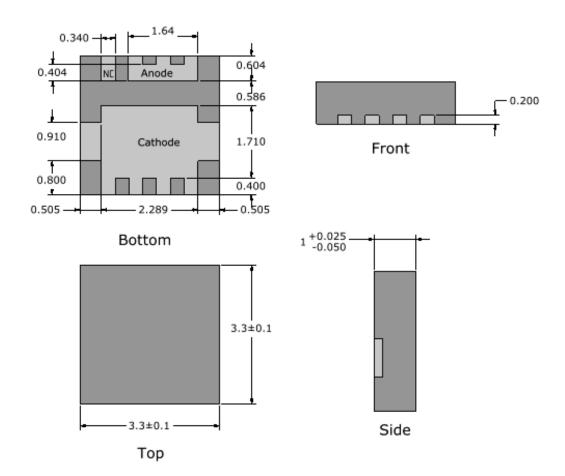
 $R_T = 0.22 + (T_J^* 2.6*10^{-3})$

Note: T_i = Diode Junction Temperature In Degrees Celcius



Package Dimensions

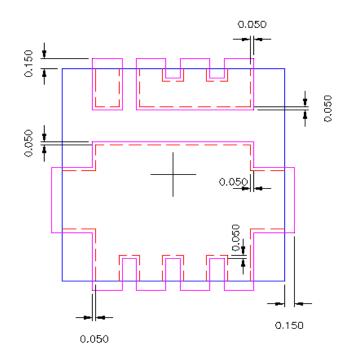
Package QFN 3.3

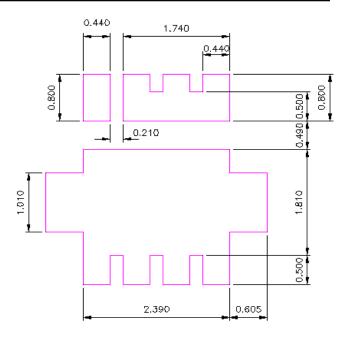


All Dimensions are in mm Tolerances are 0.05 mm if not specified NC = No Connect



Recommended Landing Pattern (All Dimensions are in mm)





Note: The design of the land pattern and the size of the thermal pad depend mainly on the thermal characteristic and power dissipation. In general, the size of the thermal pad should be as close to the exposed pad of the package as possible, provided that there is no bridging between the thermal pad and the lead pads.

The 0.050mm extra length and width provides space to accommodate the placement tolerance of the component during pick and place process. The 0.150mm along the perimeter present areas for solder to form fillet along the side metal edges of the package.

"The levels of environmentally sensitive, persistent biologically toxic (PBT), persistent organic pollutants (POP), or otherwise restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2002/95/EC on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS), as amended through April 21, 2006."

This product has not been designed or tested for use in, and is not intended for use in, applications implanted into the human body nor in applications in which failure of the product could lead to death, personal injury or property damage, including but not limited to equipment used in the operation of nuclear facilities, life-support machines, cardiac defibrillators or similar emergency medical equipment, aircraft navigation or communication or control systems, air traffic control systems, or weapons systems.

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