## General Description

The ICS1532 is a high-performance, cost-effective, 3-channel, 8-bit analog-to-digital converter with an integrated line-locked clock generator. They are part of a family of chips for high-resolution video applications that use analog inputs, such as LCD monitors, projectors, plasma displays, and HDTVs. Using low-voltage CMOS mixed-signal technology, they are an effective data-capture solution for VGA to UXGA.

The ICS1532 chips offer analog-to-digital data conversion and synchronized pixel-clock generation up to 110 Mega samples per second, (MSPS) or 110 MHz. The Dynamic Phase Adjust (DPA) circuitry allows end-user control over the pixel clock phase, relative to the recovered sync signal and analog pixel data. The ICS1532 provides two 24-bit pixels per clock. An ADCSYNC output pin provides recovered HSYNC in phase with the ADCRCLK output to be used to synchronize horizontal timing.

A clamp signal can be generated internally or provided through the CLAMP pin. An adjustable-gain video amplifier fine tunes the analog signal. The PLL uses an internal programmable feedback divider.

Two additional, independent programmable PLLs, each with spread-spectrum functionality, can support memory and panel clock requirements.
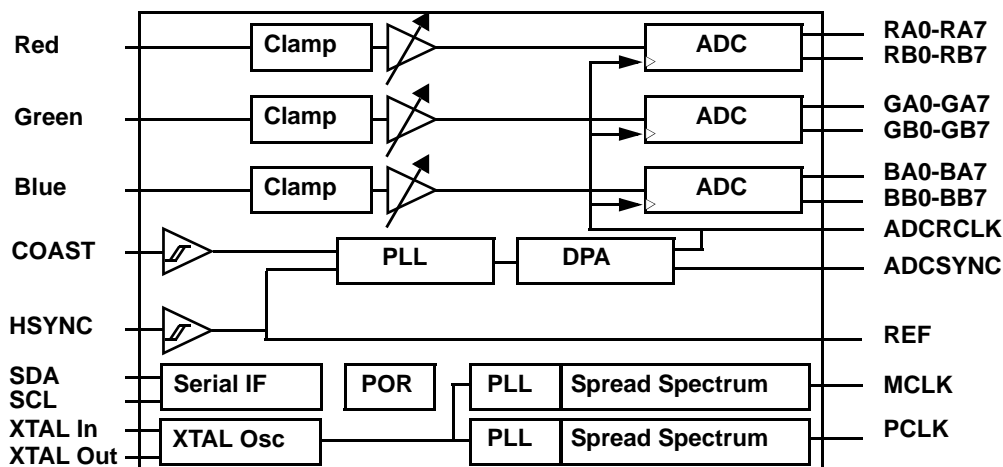
Features

- Triple 8-bit analog-to-digital conversion
- 10 to 110 MHz operation
- Direct connection to analog input data
    — Internal AC coupling capacitors
- Internal camp circuit and external clamp inputs
- Optional External Phase Detector Enable input
    — COAST
- Uses 3.3 and 2.5 VDC
    — 5 V tolerant digital inputs
- Integrated Amplifier with Adjustable Gain and Offset
- Dynamic Phase Adjust (DPA)
    — Software adjustable analog sample point
- Low jitter
- Two additional PLLs
    — Programmable spread spectrum
- Automatic Power-On Reset Detection
- Standard I^{2}C 2-wire serial interface
    — Two address sets available via external pin
- Lock detection in both hardware and software
- 144-pin low-profile quad flat pack (LQFP) package

Block Diagram

Table of Contents

Chapter 1   Summary

The ICS1532 is the ideal device for capturing analog RGB from a personal computer or other sources into the digital domain for display on a digital device such as an LCD panel. Contained inside the ICS1532 device are the following blocks to accomplish this:

- **Main PLL -** Re-generates required clock for sampling analog input data

- **DPA -** Adjusts the phase of the sampling clock.

- **Clamps** - Controls the ADC's zero code value.

- **Amplifiers** - Controls the ADC's full scale code value.

- **ADC -** Three ADCs converts the analog input into digital.

- **I2C** - Standard I^{2}C bus used for controlling the device

- **POR** - Power on reset for the I2C interface

- **Two Spread Spectrum Utility PLLs -** For generating any other clocks needed by the system.

1.1   Main Phase-Locked Loop (PLL)

Main PLL- The main PLL is used for re-generating the clocks needed to properly sample the incoming analog signals.

Figure 1-1   Simplified PLL Diagram
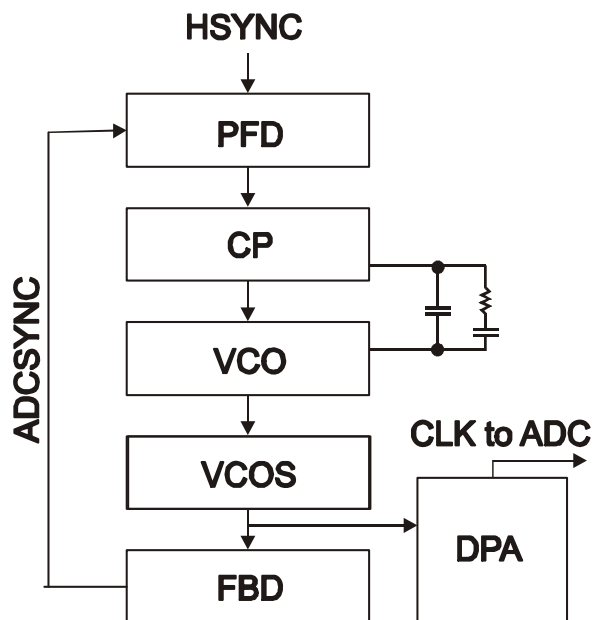
The heart of the ICS1532 is a voltage controlled oscillator (VCO). The VCO's speed is controlled by the voltage on the loop filter. This voltage will be described later in this section.

1.2   VCO Divider (VCOD)

The VCO's clock output is first passed through the VCO Divider (VCOD). The VCOD allows the VCO to operate at higher speeds than the required output clock.

NOTE: Under normal, locked operation the VCOS has no effect on the speed of the output clocks, just the **VCO frequency.**

1.3   Dynamic Phase Adjust (DPA)

The output of the VCOS is then sent through the Dynamic Phase Adjust (DPA) for phase adjustment and also the 12 bit internal Feedback Divider. The feedback divider controls how many clocks are seen during every cycle of the input reference.

1.4   Feedback Divider (FBD)

The feedback divider output is a 4 CLK wide signal called ADCSYNC. The ADCSYNC signal is aligned with the output clocks and is intended to be used by the system as a replacement for the HSYNC input, which is of indeterminate quality and is not aligned with the output clocks.

1.5   Phase Frequency Detector (PFD)

The Phase Frequency Detector (PFD) then compares ADCSYNC to the selected input HSYNC and controls the filter voltage by enabling and disabling the charge pump. The charge pump has programmable current drive and will source and sink current as appropriate to keep the input HSYNC and the ADCSYNC output aligned.

The PFD's HSYNC input is conditioned by a high-performance Schmitt trigger. This preconditioned HSYNC signal, called REF, is provided as a clean reference signal with a short transition time can be output on pin 112.

1.6   OSC Input

The high-frequency OSC input pin, has a 7-bit user programmable divider can also be selected as the loop input. This selection allows the loop to operate from

any appropriate, single ended source, typically a crystal oscillator.

Either the conditioned HSYNC input or the loop output (recovered HSYNC) is available at the FUNC pin, and is aligned with the output clocks.

1.7 Dynamic Phase Adjust - DPA

The DPA is used for adjusting the phase relationship of the main PLL's re-generated clock to the incoming analog data to assure properly sampled analog data.

The Dynamic Phase Adjust (DPA) allows a programmable clock delay relative to the input HSYNC signal. A delay of up to one clock period is programmable: See Chapter 5, "DPA Operation" for more details.

1.8 Clamps

The ICS1532 contains clamping circuitry to compensate for non zero volt black levels on the incoming video lines. Clamping causes the device to charge internal level shifting capacitors to the complementary voltage level of the analog input. This guarantees that the input is in the proper voltage range to be converted by the ADC and also has the effect of making whatever the analog voltage level on the inputs is during the Clamp interval, equal to approximately a 00 code.

Clamping may be initiated either internally, by the ADCSYNC signal, or externally via the active high CLAMP input pin. Typically, CLAMPing occurs just after the HSYNC signal goes active. However, with the externally input CLAMP signal, any area where the incoming video is at the black level may be used.

1.9 Analog Amplifiers

The ICS1532 contains three independently controlled analog amplifiers that prepare the incoming analog inputs to be converted by the ADC. These amplifiers have programmable gain and are to be adjusted by the system so that the analog output code range is as wide as practically possible.

1.10 Digital to Analog Converters

The Clamped output of the ICS1532's Analog Amplifiers is sent to the ADC's to convert the analog input's into digital equivalents.

1.11 I²C Bus Serial Interface

The ICS1532 uses a 5 Volt tolerant, industry-standard I²C-bus serial interface that runs at either low speed (100 kHz) or high speed (400 kHz). The interface uses 4 banks of indexed registers: there are write-only, read/write, and read-only registers.

Two ICS1532 devices can be addressed, according to the state of the I2CADR pin. When this pin is low, the read address is 49h, and the write address is 48h. When the pin is high, the read address is 4Bh, and the write address is 4Ah. See Chapter 10, "Programming"

1.12 Digital Inputs

All of the ICS1532's digital inputs are 5 V-tolerant.

1.13 Digital Data Outputs

The ICS1532 uses slew controlled CMOS outputs and are designed to be connected directly to the scaler or data transmitter inputs with no series resistors.

1.14 Automatic Power-On Reset Detection

The ICS1532 has automatic power-on reset detection (POR) circuitry and it resets itself if the supply voltage drops below ~1.8 VDC. No external connection to a reset signal is required and it may be, but a active low RESET# input is also provided and may be held low for ~10ms to reset the ICS1532.

1.15 Two Spread Spectrum Utility PLLs

Besides the Main, pixel clock PLL, the ICS1532 has two other independent PLLs for use as needed. Typically, these PLLs are used to drive memory and panel data clocks. Both of these additional PLLs are tailored for the required frequency ranges. Each supports software-controlled spread-spectrum clock dithering to reduce measured electro-magnetic interference (EMI).

1.16 Programmable Outputs

For general-purpose outputs, the ICS1532 provides programmable pins PSEL3, PSEL2, and PSEL1 (Reg 37:2-0).

Chapter 2   Pin Diagram and Listings

Figure 2-1.   Pin Diagram
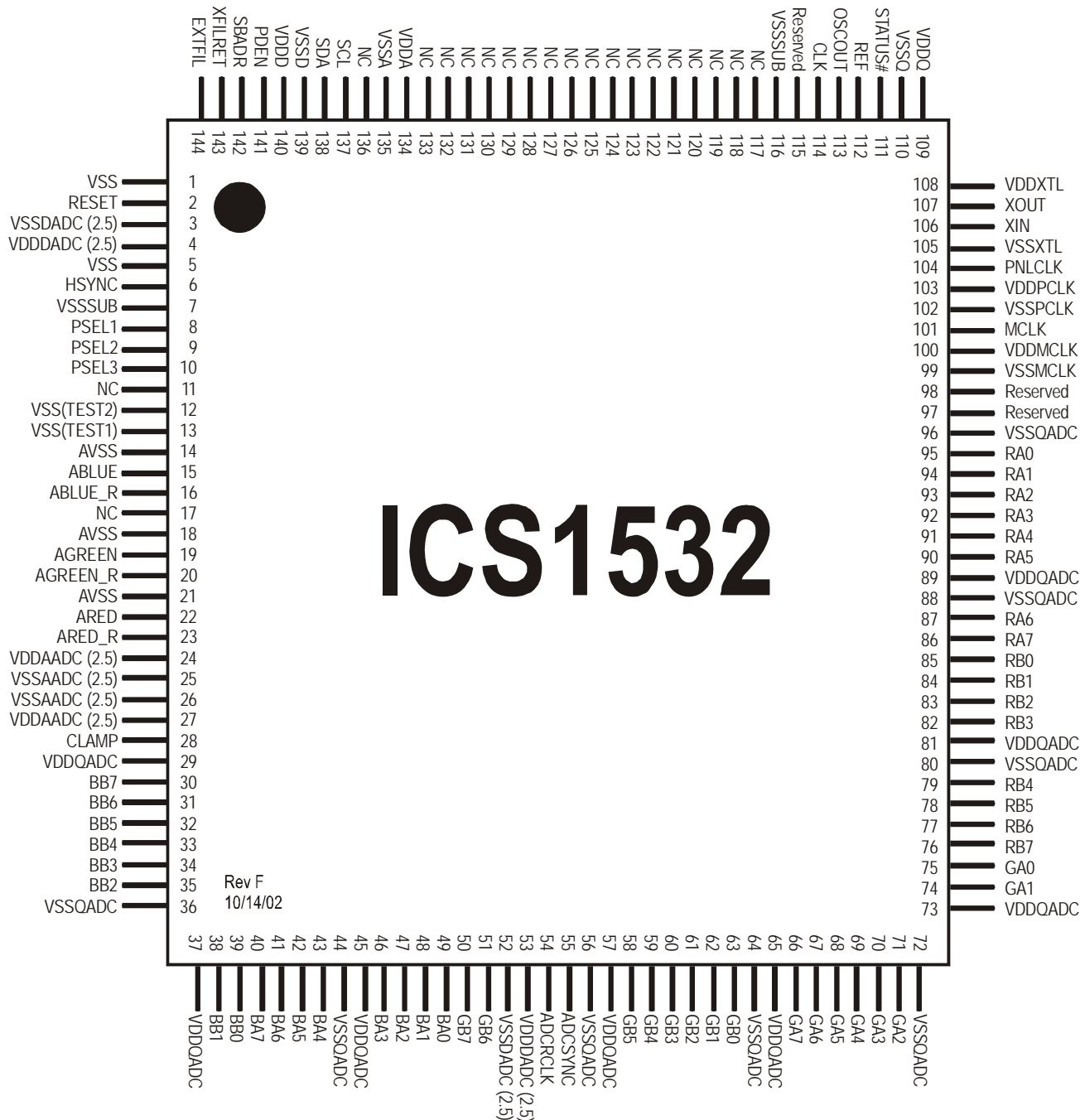
2.0.1 Pin Listing by Functional Grouping

Table 2-1. **Pin Listing by Functional Group**

Pin Group	Pin Name	Pin Type	Pin Description	Pin #
Clock In	CLAMP	Input	**External CLAMP input -** Optional	**28**
Clock In	HSYNC	Input	**Horizontal Sync Input**	**6**
Clock In	XIN	Input	**Crystal Input -** Connect 14.31818 MHz, 20pF, parallel resonance crystal or and external 14.31818-MHz clock source	**106**
Clock Out	ADCRCLK	Output	**Analog-to-Digital Converter Reference Clock** • Half-rate pixel clock for latching digital output pixel data.	**54**
Clock Out	ADCSYNC	Output	**Analog-to-Digital Converter Sync** • Recovered HSYNC output. Latch with ADCRCLK.	**55**
Clock Out	CLK	Output	**Full Rate Pixel Clock to ADC Section** • Normally not used. See ADRCRCLK	**114**
Clock Out	MCLK	Output	**Memory Clock -** Independent user-programmable clock source #1	**101**
Clock Out	OSCOUT	Output	**Oscillator Output -** Native Oscillator or Divided Oscillator Output	**113**
Clock Out	PNLCLK	Output	**Panel Clock -** Independent user-programmable clock source #2	**104**
Clock Out	REF	Output	**Reference -** Various reference line clock sync signals.	**112**
Clock Out	XOUT	Output	**Crystal Output -** Connect to the crystal above or leave open	**107**
Control In	SCL	Input	**Serial Clock for I^{2}C -** 5-V tolerant input clock from an I^{2}C bus	**137**
Control In	SBADR	Input	**I^{2}C Serial Bus Address** – Low, address is 49h for reads and 48h for writes – High, address is 4Bh for reads and 4Ah for writes	**142**
Control In	RESET	Input	**RESET Input -** Optional – Low - Device held in RESET state – High - Normal Operation -Pull high if unused	**142**
Control I/O	SDA	I/O	**Serial Data -** 5-V tolerant pin data pin for an I^{2}C bus	**138**
Control Out	PSEL1 - 3	Output	**Programmable Outputs** See Register 37h.	**8, 9, 10**
Analog Input	BLUE, GREEN, RED	Input	**Analog Blue, Green and Red Inputs** • Accepts analog data for the ADCs blue, green, and red converters	**15, 19, 22**
Analog Input	ABLUE_R AGREEN_R ARED_R	Input	**Analog Blue, Green and Red Signal Returns** • These pins provide a return path for the analog input data	**16, 20, 23**
Data Output	BA7 – BA0, GA7 – GA0, RA7 – RA0	Output	**Blue 'A' 7–0, Green 'A' 7–0, and Red 'A' 7–0.** • Output first blue, green, and red digital pixel data, respectively. • A7 = MSB	**See Figure 2-1**
Data Output	BB7 – BB0, GB7 – GB0, RB7 – RB0	Output	**Blue 'B' 7–0, Green 'B' 7–0, and Red 'B' 7–0.** • Outputs second blue, green, and red digital pixel data, respectively. • A7 = MSB	**See Figure 2-1**
Clock In	EXTFIL	Input	**External Filter-**Optional external filter input between self and XFILRET	**144**
Clock In	PDEN/COAST	Input +5	**Phase-Detector Enable -** Can disable the charge pump with Reg 0:1-0	**141**

Table 2-1. **Pin Listing by Functional Group** (*Continued*)

Pin Group	Pin Name	Pin Type	Pin Description	Pin #
Clock In	STATUS#	Output	**Status -** Active-low when locked pin works with Reg 2C:1-0	**111**
Clock In	XFILRET	Input	**External Filter Return. -** External filter input between self and EXTFIL	**143**
Ground	AVSS	Ground	**Main Analog Ground -** Connect to the common ground plane	**14, 18, 21**
Ground	VSS	Ground	**Main PLL Ground -** Connect to the common ground plane	**1 & 5**
Ground	VSSA	Ground	**Main PLL Analog Ground -** Connect to the common ground plane	**135**
Ground	VSSAADC(2.5)	Ground	**Analog ADC Ground -** Ground for 2.5 volt analog portions of the ADC • Connect to the common ground plane	**25 & 26**
Ground	VSSD	Ground	**Digital Ground -** Connect to the common ground plane	**139**
Ground	VSSDADC(2.5)	Ground	**Digital ADC Ground -** Ground for 2.5 volt digital portions of the ADC • Connect to the common ground plane	**3, 52**
Ground	VSSMCLK	Ground	**MCLK PLL Ground -** Connect to the common ground plane	**99**
Ground	VSSPCLK	Ground	**PNLCLK PLL Ground -** Connect to the common ground plane	**102**
Ground	VSSQ	Ground	**Main PLL Output Ground -** Connect to the common ground plane	**110**
Ground	VSSQADC	Ground	**Pixel Data Output Driver Ground** • Connect to the common ground plane	**36, 44, 56, 64, 72, 80, 88, 96**
Ground	VSSSUB	Ground	**Ground for Substrate -** Connect to the common ground plane	**7, 116**
Ground	VSSTEST2 VSSTEST1	Ground	**Ground or Test Outputs -** Connect to the common ground plane	**12, 13**
Ground	VSSXTL	Ground	**Crystal Oscillator Ground -** Connect to the common ground plane	**105**
Power	VDDA	3.3	**(3.3 V) Supply for Analog Pixel PLL Circuitry**	**134**
Power	VDDAADC(2.5)	2.5	**(2.5 V) Supply for Analog ADC Circuitry**	**24 & 27**
Power	VDDD	3.3	**(3.3 V) Supply for Main PLL and I²C Bus**	**140**
Power	VDDDADC(2.5)	2.5	**(2.5 V) Supply for Digital ADC Circuitry**	**4, 53**
Power	VDDMCLK	3.3	**(3.3 V) Supply for MCLK**	**100**
Power	VDDPCLK	3.3	**(3.3 V) Supply for PNLCLK**	**103**
Power	VDDQ	3.3	**(3.3 V) Supply for Output Drivers**	**109**
Power	VDDQADC	3.3	**(3.3 V) Supply for Pixel Data Output Drivers**	**29, 37, 45, 57, 65, 73, 81, 89**
Power	VDDXTL	3.3	**(3.3V) Supply for Crystal Oscillator**	**108**
NC	No Connect	**NC**	**No Connect -** Do not connect these pins.	**11, 17, 117 - 133, 136**
Reserved	Reserved	**RES.**	**Reserved -** Do not connect these pins.	**97, 98**

Chapter 3   Functional Blocks

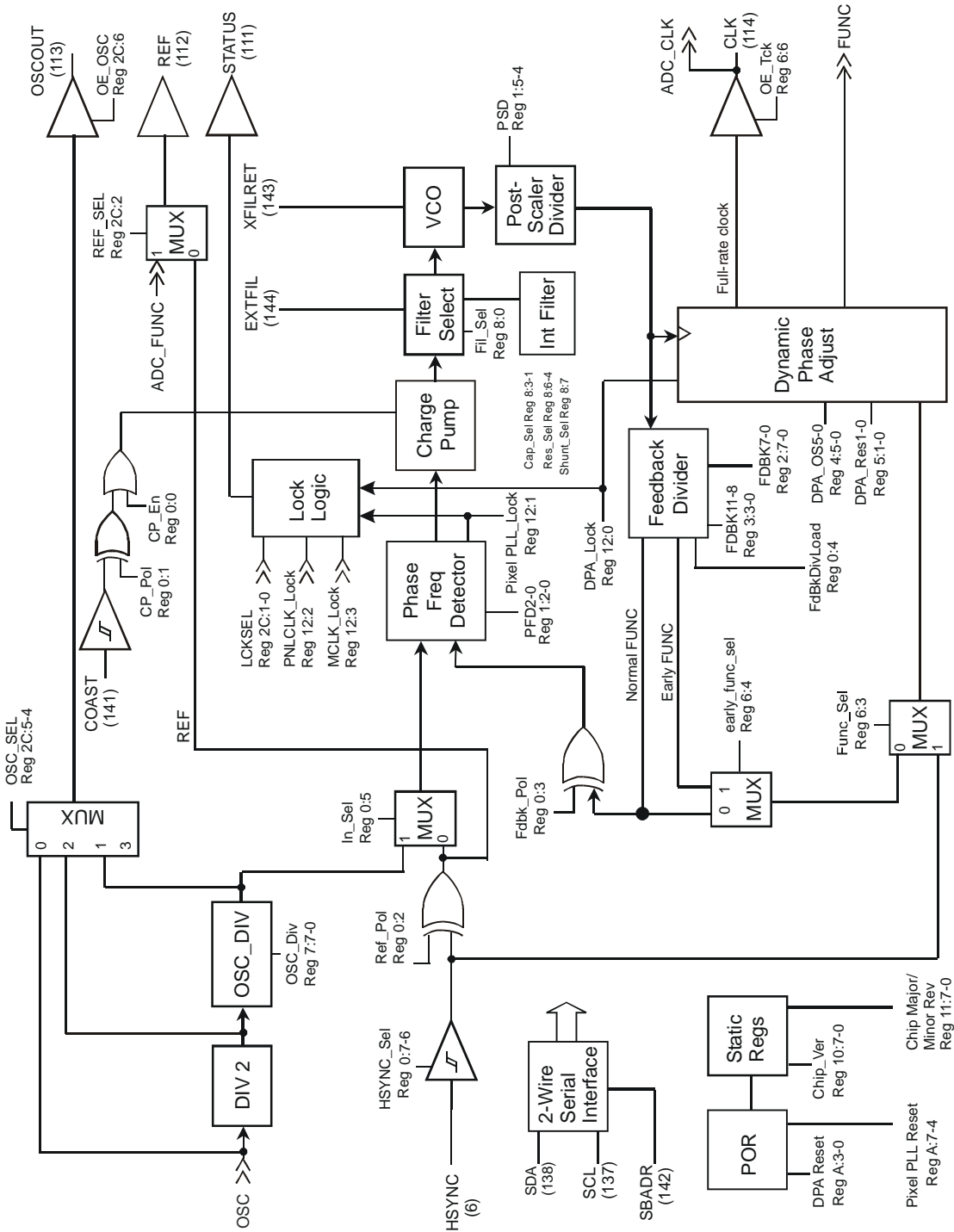**Figure 3-1.   Pixel PLL Block Diagram**
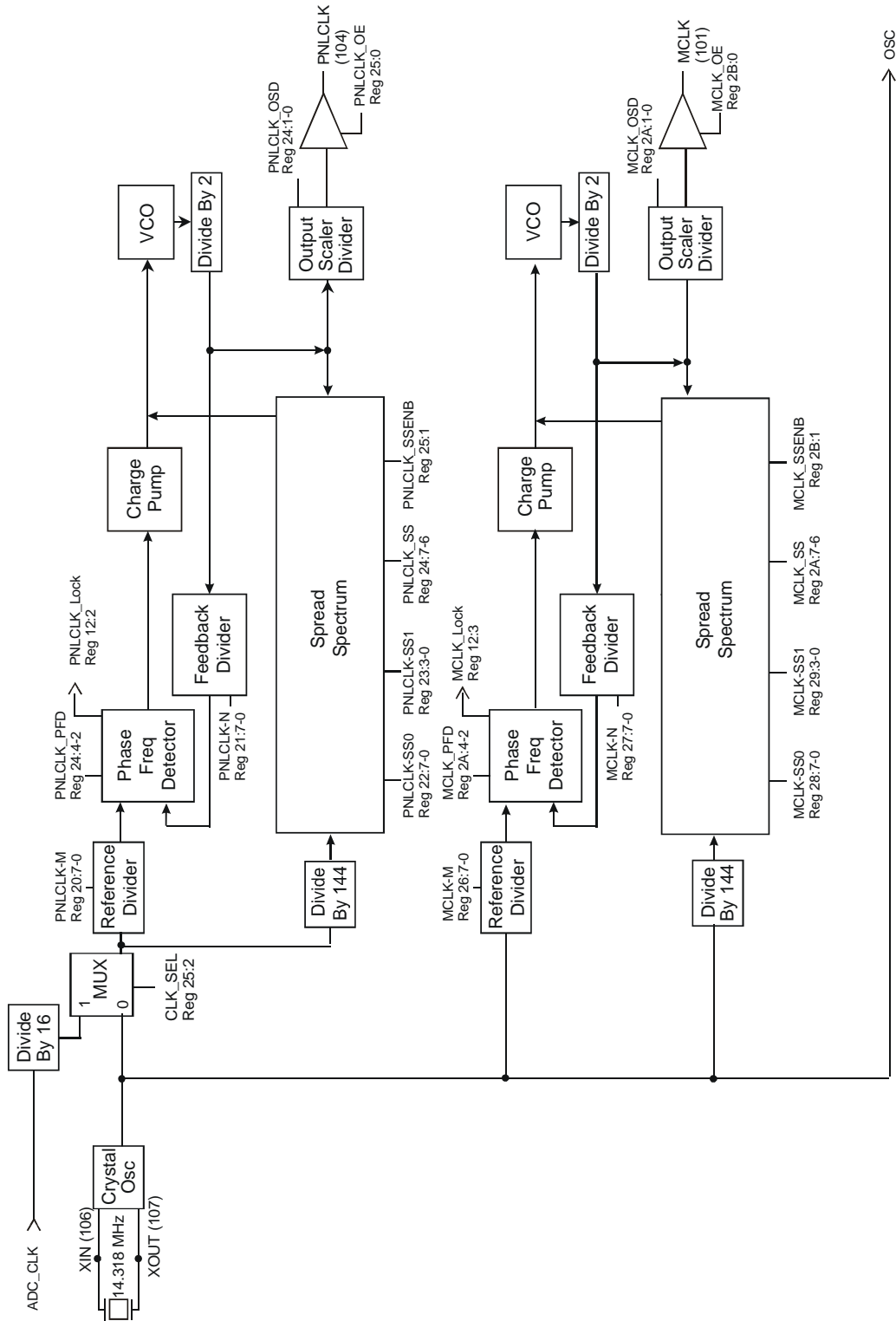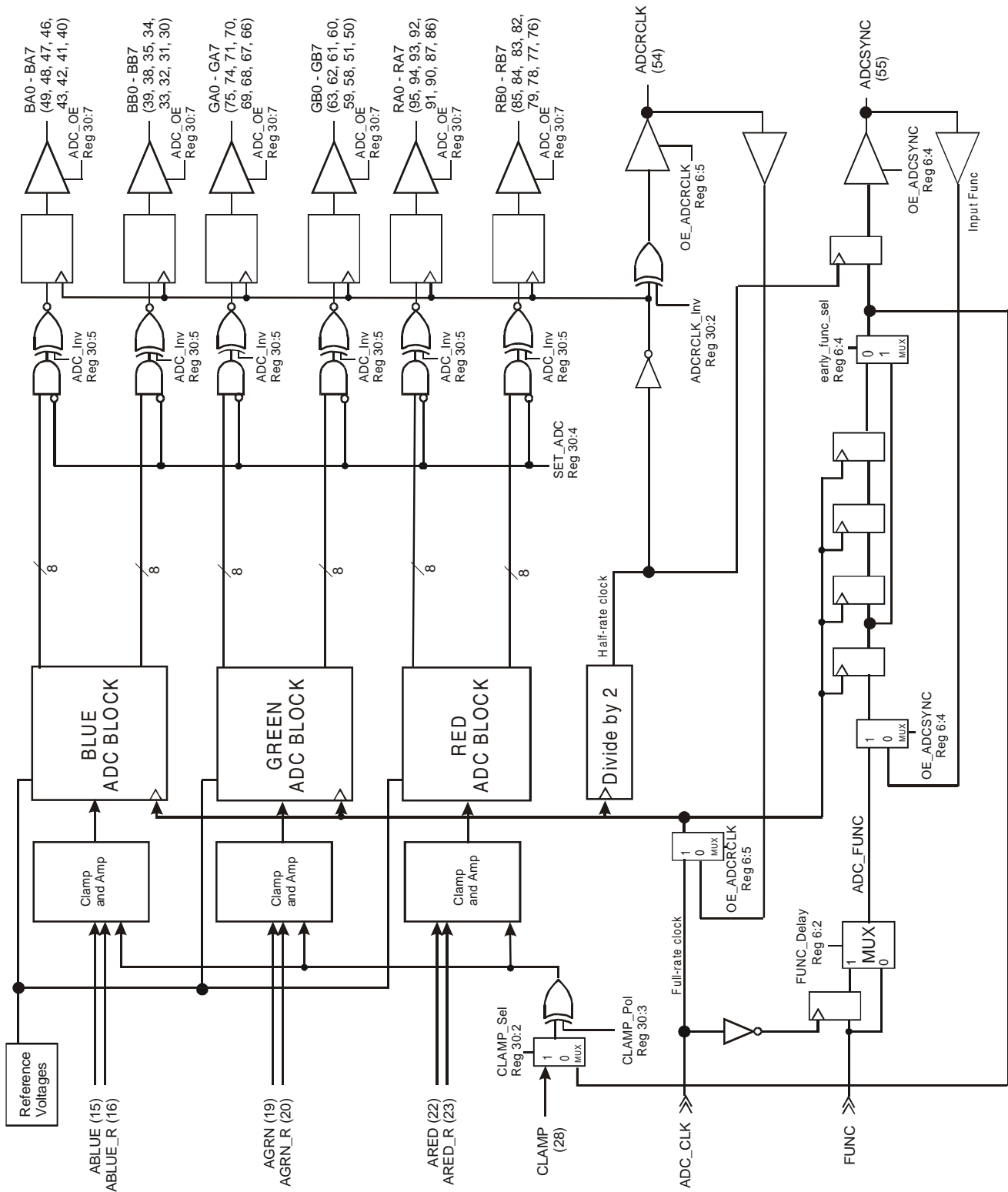
Figure 3-2.   CLK Block Diagram

Figure 3-3.   ADC Block Diagram

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Chapter 4   Register Set

The tables in this chapter detail the functionality of the ICS1532 Register Set bits. The tables include the register locations, the bit positions, names, and definitions, along with their read/write access, reset values, and any special functions or capabilities.

4.1   Reserved Bits

The ICS1532 has a number of reserved bits throughout the Register Set. These bits provide enhanced test functions (intended for use only by ICS manufacturing) and calibration functions (intended for use in production environments).

Important: The customer must not change the value of reserved bits. If the customer changes the default values of these reserved bits, normal operation of the ICS1532 can be affected.

4.2   Register Set Conventions

Register Set conventions include the following:

- An "#" on the end if a register bit or pin name indicates active low. (Low = True, High = False)
- Bits are listed in the order of most-significant bit (MSB) to least-significant bit (LSB).
- Unless otherwise indicated, bit settings are listed in terms of digital (and not hexadecimal) values.
- When a bit definition includes word(s) in parentheses, the word in parenthesis is not part of the bit name, but is given to explain the origin of the bit's name.

4.3   Register Set Abbreviations and Acronyms

Table 4-1 lists and defines abbreviations and acronyms used specifically in this chapter.

Table 4-1.   Register Set Abbreviations and Acronyms
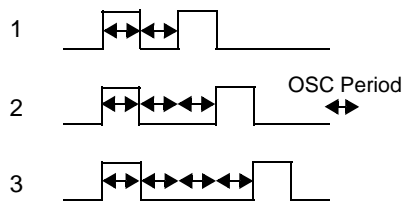
Abbreviation or Acronym	Definition
D-DPA	**Double-Buffered / Dynamic Phase Adjust.** Indicates double-buffered registers for which working registers load during a software Dynamic Phase Adjust reset. (RegA = xAh)
D-MK	**Double-Buffered / Memory Clock.** Indicates double-buffered registers for which working registers load during a software MCLK reset. (Reg2D = 5xh)
D-PK	**Double-Buffered / Panel Clock.** Indicates double-buffered registers for which working registers load during a software PNLCLK reset. (Reg2D = xAh)
D-PLL	**Double-Buffered / Phase-Locked Loop.** Indicates double-buffered registers for which working registers load during a software pixel PLL reset. (RegA = 5xh)
IN-A	**Increment All.** Indicates a value that increments with each all-layer revision of the ICS1532.
Reg	**Register**
R/W	**Read/Write**

4.4   Complete Register Set

Table 4-2.   New Register Set Outline

Register Index	Register Name	Register Access	Bit #	Bit Name	Brief Description	Reset Value
00h	Input Control	R/W	7-6	HSYNC_Sel	Select HSYNC Input Threshold for Main PLL – See **Chapter 11-3, "Pin Specific I/O AC Parameters"**	0
			5	In_Sel	Select Main PLL Phase Detector Input – 0 = HSYNC source selected by Reg0:7-6 – 1 = Input is the OSC pin	1
			4	Fdbk Div Load	Select load for Feedback Divider – 0 = New values loaded on a pixel PLL reset.-(Normal Operation) – 1 = New values loaded on the HSYNC without a PLL reset - Only usable for small changes	0
			3	Fdbk_Pol	Select feedback polarity for Phase/Frequency Detector – 0 = Main/Pixel PLL uses the rising edge – 1 = Main/Pixel PLL uses the falling edge	0
			2	Ref_Pol	Select polarity of external reference – 0 = Rising HSYNC Edge Selected – 1 = Falling HSYNC Edge Selected	0
			1	CP_Pol	Select polarity of COAST Input if Reg0:0=1 – 0 = Charge Pump enabled if COAST pin high – 1 = Charge Pump enabled if COAST pin low	0
			0	CP_En	Charge Pump (CP) Enable – 0 = CP enabled by Reg0:1 and COAST – 1 = CP always Enabled - Normal Operation	1
01h	Loop Control	R/W. D-PLL.	7-6	Reserved	Reserved	0
			5-4	VCOS	Select VCO Scaler Value VCO frequency = (Output frequency) * VCOS(d) – 00 = 2:1 – 01 = 4:1 – 10 = 8:1 – 11 = 16:1	0
			3	Reserved	Reserved	0
			2-0	ICP	ICP - Charge Pump Current – 000 = ~2 μA – 001 = ~4μA – 010 = ~8μA (Typical with Internal Filter) – 011 = ~16μA. – 100 = ~32μA – 101 = ~64μA – 110 = ~120μA. – 111 = ~190μA	0
02h	Fdbk Div 0	R/W. D-PLL.	7-0	FDBK [7-0]	Feedback Divider LSB's bits 7-0 - See Reg3 for MSB's – Controls the number of CLK outputs per HSYNC – Actual # of CLK's = 8 + (Reg3 + Reg2)d	N/A
03h	Fdbk Div 1	R/W. D-PLL.	7-4	Reserved	Reserved	–
			3-0	FDBK [11-8]	Feedback Divider MSB's bits 11-8 - See Reg2	N/A
04h	DPA Offset	R/W	7-6	Reserved	Reserved	0
			5-0	DPA_OS	Dynamic Phase Adjust (DPA) Offset – *See Chapter 5, "DPA Operation"* The value programmed here must be less than the DPA Resolution controlled by Reg5:1-0	0

Table 4-2. New Register Set Outline (*Continued*)

Register Index	Register Name	Register Access	Bit #	Bit Name	Brief Description	Reset Value
05h	DPA Control	R/W. D-DPA.	7-2	Reserved	Reserved	–
			1-0	DPA_Res	DPA resolution (Number of available Delay Elements) **See Chapter 5, "DPA Operation"** – 00 = 16 elements - supports 55 to 110 MHz – 01 = 32 elements - supports 27 to 110 MHz – 10 = Reserved – 11 = 64 elements - supports 14 to 64 MHz	N/A
06h	Output Enables	R/W	7	Reserved	Reserved	0
			6	OE_TCLK	Enable CLK output to ADC and CLK pin 1 = MUST be Enabled for Normal Operation	0
			5	OE_ADCRCLK	Enable ADCRCLK clock output	0
			4	OE_ADCSYNC	Enable output for ADCSYNC	0
			3	FUNC_Sel	Select signal source for ADC_FUNC signal 0 = Output of the Feedback Divider - Normal Operation 1 = ADC_FUNC output is REF	0
			2	FUNC_Delay	Additional one CLK delay for ADC_FUNC signal	0
			1	Reserved	Reserved	0
			0	Reserved	Reserved	0
07h	OSC Divider	R/W	7-0	OSC_Div	Oscillator divider value – 00000000 = Reserved. – 00000001 = (OSC / 2) – 00000010 = (OSC / 2) / 2 – 00000011 = (OSC / 2) / 3, and so forth.	0
08h	Internal Filter	R/W	7	Shunt_Sel	Select additional Cp capacitor	1
		Values?	6-4	Res_Sel	Select additional Rs resistance	7
		Values?	3-1	Cap_Sel	Select additional Cs capacitance	7
			0	Fil_Sel	Selects Loop Filter Select 1 = Internal (Typical) 0=External	1
09h	Reserved					N/A
0Ah	Pixel PLL/ DPA Resets	Write	7-4	Pixel PLL Reset	Writing 5xh resets pixel PLL and loads working Regs 1h through 3h	N/A
			3-0	DPA Reset	Writing xAh resets DPA and loads working Reg 5h	N/A
0Bh-0Fh	Reserved					N/A
10h	Chip Ver	Read	7-0	Chip Ver	Read chip version 32 decimal (20h) as in 1532	20
11h	Chip Rev	Read. IN-A.	7-4	Chip Major Rev	Value increments with major chip revision.	01

The OSC_Div register entry (07h) includes timing diagrams labeled 1, 2, and 3, with an "OSC Period" marker.

Table 4-2. New Register Set Outline (*Continued*)

Register Index	Register Name	Register Access	Bit #	Bit Name	Brief Description	Reset Value
			3-0	Chip Minor Rev	Value increments with minor chip revision.	00
12h	Rd_Reg	Read	7-4	Reserved	Reserved	N/A
			3	PLL_Lock	Pixel PLL lock status - 1 = Locked, 0 = Unlocked	N/A
			2	MCLK_Lock	Memory MCLK lock status - 1 = Locked, 0 = Unlocked	N/A
			1	PCLK_Lock	Panel PLL lock status - 1 = Locked, 0 = Unlocked	N/A
			0	Reserved	Reserved	N/A
13h-1Fh	Reserved					N/A
20h	PNLCLK-M	R/W. D-PK.	7-0	PNLCLK_M	Select value for PNLCLK M Reference Divider	0
21h	PNLCLK-N	R/W. D-PK.	7-0	PNLCLK_N	Select value for PNLCLK N Feedback Divider $F_{PNLCLK} = (OSC \times (N + 8)) / (M+2)$	0
22h	PNLCLK-SS0	R/W. D-PK.	7-0	PNLCLK_SS0	Value for PNLCLK spread-spectrum counter LSB's bits 7-0 - Controls amount of frequency spread Allowed Values = (288 *N / M) $\pm$ 8	0
23h	PNLCLK-SS1	R/W. D-PK.	7-4	Reserved	Reserved	0
			3-0	PNLCLK_SS1	Value for PNLCLK spread-spectrum counter MSBs bits 11-8 See Reg22	0
24h	PNLCLK-SSOE	R/W. D-PK.	7-6	PNLCLK_SS	Select PNLCLK spread-spectrum gain – 0 = The gain is 1 – 1 = The gain is 2 – 2 = The gain is 4 – 3 = The gain is 8	0
			5	Reserved	Reserved	0
			4-2	PNLCLK_PFD	PNLCLK Phase/Frequency Detector gain – 000 = Gain is 1 – 001 = Gain is 2 – 010= Gain is 4 – 011 = Gain is 8, and so forth... – 111 = Gain is 128	0
			1-0	PNLCLK_OSD	PNLCLK Output Scaler Divider – 00 = Divide by 1 – 01 = Divide by 2 – 10= Divide by 4 – 11 = Divide by 8	0
25h	PNLCLK-OE	R/W	7-3	Reserved	Reserved	11100
			2	CLK_SEL	Select input for PNLCLK PLL – 0 = PNLCLK PLL input is from the crystal input – 1 = Input is from ADC_CLK, divided by 16	0
			1	PNLCLK_SSENB	Enable PNLCLK spread-spectrum	0
			0	PNLCLK_OE	Enable PNLCLK output	0
26h	MCLK-M	R/W. D-MK.	7-0	MCLK_M	Value for MCLK M Feedback Divider	0
27h	MCLK-N	R/W. D-MK.	7-0	MCLK_N	Value for MCLK N (Numerator) Feedback Divider $F_{MCLK} = (OSC \times (N + 8)) / (M+2)$	0

Table 4-2. New Register Set Outline (*Continued*)

Register Index	Register Name	Register Access	Bit #	Bit Name	Brief Description	Reset Value
28h	MCLK-SS0	R/W. D-MK.	7-0	MCLK_SS0	Select MCLK spread-spectrum counter LSB's bits 7-0 See Reg29 - Controls amount of frequency spread Allowed Values = (288 *N / M) ± 8	0
29h	MCLK-SS1	R/W. D-MK.	7-4	Reserved	Reserved	1010
			3-0	MCLK_SS1	Select MCLK spread-spectrum counter MSBs bits 11-8 See Reg28	0
2Ah	MCLK-SSOE	R/W. D-MK.	7-6	MCLK_SS	Select MCLK spread-spectrum gain – 00 = The gain is 1 – 01 = The gain is 2 – 10 = The gain is 4 – 11 = The gain is 8	0
			5	Reserved	Reserved	0
			4-2	MCLK_PFD	Select MCLK Phase/Frequency Detector gain – 000 = Gain is 1 – 001 = Gain is 2 – 010 = Gain is 4 – 011 = Gain is 8 – 100 = Gain is 16, and so forth...	0
			1-0	MCLK_OSD	Select value for MCLK Output Scaler Divider – 00 = Divide by 1 – 01 = Divide by 2 – 10 = Divide by 4 – 11 = Divide by 8	0
2Bh	MCLK-OE	R/W	7-2	Reserved	Reserved	010000
			1	MCLK_SSENB	Enable MCLK spread-spectrum (1 = Enabled)	0
			0	MCLK_OE	Enable MCLK output (1 = Enabled)	0
2Ch	OUTPUT MUX	R/W	7	High_Drive#	Disable high drive for ADC pixel data output pins	0
			6	OE_OSC	Enable OSCOUT output pin (1 = Enabled)	1
			5-4	OSC_Sel	Select OSCOUT Output – 00 = OSCOUT source is OSC. – 01 = OSCOUT source is OSCDIVIDER (Reg7) – 10 = OSCOUT source is OSC/2. – 11 = Reserved	0
			3	Reserved	Reserved	0
			2	REFSEL	Select REF status	0
			1-0	LCKSEL#	Select active low output for STATUS (pin 111) Low when selection below is properly locked, else high – 00 = Main Pixel PLL – 01 = MCLK: Memory Clock – 10 = Reserved – 11 = PNLCLK: Panel Clock	1
2Dh	PLL Reset	Write	7-4	MCLK_Reset	Writing 5xh resets MCLK PLL & loads Regs 26h~2Bh	N/A
			3-0	PNLCLK_Reset	Writing xAh resets PNLCLK PLL & loads Regs 20~25h	N/A
2Eh-2Fh	Reserved					N/A
30h	ADC CTRL	R/W	7	ADC_OE	Enable ADC output (1 = Enabled)	0
		??????	6	ADC_Inv	Invert ADCRCLK signal (1=Latch data on rising edge)	0
			5	Force_ADC	Force ADC Outputs to state of Reg30:3	1

Table 4-2. New Register Set Outline (*Continued*)

Register Index	Register Name	Register Access	Bit #	Bit Name	Brief Description	Reset Value
		??????	4	ADC_Clock_D	ADC clock state delay (1 = ?????)	0
			3	ADC_Inv	Invert ADC Outputs (1- White = FF, 0 - White = 00)	0
			2	CLAMP_Sel	Clamp Select – 00 = External CLAMP (pin 28) – 10 = Internal CLAMP (same as FUNC)	0
			1	Reserved	Reserved	0
			0	CLAMP_Pol	Polarity of Clamping Control Signal 0 = Active High Clamp (Normal operation) 1 = Active Low Clamp	0
31h	R_Control	R/W	7	R_VIN_Range	Red Input Voltage Range (0=700mv, 1=1V)	1
			6	Reserved	Reserved	0
		????	5	R_CLAMP_T3	Red Clamp Time Constant (0= Nom., 1=0.3 Nom.)	0
		????	4	R_CLAMP_Type	Soft/Xhard Clamp Function	1
		????	3	R_CLAMP_T5	Red Clamp Time Constant (0= Nom., 1=0.5 Nom.)	0
			2-1	Reserved	Reserved	1
			0	XPD_R#	Power Down Red Channel (0=Powered Down)	1
32h	G_Control	R/W	7	G_Fixed_Gain	Green Gain Adjust. (0=100%, 1=140%)	1
			6	Reserved	Reserved	0
		????	5	G_CLAMP_T3	Green Clamp Time Constant (0= Nominal, 1=0.3 Nom.)	0
		????	4	G_CLAMP_Type	Green Soft/Xhard Clamp Function	1
		????	3	G_CLAMP_T5	Green Clamp Time Constant (0= Nominal,1=0.5 Nom.)	0
			2	Reserved	Reserved	1
			1	SOG	Sync On Green	0
			0	XPD_G#	Power Down Green Channel (0=Powered Down)	1
33h	B_Control	R/W	7	B_Fixed_Gain	Blue Gain Adjust. (0=100%, 1=140%)	1
			6	Reserved	Reserved	0
		????	5	B_CLAMP_T3	Blue Clamp Time Constant (0= Nominal, 1=0.3 Nom.)	0
		????	4	B_CLAMP_Type	Blue Soft/Xhard Clamp Function	1
		????	3	B_CLAMP_T5	Blue Clamp Time Constant (0= Nominal,1=0.5 Nom.)	0
			2-1	Reserved	Reserved	0
			0	XPD_B#	Power Down Blue Channel (0=Powered Down)	1
34h	R_Gain	R/W	7-3	R_PGA_Gain	Fine adjust red channel ADC ladder voltage	00100
			2-0	R_ADC_Gain	Adjust Video Amp Gain for red channel of ADC	000
35h	G_Gain	R/W	7-3	G_PGA_Gain	Fine adjust green channel ADC ladder voltage	00100
			2-0	G_ADC_Gain	Adjust Video Amp Gain for green channel of ADC	000
36h	B_Gain	R/W	7-3	B_PGA_Gain	Fine adjust blue channel ADC ladder voltage	00100
			2-0	B_ADC_Gain	Adjust Video Amp Gain for blue channel of ADC	000
37h	PSEL	R/W	7-4	BG_CAL	Band Gap Calibration (0=Normal Operation)	0
			3	XBG_PD#	Band Gap Power Down (0=Powered Down)	1
			2	PSEL3	State of PSEL3 (pin 10)	0
			1	PSEL2	State of PSEL2 (pin 9)	0
			0	PSEL1	State of PSEL1 (pin 8)	0
38h	R_Offset		7-0	R_Offset	Red channel offset (00=minimum offset)	80h
39h	G_Offset		7-0	G_Offset	Green channel offset (00=minimum offset)	80h

Table 4-2. New Register Set Outline (*Continued*)

Register Index	Register Name	Register Access	Bit #	Bit Name	Brief Description	Reset Value
3Ah	B_Offset		7-0	B_Offset	Blue channel offset (00=minimum offset)	07h
3Bh	IBias		7-6	IBias_Buf	ADC Buffer Bias Adjustment	10
			5-4	IBias_VA	Video Amp Bias Adjustment	10
			3-0	IBias_ADC	ADC Bias Adjustment	1010
3Ch	Test_Mux		7-3	CTM	Channel Test Mux	1010
			2-0	BGTM	Band Gap Test Mux	1010

Chapter 5   DPA Operation

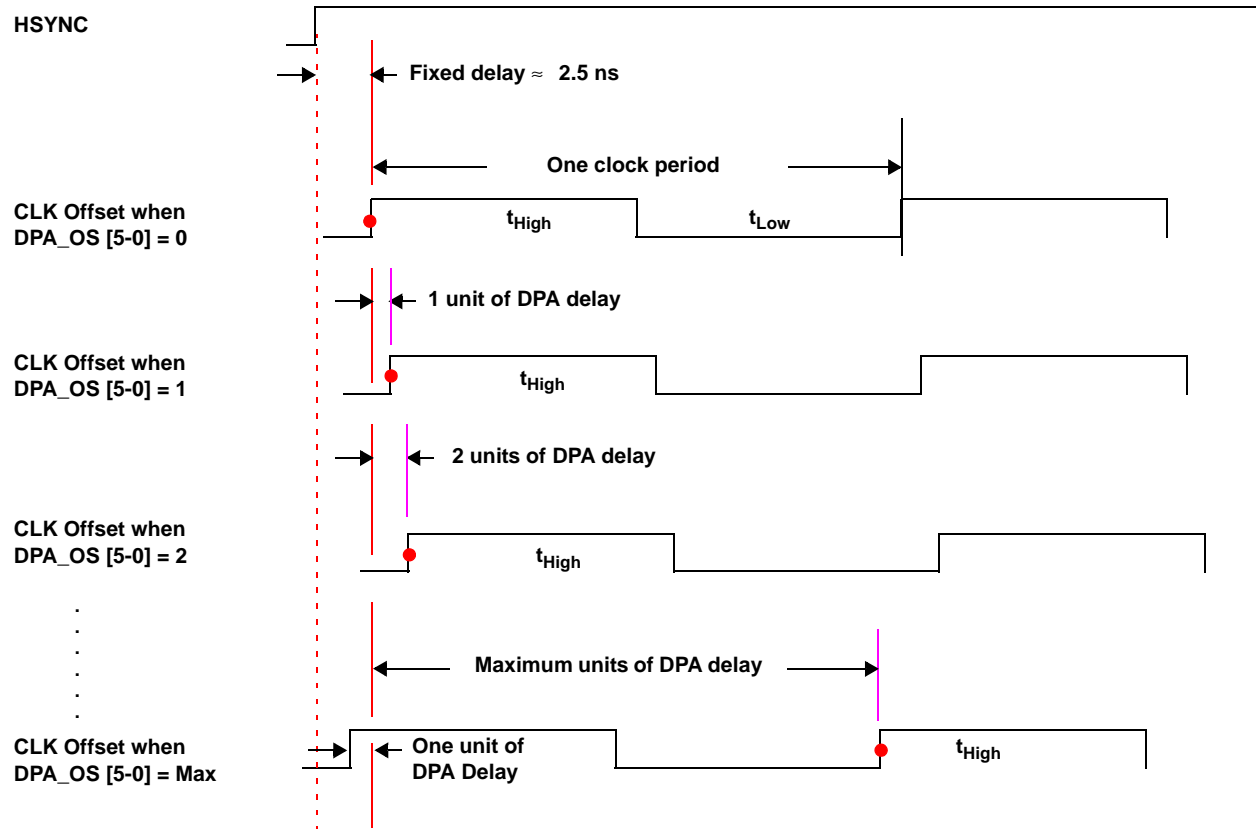**Figure 5-1.   DPA Offset (As Determined by Regs 04 and 05)**

Table 5-1.   DPA Control

Reg 05:1-0		1. Number of Delay Element Units (Decimal)	2. Reg 04:5-0 Max. Value (Hex)	3. Pixel Clock Range (MHz)
Bit 1	Bit 0			
0	0	16	0F	55 ▬▬▬ 110
0	1	32	1F	27 ▬▬▬▬▬ 110
1	0	Reserved	Reserved	
1	1	64	3F	14 ▬▬ 64

Chapter 6   OSC Divider & OSCOUT

The ICS1532 accepts either a crystal across XIN and XOUT or a single ended clock on the XIN input (with XOUT left open). See Table 11-4 for crystal requirements. This input (OSC) may be output to the OSCOUT pin at the same input frequency, half the input frequency, or divided by >2. This translates to OSC, OSC/2 and the OSC Divider and is selected by Register2C:5~4.

The OSC Divider works as follows, The period of the OSC input becomes the high time of the OSC_OUT signal and the low time is controlled by Register 7.

Table 6-1   OSC Divider Functionality

Parameter	Value
OSC Divider Frequency	(Input Osc Frequency) * [(Register 7: 6~0) + 2]
OSC High Time	Input OSC Period
OSC Low Time	[Reg7 + 1] * Input OSC Period
Minimum OSC Divider	3 (Reg7:6~0 = 0000001)
Maximum OSC Divider	257 (Reg7 = 1111 1111)
RESERVED OSC Divider	0 (Reg7 = 0000 0000)

Chapter 7   Loop Filter

The ICS1532 contains an internal loop filter and also supports the use of an external loop filter configured as in Figure 7-1. Selection between these two filters is controlled by Register 8:7. A 0 selects the external, a 1 selects the internal filter.

Figure 7-1   External Loop Filter
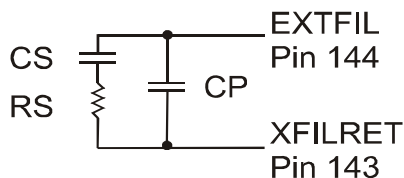
While the internal loop filter works well for most applications, IDT still recommends the implementation of an external filter network on all designs.

Implementing the external loop filter gives the system engineer flexibility to add external filter functionality if without having to alter the PCB.

Chapter 8   PLL Parameter Settings

Settings for all standard VESA video modes are provided by IDT as a starting point for the systems engineer. These files are in human readable text files (*.ics files) and come bundled within the ICS1532 Register Editor Tool.

This tool directly drives the ICS1532EB Evaluation Board and can be downloaded from www.idt.com.

Chapter 9   Input Termination

The ICS1532 is a high speed Analog to Digital converter capable of operating at 110 MSPS. Since VGA/VESA video is comprised of 700 mV vpp waveforms potentially toggling high speed, care needs to be taken to preserve the quality of these analog input signals from reflections and coupled noise all the way to the input pins of the ICS1532.

The R, G and B video inputs and their dedicated return signals must be…

- Routed as a clean, minimal length traces to minimize loading and pickup
- 75 Ohm characteristic impedance to eliminate reflections
- Appropriate signal pairs being located as close as possible to each other and far from noise sources
- Properly terminated as shown in Figure 9-1 with termination resistors placed as close to the ICS1532 as possible.
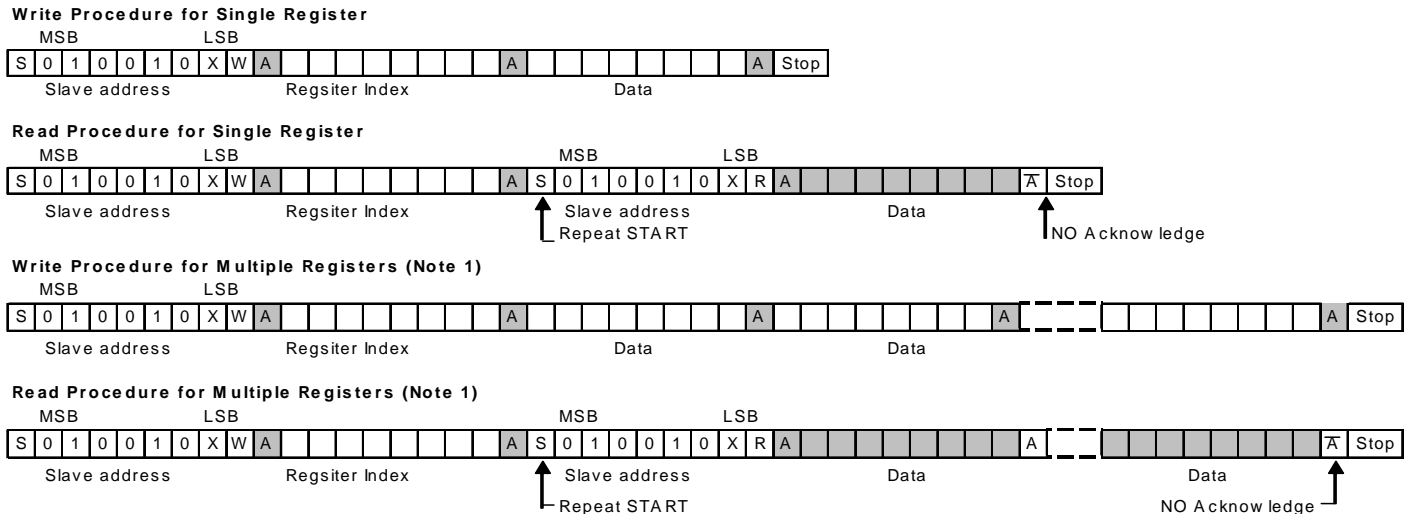
Figure 9-1.   Recommended Termination
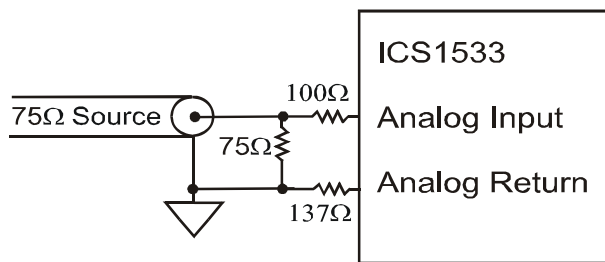
Chapter 10   Programming

10.1   I2C Serial Bus: Data Format

Figure 10-1.   ICS1532 Data Format for I2C Serial Bus

Write Procedure for Single Register

MSB   LSB

| S | 0 | 1 | 0 | 0 | 1 | 0 | X | W | A | | | | | | | | A | | | | | | | | A | Stop |

Slave address   Regsiter Index   Data

Read Procedure for Single Register

MSB   LSB   MSB   LSB

| S | 0 | 1 | 0 | 0 | 1 | 0 | X | W | A | | | | | | | | A | S | 0 | 1 | 0 | 0 | 1 | 0 | X | R | A | | | | | | | | A̅ | Stop |

Slave address   Regsiter Index   ↑ Slave address   Data   ↑ NO Acknowledge
                                        └ Repeat START

Write Procedure for Multiple Registers (Note 1)

MSB   LSB

| S | 0 | 1 | 0 | 0 | 1 | 0 | X | W | A | | | | | | | | A | | | | | | | | A | | | | | | | | A | Stop |

Slave address   Regsiter Index   Data   Data

Read Procedure for Multiple Registers (Note 1)

MSB   LSB   MSB   LSB

| S | 0 | 1 | 0 | 0 | 1 | 0 | X | W | A | | | | | | | | A | S | 0 | 1 | 0 | 0 | 1 | 0 | X | R | A | | | | | | | | A | | | | | | | | A̅ | Stop |

Slave address   Regsiter Index   ↑ Slave address   Data   Data
                                        └ Repeat START   NO Acknowledge ↑

Legend

All values are sent with the most-significant bit (MSB) first and least-significant bit (LSB) last.
R = Read = 1
W = Write = 0
S = Start (SDA goes low when SCL was high, then SCL goes low too)
A = ACK = Acknowledge = 0
A̅ = NAK = No Acknowlege = 1
X = Bit value that equals logic state of SBADR pin.

- - - = (Dashed Line) Multiple transactions

☐ Bus Master drives signal to ICS1532   ▨ ICS1532 (Slave Device) drives signal to Bus Master

Note: In general, the:

- Lower nibble of the I^{2}C register automatically increments after each successive data byte is written to or read from the ICS1532.

- Upper nibble of the I^{2}C register does not automatically increment, and the software must explicitly re-address the ICS1532. As a result, to write or read all the ICS1532 registers, the software:
  – Must NOT index 0 and then do 64 one-byte transactions.
  – Must break the transactions into at least four separate bus transactions:
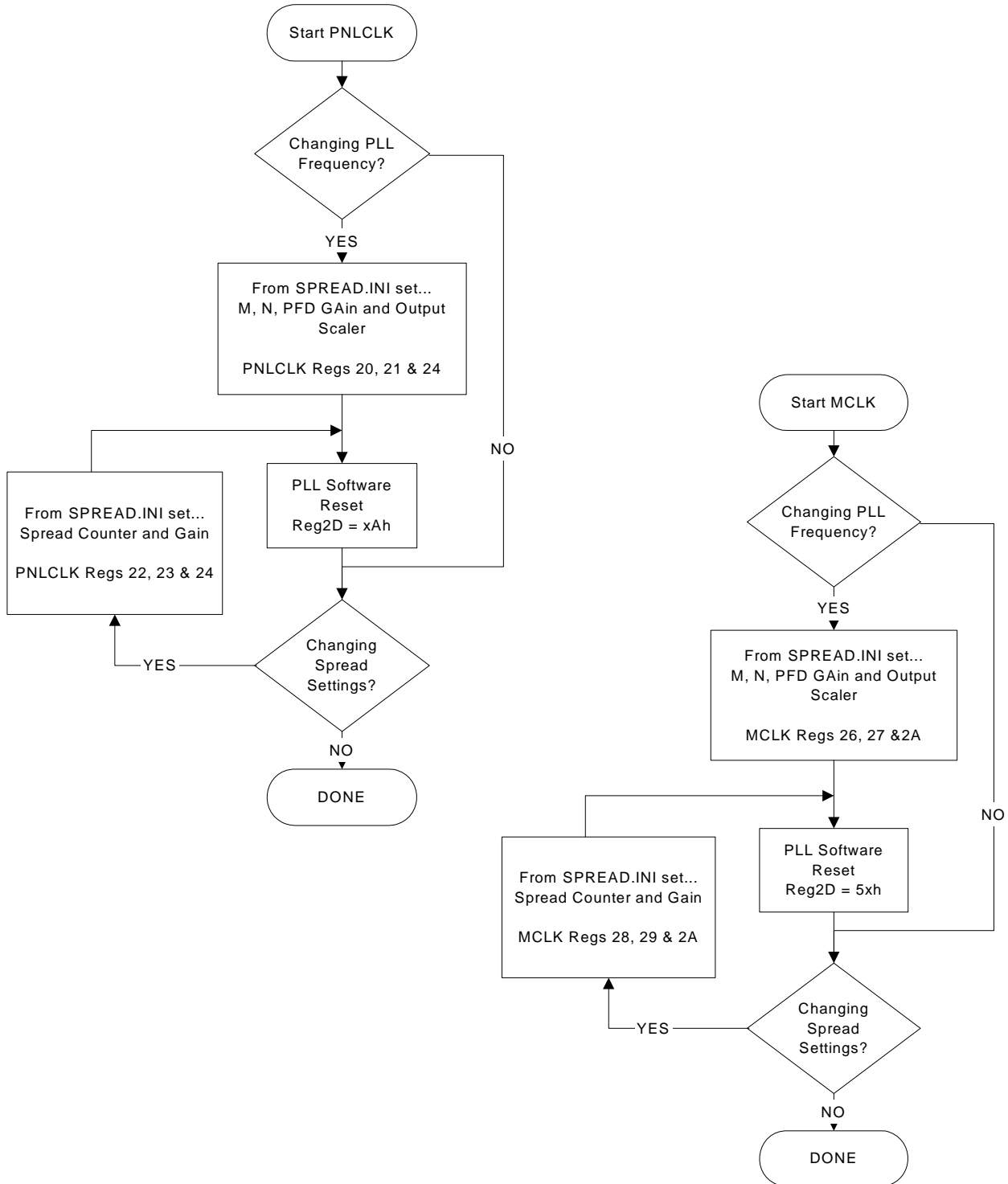   (1) 00 to 0F (2) 10 to 1F (3) 20 to 2F (4) 30 to 3F

10.2 Programming Flow for Modifying PLL and DPA Settings

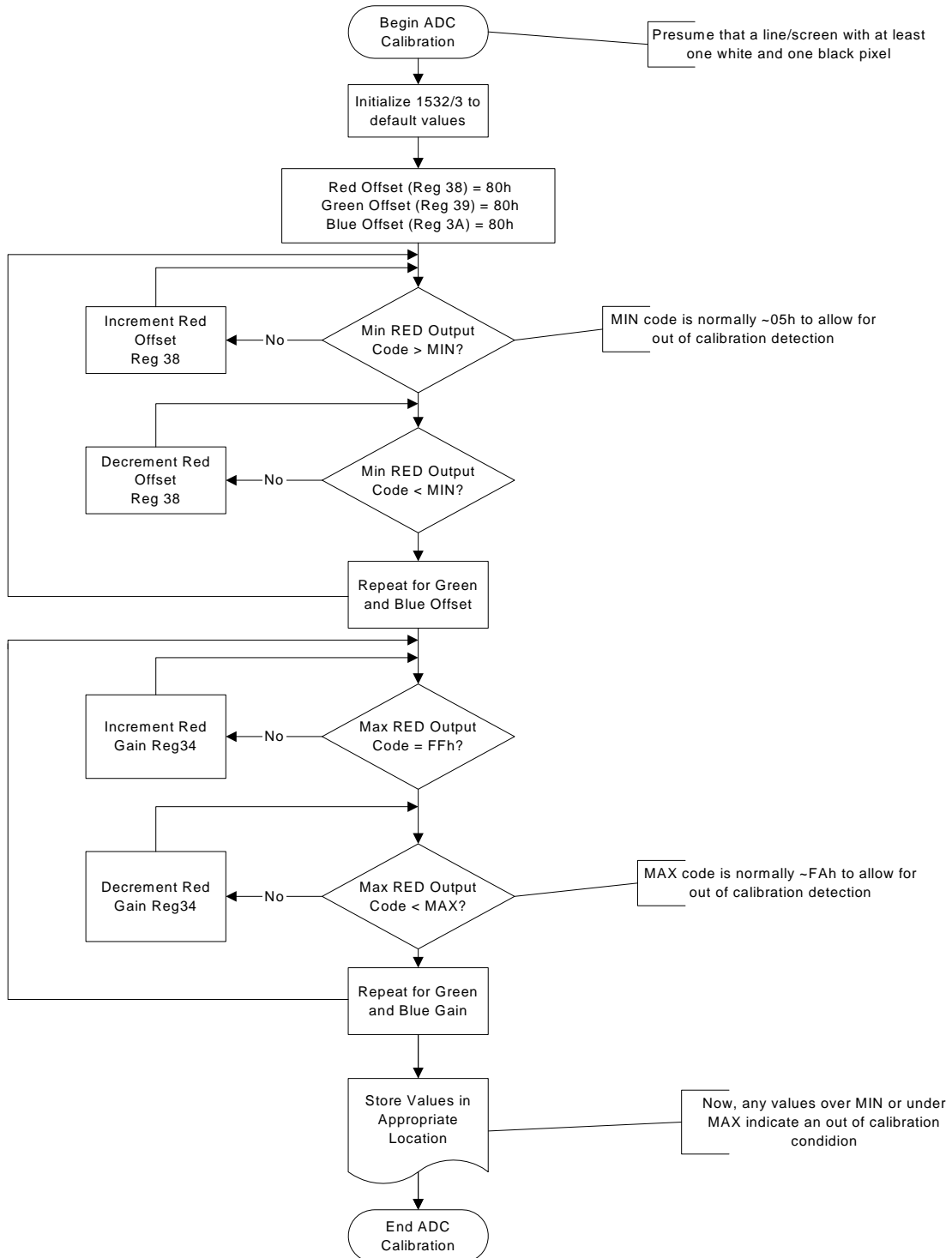**Figure 10-2.   ICS1532 Flow for Capture/Input Clock PLL**
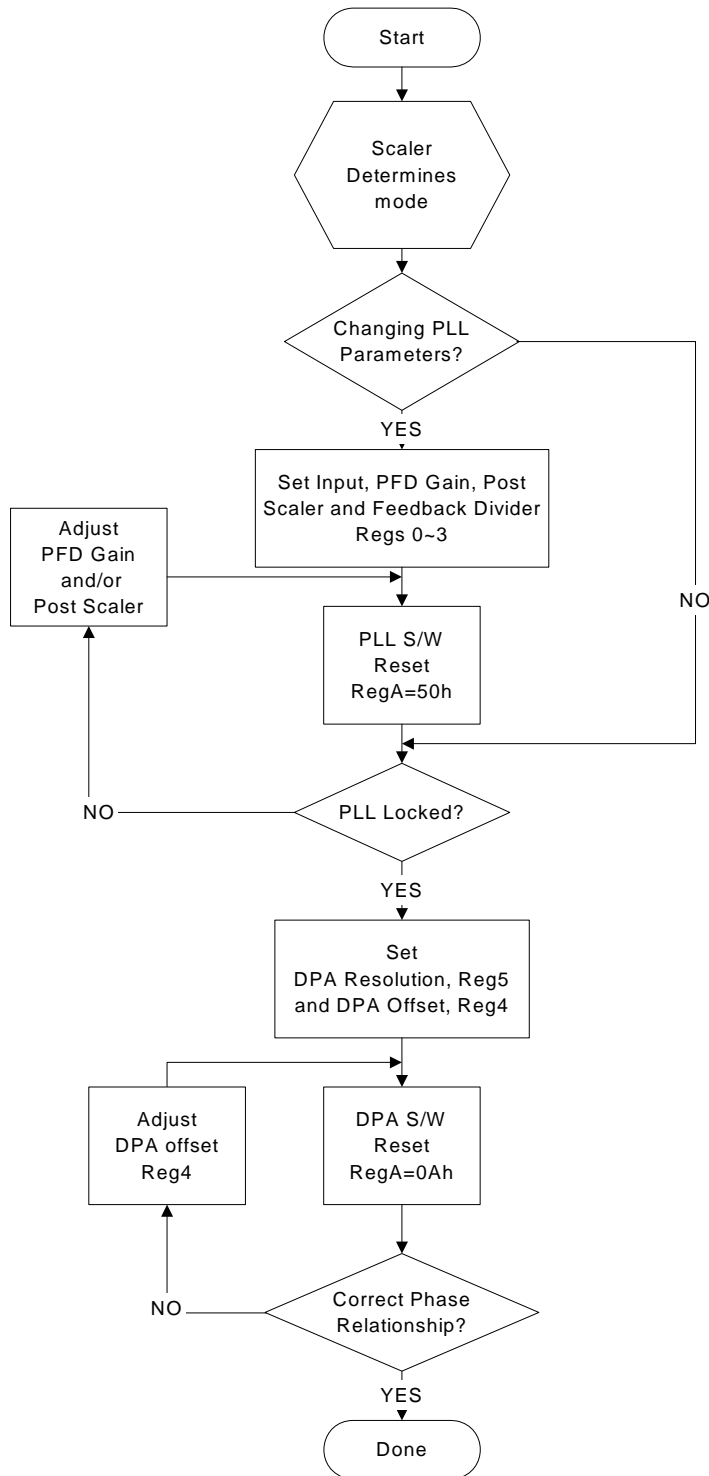
10.2.1 Programming Flow for Modifying Settings for Spread Spectrum

Figure 10-3. ICS1532 Flow for PNLCLK and MCLK PLL Spread-Spectrum Settings

www.idt.com

10.2.2   Programming Flow for Calibrating

Figure 10-4.   ICS1532 Flow for ADC Calibration

Chapter 11 AC/DC Operating Conditions

11.1 Absolute Maximum Ratings

Table 11-1 lists absolute maximum ratings for the ICS1532. Stresses above these ratings can cause permanent damage to the ICS1532. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the ICS1532 at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

During normal operation, the supply voltages for the ICS1532 must remain within the recommended operating conditions.

Table 11-1. ICS1532 Absolute Maximum Ratings

Item	Rating	Notes
VDD, VDDQ (See Note)	4.3 V	Measured with respect to VSS
VDDxADC (See Note)	3.6 V	Measured with respect to VSS
Digital Inputs	VSS -0.3 V to +5.5 V	
Digital Outputs	VSSQ -0.3 V to VDDQ +0.3 V	
Analog Inputs	VSS -0.3 V to +5.5 V	
Analog Outputs	VSSA -0.3 V to VDDA +0.3 V	
Storage Temperature	-65 to +150° C	
Junction Temperature	125° C	
Soldering Temperature	260° C	20 seconds max

NOTE: Electrostatic-sensitive device. Do not open or handle except in a static-free workstation.)

11.2 Recommended Operating Conditions

Table 11-2. Environmental Conditions

Parameter	Minimum	Typical	Maximum	Units
Ambient Operating Temperature	0		+70	°C
3.3 Power Supply Voltage	+3.15	+3.3	+3.45	V
2.5 Volt Power Supply Voltage	+2.35	+2.5	+2.65	V

11.3 AC Operating Characteristics

Table 11-3   Pin Specific I/O AC Parameters

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
AC Inputs						
HSYNC Input Frequency	f_{HSYNC}	12		120	kHz	
COAST Input Frequency	f_{PDEN}	30		120	Hz	
Analog Input (HSYNC)						
Input High Voltage	V_{IH}		1.8	5.5	V	Reg0:7~6 = 00
Input Low Voltage	V_{IL}	VSS - 0.3	1.1		V	Reg0:7~6 = 00
Input High Voltage	V_{IH}		2.3	5.5	V	Reg0:7~6 = 01
Input Low Voltage	V_{IL}	VSS - 0.3	1.1		V	Reg0:7~6 = 01
Input High Voltage	V_{IH}		1.9	5.5	V	Reg0:7~6 = 10
Input Low Voltage	V_{IL}	VSS - 0.3	1.3		V	Reg0:7~6 = 10
Digital Inputs (SDA, SCL, EXTFB, OSC, I²CADDR)						
Input High Voltage	V_{IH}	2		5.5	V	
Input Low Voltage	V_{IL}	VSS - 0.3		0.8	V	
Input Hysteresis		0.2		0.6	V	
POR Threshold		VSS	1.8		V	Voltage that resets register values
SDA Digital Output						
SDA Output Low Voltage	V_{OL}			0.4	V	IOUT = 3 ma
SDA Output High Voltage	V_{OH}			6.0	V	Set by external Rset resistor
Pixel Data Outputs						
Output Impedance	R_O		65		Ω	1 V < V_O < 2 V
Skew from ADCRCLK	Tsk		4ns			
LVCMOS Outputs (ADCRCLK, ADSYNC, LOCK/REF)						
Output Impedance	R_O	45	65	85	Ω	1 V < V_O < 2 V
ADCRCLK Output Frequency	F_s MAX/2			50	MHz	VDDD = 3.3 V
Duty Cycle	S_{DC}	45		55	%	3

Note 1- V_{OL} must not fall below the level given so that the correct value for IOUT can be maintained.

Note 2- Measured at 135 MHz, 3.6 VDC, 0°C, 20 pF, Unterminated

Table 11-4 AC Operating Characteristics (VDDx = 3.3 Volts, VDDx(2.5) = 2.5 Volts, Temperature = 25°C

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
ADC Resolution			8	8	Bits	
DC Accuracy						
Differential Nonlinearity	DNL		+1.2/-1	+2.75/-1	LSB	
Integral Nonlinearity	INL			±2.5	LSB	
No Missing Codes						By Design
Analog Inputs						
ADC Input Voltage Range	V_{IA}	0.5	0.7	1.2	Vpp	
Input Capacitance	I_C			2	pF	
Input Resistance	I_R	1			MΩ	
Switching Performance						
Analog Conversion Rate		10		110	MHz	
I2C Bus Speed		100		4,000	KHz	
VCO Frequency		150		1,000	MHz	
Sampling Clock Frequency		10		110	MHz	
Clock Jitter			1		ns	
Digital Inputs						
Input High Voltage	V_{IH}	2		5.5	V	5.5
Input Low Voltage	V_{IL}	VSS-0.3		0.8	V	
Input High Current	I_{IH}			-1	uA	
Input Low Current	I_{IL}			1	uA	
Input Capacitance	I_c			3	pF	
Digital Outputs						
Output High Voltage	V_{OH}	VDD-0.1			V	
Output Low Voltage	V_{OL}			0.1	V	
Pixel Data Output Impedance	R_O		65		Ω	1 V < V_O < 2 V
ADCRCLK to Pixel Data Skew	Tsk		±5		ns	
ADCRCLK Duty Cycle		45	50	55	%	Note 2
Output Coding			Binary			By Design
Power Requirements						
3.3 V Digital Supply Voltage	IDDD	+3.15	+3.3	+3.45	V	
3.3 V Analog Supply Voltage	IDDA	+3.15	+3.3	+3.45	V	
2.5 V Supply Voltage	IDDA2.5	+2.35	+2.5	+2.65	V	
3.3 V Digital Supply Current				135	mA	110 MHz
3.3 V Analog Supply Current				125	mA	110 MHz
2.5 V Supply Current				125	mA	110 MHz

Table 11-4   AC Operating Characteristics (VDDx = 3.3 Volts, VDDx(2.5) = 2.5 Volts, Temperature = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Total Power Dissipation			900	1200	mW	110 MHz
Crystal Requirements						
Frequency - Parallel Resonance		10	14.3$\overline{18}$	20	MHz	
Load Capacitance		-	20	-	pF	
Zero frequency error by design when the total on-chip + stray capacitance is equal to 20pF. When using spread spectrum functionality, 14.3$\overline{18}$ MHz is REQUIRED.						
Dynamic Performance						
Analog Input Bandwidth			450		MHz	
Signal-to-Noise Ratio	SNR	32	44		dB	108 MHz Internal PLL
Crosstalk			50		dBc	
Thermal Characteristics						
Junction to Case Thermal Resistance			9		^{o}C/W	
Junction to Ambient Thermal Resistance			32		^{o}C/W	Flow = 0 m/s

# Chapter 12   Timing Diagrams

12.1   AC Timing Diagrams

12.1.1   Phase-Locked-Loop Timing for Digital Setup and Hold

The input HSYNC signal is used to generate the REF output signal. In the Phase/Frequency Detector, the REF signal is compared with ADCSYNC (which provides the recovered HSYNC signal). Table 12-1 gives the timing for these signals, and Figure 12-1 shows timing characteristics.

Table 12-1.   Phase-Locked-Loop Timing

Time Period	Timing Description	Min	Typ	Max	Units
t1	Input HSYNC Rise Time to REF Rise Time	TBD	7	TBD	ns
Tp	ADCRCLK Period		$Tp = \dfrac{\text{Input HSYNC Frequency}}{(\text{Reg 03 and 02}) + 8}$		ns
Td	ADCRCLK Duty Cycle	45-55	50-50	55-45	%
t2	ADCSYNC Active Time		4 x Tp		ns

Figure 12-1.   Timing for Phase-Locked Loop
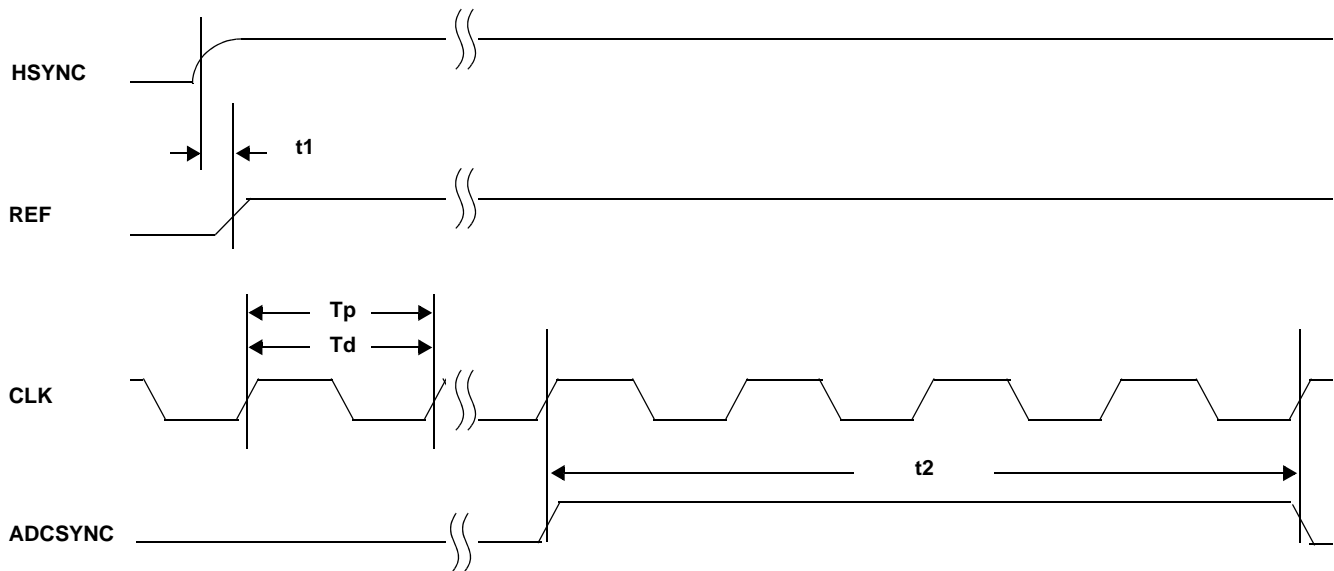
12.1.2   Digital Output Data Timing
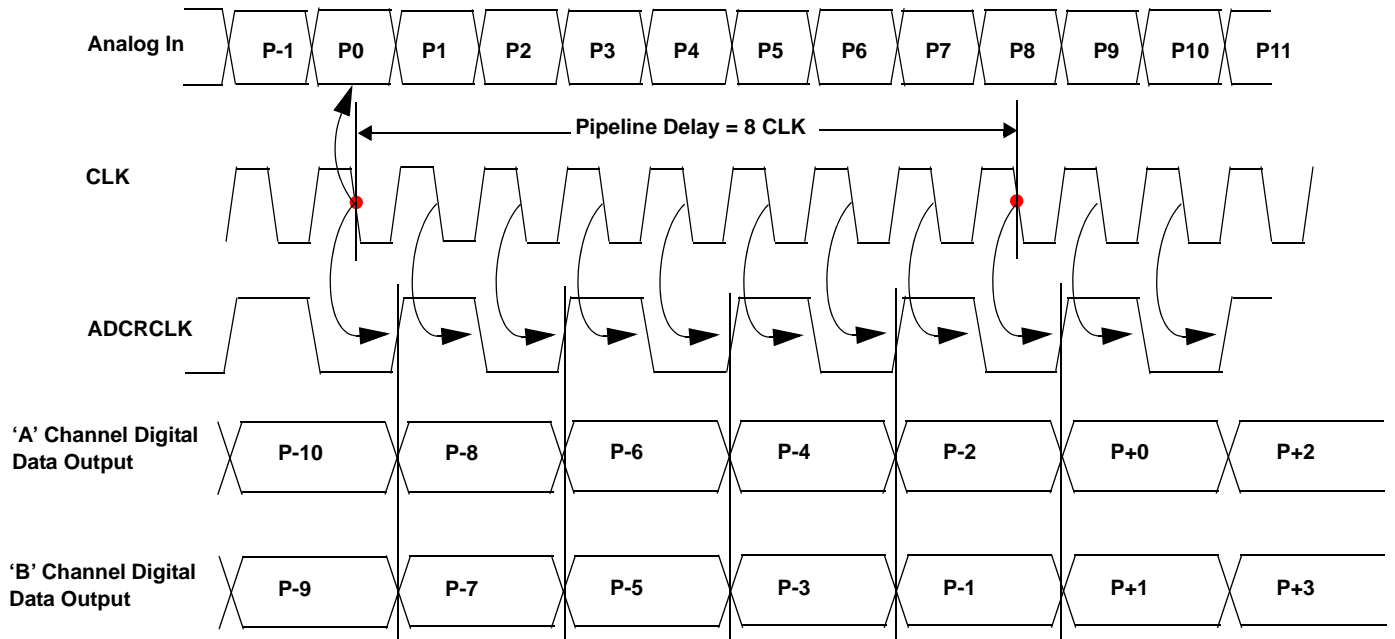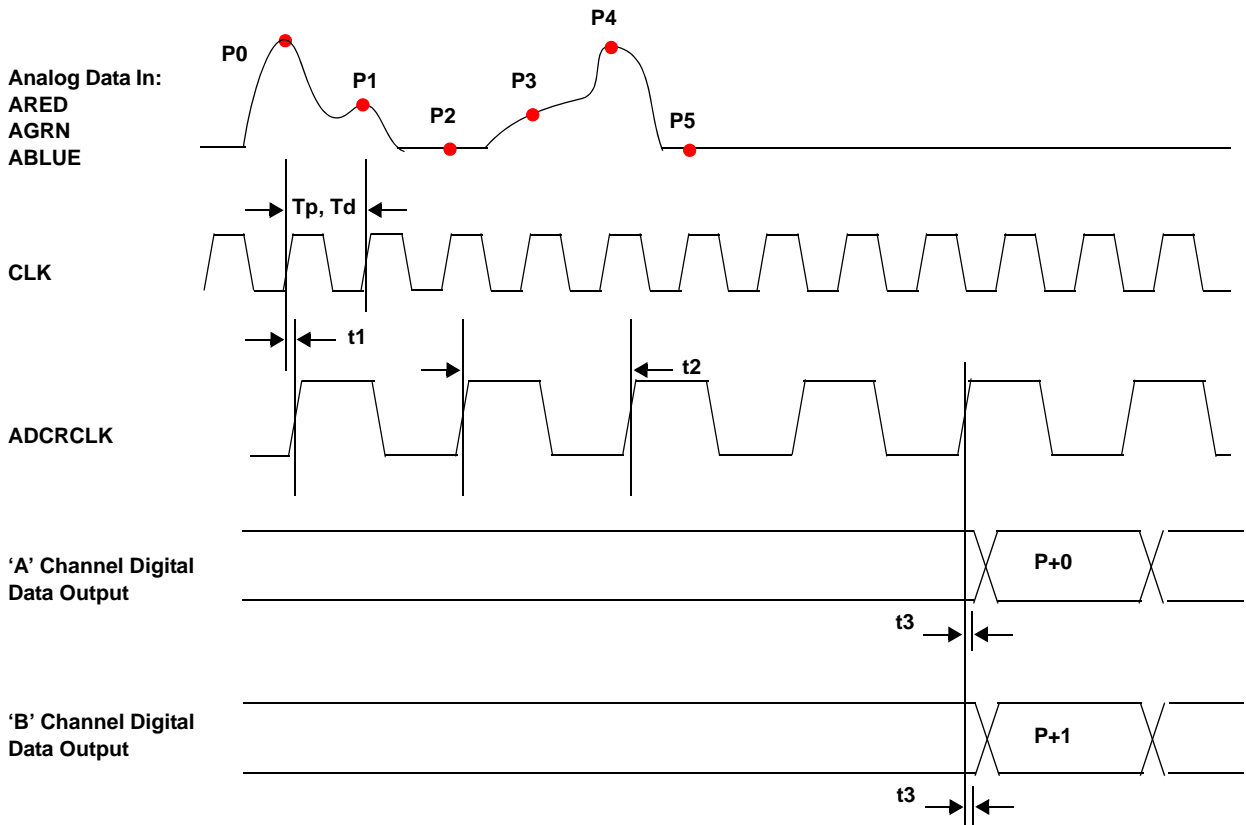
Figure 12-2.   Two Pixel per Clock Output Data

Table 12-2. Timing for 2-Pixels-per-Clock Mode

Time Period	Timing Description	Min	Typ	Max	Units
Tp, Td	CLK Period, CLK Duty Cycle		See Table 12-1.		ns
t1	CLK Rise Time to ADCRCLK Rise Time		2.6		ns
t2	ACDRCLK Period		$t2 = 2 \times Tp$		ns
t3	Digital Data Skew from ADCRCLK				ns

Figure 12-3.   AC Timing for 2-Pixels-per-Clock Mode

12.1.3   ADCRCLK v.s. ADCSYNC Edge Relationships and Invalid Data

Figure 12-4.   ADCSYNC AutoZero Event
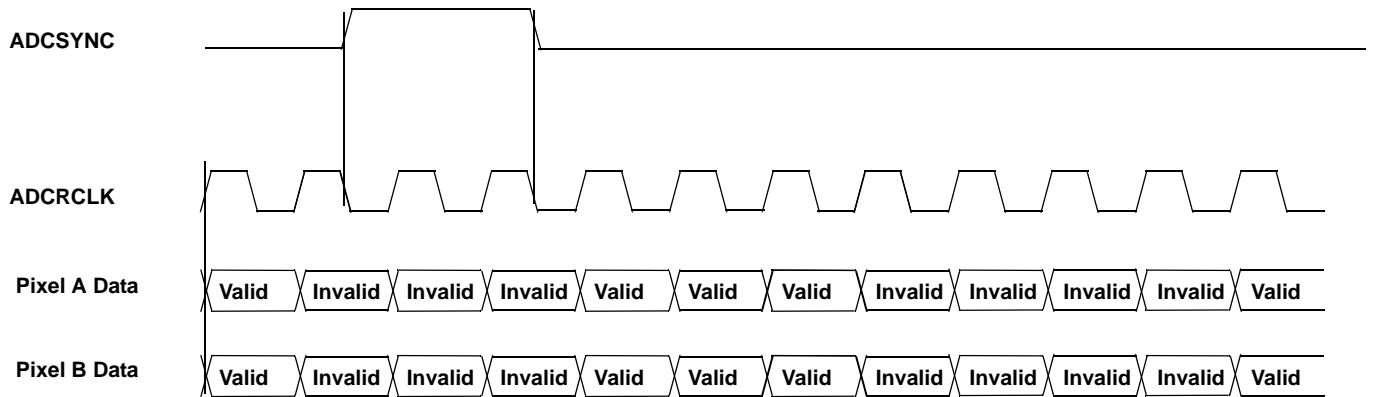
12.2   Resetting the ICS1532 to a known state

Below is shown the two ways to reset the ICS1532 to a known state.

12.2.1   Reset Pin Input

Momentarily bring the active high RESET# input pin low to cause the part to reset to a known state.

12.2.2   Power-On Reset (POR) Timing

The ICS1532 incorporates special internal power-on reset circuitry that requires no external reset signal.

To use the POR circuitry:

– Reduce the level of the all supply voltages to the ICS1532 (and the voltage seen on all ICS1532 pins) so that it is below the threshold voltage (VDD_{th}) of the POR circuit for the period t1 shown below

– Keep the supply voltage below that threshold voltage for time t1, such that power-conditioning capacitors for the printed circuit board are drained and the proper reset state is latched.

- A successful power-on reset results in all the ICS1532 registers having the appropriate reset values as stated in the tables in Chapter 4, "Register Set".

Table 12-3.   ICS1532 POR Transition Times

Symbol	Timing Description	Min	Typ	Max	Units
VDD	Supply Voltage ('On' State)	3.15	3.3	3.45	V
VDD_{th}	Threshold Supply Voltage		1.8		V
t_1	Hold Time for Reset State		10		ms

Figure 12-5.   Power-On Reset Condition for ICS1532
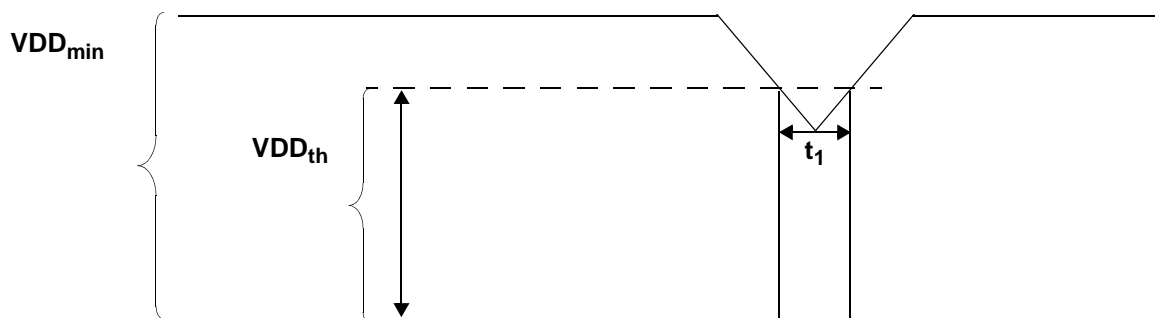
Chapter 13   Package Dimensions

This section gives the physical dimensions for the package for the ICS1532, which is a 144-pin LQFP.

- The lead count (N) for the package is 144 leads.
- The nominal footprint (that is the body) for the package is 20 mm × 20 mm × 1.4 mm.
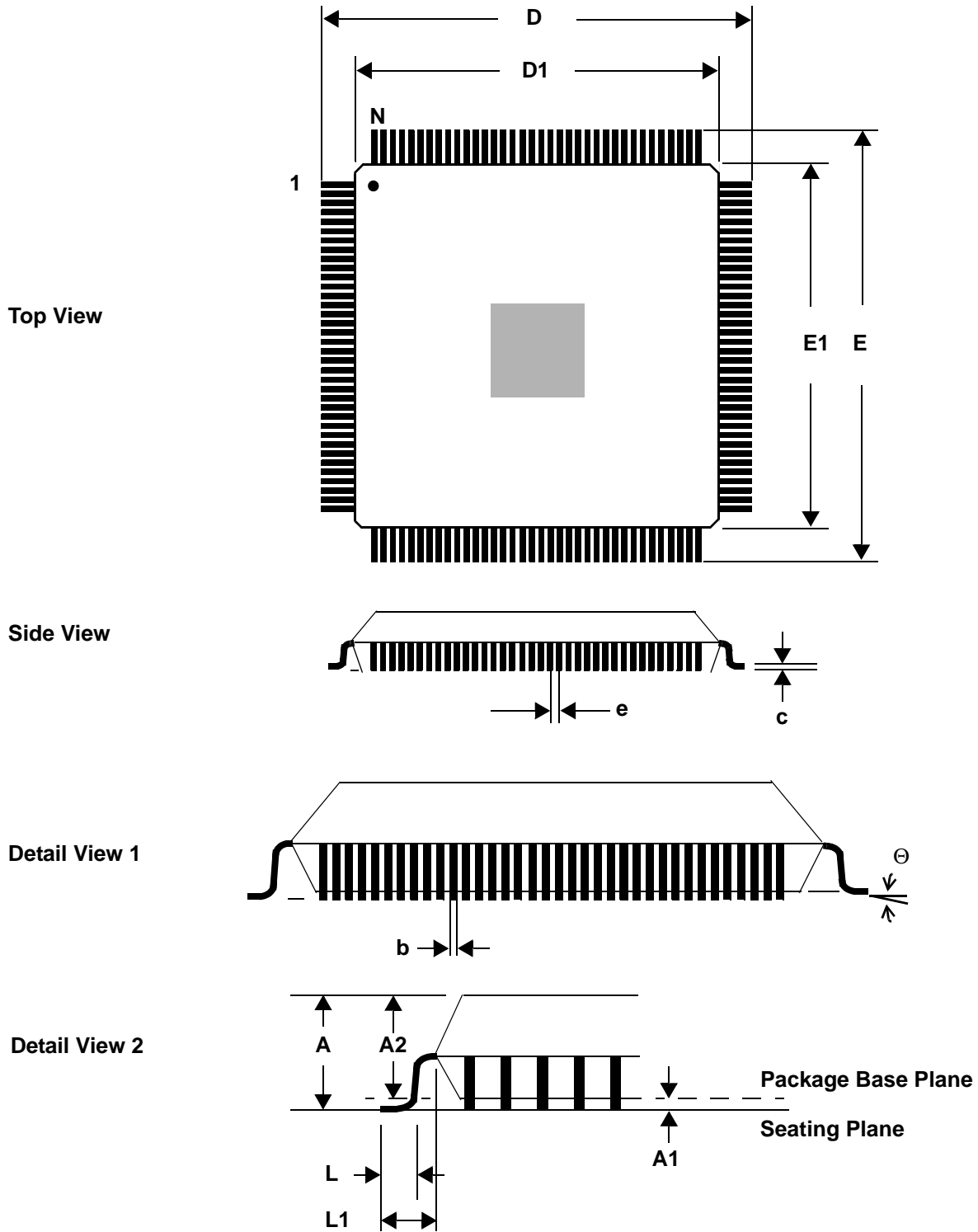
Note:

1. For full mechanical specifications, see JEDEC drawing number MS-026 Rev A.
2. Table 13-1 lists the ICS1532 physical dimensions. These dimensions are:
   a. For planning purposes only.
   b. Subject to change.
   c. Shown in Figure 13-1.

Table 13-1.   Physical Dimensions for ICS1532

Symbol	Description	Min.	Nominal	Max.	Unit
A	Full Package Height			1.60	mm
A1	Package Body Standoff (the distance from the seating plane to the base plane of the package body)	0.05		0.15	mm
A2	Package Body Thickness	1.35	1.40	1.45	mm
b	Lead Width	0.17	0.22	0.27	mm
c	Lead Thickness	0.09		0.20	mm
D	Tip-to-Tip Dimension		22.0		mm
D1	Package Body Dimension		20.0		mm
e	Lead Pitch		0.50		mm
E	Tip-to-Tip Dimension		22.0		mm
E1	Package Body Dimension		20.0		mm
L	Lead Tip Length	0.45	0.60	0.75	mm
L1	Lead Length, Entire Length		1.0		mm
Q	Lead Tip Angle	0	3.5	7	degrees

Figure 13-1. Physical Dimensions for ICS1532

Top View

Side View

Detail View 1

Detail View 2

D

D1

N

1

E1 E

e

c

Θ

b

A

A2

Package Base Plane

Seating Plane

A1

L

L1

Chapter 14   Ordering Information

Figure 14-1   ICS1532 Ordering Information

Part / Order Number	Marking	Package	Shipping
1532A	ICS1532A	144-pin LQFP	Trays

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