

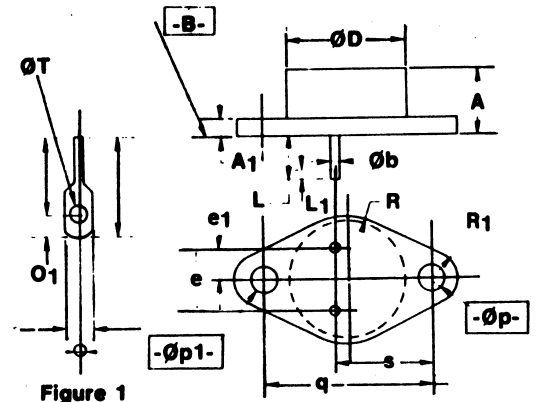
PARAMETERS

2N6649

PNP DARLINGTON TRANSISTOR

Description: PNP Darlington Transistor

Manufacturer.....	
Mil/High-Rel? (Y/N).....	
Ic Max. (A).....	10
Vbr CEO.....	60
Max. PD (W).....	27
Derate Above 25xC.....	570m
Min hFE.....	1.0k
Max. hFE.....	20k
@Ic (test) (A).....	5.0
@VCE (test).....	3.0
Trans. Freq (Hz) Min.....	20M
Icbo Max. @Vcb Max. (A).....	300uL6
R(sat) (j).....	300m
t(on) Delay (S).....	
Tr Max. (s).....	
t(stor) Max. (S).....	
t(f) Max. (S).....	
Mat.....	Silicon
Oper. Temp (xC) Max.....	150u
Pkg Style.....	T0-204AA
Surface Mounted (Y/N).....	N
Pinout Equivalence Number.....	3-38



u Junction Temperature 2 It(rms) Derating Begins at 100xC 6 ICEV
 L Measured at 25xC Case Tempe.

SYMBOL	AA		NOTE
	MIN.	MAX.	
A	6.4	11.4	
A1	-	3.42	
b	-	-	
Øb	.968	1.092	3
ØD	-	22.22	
e	10.67	11.17	
e1	5.21	5.21	
L	7.93	-	3
L1	-	-	
O1	-	-	
Øp	3.84	4.08	5,9
Øp1	3.84	4.08	5,9
q	30.15 BSC		
R	-	13.33	
R1	-	4.77	6
S	16.64	17.14	
ØT	-	-	
NOTE	1,2,8,9,10,11		

NOTES:

1. Refer to applicable symbol list.
2. Dimensioning and tolerancing per ansi Y14.5, 1973.
3. Two leads.
4. Square or radius on end of terminal optional.
5. Two holes.
6. Both ends.
7. Figure 1 lead configuration applicable.
8. Datum surface -B- is seating plane.
9. Dimensions -Øp- & -Øp1- are datums.
10. Positional tolerance for ØD:
 $\phi \pm 0.25 (M) B \pm 0.1 (M) \phi R (M)$
11. Controlling dimension: Millimeters

