19-3799; Rev0; 3/91

MAXIM

CMOS Dual 12-Bit Double-Buffered µP-Compatible DAC

MX7549

General Description

Maxim's MX7549 is a dual, 12-bit, four-quadrant multiplying, current-output D/A converter (DAC) with 1% DAC-to-DAC matching. Thin-film resistors, laser-trimmed at the wafer level, maintain full accuracy over the operating temperature range. Other features include ±1/2LSB maximum integral nonlinearity, ±3LSB full-scale error, and ±5ppm/°C gain temperature coefficient.

Three address lines controlled by standard CHIP SELECT ($\overline{CS}$) and WRITE ($\overline{WR}$) signals simplify microprocessor (µP) interfacing. Each DAC is loaded in three 4-bit nibbles. The UPDATE ($\overline{UPD}$) input updates the output of both DACs simultaneously.

All digital inputs are TTL, 74HC, and +5V CMOS compatible. The MX7549 operates from a single +5V to +15V supply and is pin-compatible with the AD7549.

Applications

Automatic Test Equipment (ATE)

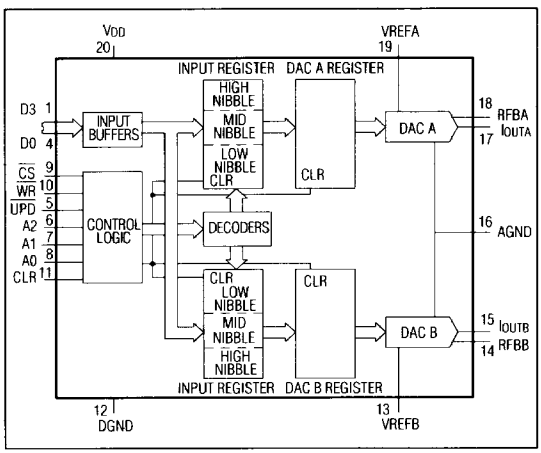
Microprocessor-Based Process Control

Programmable Power Supplies

Programmable Filters

Synchro Applications

Functional Diagram



Features

- ◆ **Two 12-Bit, Double-Buffered DACs in One Package**
- ◆ **4-Bit Microprocessor Interface**
- ◆ **Four-Quadrant Multiplication**
- ◆ **1% DAC-to-DAC Matching**
- ◆ **±1/2LSB Max Integral Nonlinearity**
- ◆ **±3LSB Max Full-Scale Error**
- ◆ **±5ppm/°C Max Gain Tempco**
- ◆ **Operates with a Single +5V to +15V Supply**
- ◆ **Pin-Compatible with the AD7549**

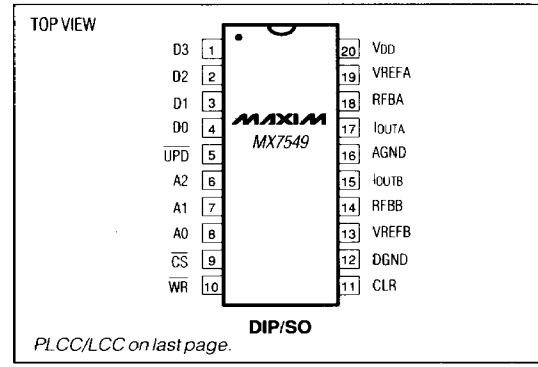
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSBs)
MX7549JN	0°C to +70°C	20 Plastic DIP	±1
MX7549KN	0°C to +70°C	20 Plastic DIP	±1/2
MX7549JCWP	0°C to +70°C	20 Wide SO	±1
MX7549KCWP	0°C to +70°C	20 Wide SO	±1/2
MX7549JP	0°C to +70°C	20 PLCC	±1
MX7549KP	0°C to +70°C	20 PLCC	±1/2
MX7549JC/D	0°C to +70°C	Dice*	±1
MX7549AQ	-40°C to +85°C	20 CERDIP	±1
MX7549BQ	-40°C to +85°C	20 CERDIP	±1/2
MX7549SE	-55°C to +125°C	20 LCC**	±1
MX7549TE	-55°C to +125°C	20 LCC**	±1/2
MX7549SQ	-55°C to +125°C	20 CERDIP**	±1
MX7549TQ	-55°C to +125°C	20 CERDIP**	±1/2

*Contact factory for dice specifications.

**Contact factory for availability and processing to MIL-STD-883.

Pin Configurations



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ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND ..... -0.3V to +17V
VREFA to AGND ..... ±25V
VREFB to AGND ..... ±25V
VRFBA to AGND ..... ±25V
VRFBB to AGND ..... ±25V
AGND to DGND ..... -0.3V to V_{DD}+0.3V
Digital Input Voltage to DGND ..... -0.3V to V_{DD}+0.3V
Analog Outputs to DGND ..... -0.3V to V_{DD}+0.3V

Power Dissipation to +75°C (any package) 550mW
Derate above +75°C by ..... 10mW/°C
Operating Temperature Ranges:
MX7549J_/K_ ..... 0°C to +70°C
MX7549AQ/BQ ..... -40°C to +85°C
MX7549S_/T_ ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +15V ±5%; VREFA = VREFB = +10V; I_{OUTA} = I_{OUTB} = AGND = DGND = 0V; All Grades; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
ACCURACY								
Resolution	N				12			Bits
Integral Nonlinearity	INL			J/A/S			±1	LSB
				K/B/T			±1/2	
Differential Nonlinearity	DNL	Guaranteed monotonic over temperature					±1	LSB
Full-Scale Error				J/A/S			±6	LSB
				K/B/T			±3	
Gain Temperature Coefficient (Note 2)	ΔGain/ ΔTemp					±1	±5	ppm/°C
Output Leakage Current	I_{OUT}	DAC_ Register loaded with all 0's	T_A = +25°C				20	nA
			T_A = T_{MIN} to T_{MAX}	J/K/A/B			150	
				S/T			250	
Reference Input Resistance					7	11	18	kΩ
VREFA, VREFB Input Resistance Match	VREF			J/A/S		±1	±3	%
				K/B/T		±1	±2	
DYNAMIC PERFORMANCE (Note 3)								
Output-Current Settling Time (Note 4)	t_S		T_A = +25°C			0.8	1.5	µs
AC Feedthrough VREF_ to I_{OUT}_ (Note 5)			T_A = +25°C				-70	dB
			T_A = T_{MIN} to T_{MAX}				-65	
Digital-to-Analog Glitch Impulse	Q	Note 6	T_A = +25°C			10		(nV)(s)
Output Capacitance	C_{OUT}	DAC_ loaded with all 0's				40	80	pF
		DAC_ loaded with all 1's				100	160	
Channel-to-Channel Isolation VREF_ to I_{OUT}_		VREFA = 20Vp-p 100kHz sine wave, VREFB = 0V or VREFB = 20Vp-p 100kHz sine wave, VREFA = 0V				-62		dB
Digital Crosstalk		For code transitions from all 0's to all 1's				10		(nV)(s)
Output-Noise Voltage Density		From RFBA to I_{OUTA} and from RFBB to I_{OUTB}. 10Hz to 100kHz.				15		nV/√Hz
Harmonic Distortion	THD	V_{IN} = 6Vrms 1kHz				-90		dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +15V ±5%; VREFA = VREFB = +10V; I_{OUTA} = I_{OUTB} = AGND = DGND = 0V; All Grades; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL INPUTS							
Input Current	I_{IN}	V_{IN} = V_{DD}	T_A = +25°C			±1	µA
			T_A = T_{MIN} to T_{MAX}			±10	
Input Low Voltage	V_{IL}					0.8	V
Input High Voltage	V_{IH}			2.4			V
Input Capacitance (Note 3)	C_{IN}					7	pF
POWER REQUIREMENTS							
Power Supply	I_{DD}	All digital inputs at V_{IH}				3	mA
Power-Supply Rejection	$\frac{\Delta Gain}{\Delta V_{DD}}$	V_{DD} = 10.8V to 15.75V			±0.0005	±0.002	%/%

TIMING CHARACTERISTICS

(V_{DD} = +15V, VREFA = VREFB = +10V; I_{OUTA} = I_{OUTB} = AGND = DGND = 0V; All Grades; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Address Valid to Write Setup Time	t_1		T_A = +25°C		50			ns
			T_A = T_{MIN} to T_{MAX}	J/A	75			
				S/T	90			
Address Valid to Write Hold Time	t_2				0			ns
Data Setup Time	t_3		T_A = +25°C		70			ns
			T_A = T_{MIN} to T_{MAX}	J/A	95			
				S/T	120			
Data Hold Time	t_4				0			ns
Chip Select or Update to Write Setup Time	t_5				0			ns
Chip Select or Update to Write Hold Time	t_6				0			ns
Write Pulse Width	t_7		T_A = +25°C		50			ns
			T_A = T_{MIN} to T_{MAX}	J/A	75			
				S/T	90			
Clear Pulse Width	t_8		T_A = +25°C		50			ns
			T_A = T_{MIN} to T_{MAX}	J/A	75			
				S/T	90			

Note 1: At V_{DD} = +5V, the device is functional with degraded performance. Performance at power-supply tolerance limits is guaranteed by Power-Supply Rejection test.
Note 2: Guaranteed by design.
Note 3: These characteristics are for design guidance only and are not subject to test.
Note 4: Measured to 0.01% of full-scale range. I_{OUT} Load = 100Ω, CEXT = 13pF. DAC output measured from falling edge of $\overline{WR}$.
Note 5: VREF_ = 20Vp-p 10kHz sine wave. DAC register is loaded with all zeros.
Note 6: Measured with V_{REFA} = V_{REFB} = 0V. I_{OUTA}, I_{OUTB} load = 100Ω, C_{EXT} = 13pF. DAC registers alternately loaded with all 0's and 1's.

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Pin Description

PIN	NAME	FUNCTION
1	D3	Data Bit 3, 7, or 11 (MSBs)
2	D2	Data Bit 2, 6, or 10
3	D1	Data Bit 1, 5, or 9
4	D0	Data Bit 0, 4, or 8 (LSBs)
5	$\overline{UPD}$	$\overline{UPDATE}$ Input - active low. Updates both DAC registers simultaneously from input registers.
6-8	A2-A0	Address Lines 2 - 0
9	$\overline{CS}$	$\overline{CHIP\ SELECT}$ Input - active low
10	$\overline{WR}$	$\overline{WRITE}$ Input - active low
11	CLR	CLEAR Input - active high. Clears all registers.
12	DGND	Digital Ground
13	VREFB	Voltage Reference Input to DAC B
14	RFBB	Feedback Resistor for DAC B
15	I_{OUTB}	DAC B Output
16	AGND	Analog Ground
17	I_{OUTA}	DAC A Output
18	RFBA	Feedback Resistor for DAC A
19	VREFA	Voltage Reference Input to DAC A
20	V_{DD}	Supply Voltage Input

Detailed Description

The nibble input registers of both DACs share a common 4-bit input buffer. Address inputs A2 - A0 select which DAC will receive a 4-bit nibble from the input data bus. With $\overline{CS}$, the address lines, and $\overline{WR}$ low, the low-nibble (4 least significant bits (LSBs)) from the input buffer transfers to the DAC A low-nibble register (Table 1). The mid- and high-nibbles (4 mid and most significant bits (MSBs)) are then transferred in two additional WRITE cycles, reflecting the subsequent 3-bit address codes. The 4th WRITE cycle transfers the 12-bit data from the DAC A nibble input registers to the DAC A register. The DAC B register is loaded in a similar manner. With $\overline{CS}$ high, $\overline{UPD}$ low, and after all nibble input registers are loaded, strobing $\overline{WR}$ updates DAC A and DAC B registers simultaneously, eliminating one WRITE cycle. All digital inputs incorporate standard protection circuitry and are TTL, 74HC, and +5V CMOS compatible.

D/A Converter

The basic MX7549 circuit includes two identical DACs with laser-trimmed, thin-film (R-2R) arrays with NMOS current-steering switches (Figure 1). Binary-weighted currents switch between AGND and the output, depending on the status of each input data bit.

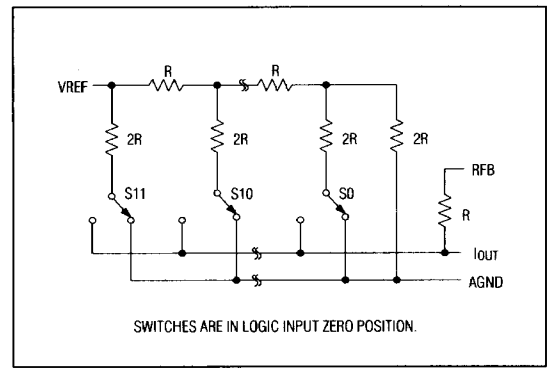

Figure 1. MX7549 Simplified DAC Schematic

The current output can be converted to a voltage by adding an external output amplifier (Figures 3, 4). The VREF input accepts a wide range of signals, including fixed and time-varying voltage or current inputs. Consider the temperature coefficient of R1 (R3) and R2 (R4) to minimize gain variation with temperature. The internal feedback resistor is compensated with an NMOS switch that matches the NMOS switches used in the R-2R array. This yields excellent supply rejection and gain temperature coefficients.

The output capacitance, C_{OUT}, is code dependent and is typically 40pF with DAC loaded with all zeros, or 100pF with all ones.

Digital Circuit

Logic inputs are TTL, 74HC, and +5V CMOS compatible (0.8V and 2.4V) at V_{DD} = +12V to +15V. DAC supply current can be reduced below specified levels by keeping digital input voltages as close to the logic supply and ground as possible (as with CMOS logic levels).

Table 1. MX7549 Truth Table

CLR	$\overline{UPD}$	$\overline{CS}$	$\overline{WR}$	A2	A1	A0	FUNCTION
0	X	X	1	X	X	X	No data transfer
0	1	1	X	X	X	X	No data transfer
1	X	X	X	X	X	X	All registers cleared
0	1	0	⊓	0	0	0	DAC A low-nibble register loaded from data bus
0	1	0	⊓	0	0	1	DAC A mid-nibble register loaded from data bus
0	1	0	⊓	0	1	0	DAC A high-nibble register loaded from data bus
0	1	0	⊓	0	1	1	DAC A register loaded from nibble registers
0	1	0	⊓	1	0	0	DAC B low-nibble register loaded from data bus
0	1	0	⊓	1	0	1	DAC B mid-nibble register loaded from data bus
0	1	0	⊓	1	1	0	DAC B high-nibble register loaded from data bus
0	1	0	⊓	1	1	1	DAC B register loaded from nibble registers
0	0	1	⊓	X	X	X	DAC A and B registers updated simultaneously

Note: X = Don't care

Interface

Figure 2 shows the timing diagram for the MX7549. A2, A1, and A0 select the nibble (low, mid, or high) input registers for DAC A or DAC B (Table 1). Data is transferred on the falling edge of $\overline{WR}$ with $\overline{CS}$ and CLEAR (CLR) low. When loading the high-nibble register, D11 is the MSB of the 4-bit data input. Similarly, D7 is the MSB for the mid nibble, and D3 is the MSB for the low nibble. Once the nibble input registers are loaded, the appropriate DAC register is selected and the data transferred. When $\overline{UPD}$ and CLR are low and $\overline{CS}$ high, the DAC registers are updated simultaneously when $\overline{WR}$ goes active (low).

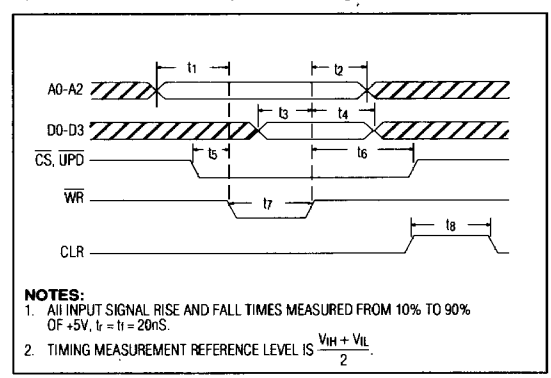

Figure 2. Timing Diagram for MX7549

Applications

Unipolar Operation

Figure 3 shows the most common configuration for the MX7549 that is used for unipolar binary operation or two-quadrant multiplication when $V_{IN\_}$ is an AC signal. For full-scale adjustment, load 1's into the DAC A register, and trim R1 until $V_{OUT\_} = -V_{IN}(4095/4096)$. Alternatively, R1-R4 can be omitted, and the reference voltage can be adjusted to compensate for full-scale error. DAC B full-scale errors are trimmed in the same manner.

Capacitors C1 and C2 provide phase compensation. They also reduce overshoot and ringing when fast amplifiers are used at the DAC output. Single or dual op amps can be used in this application.

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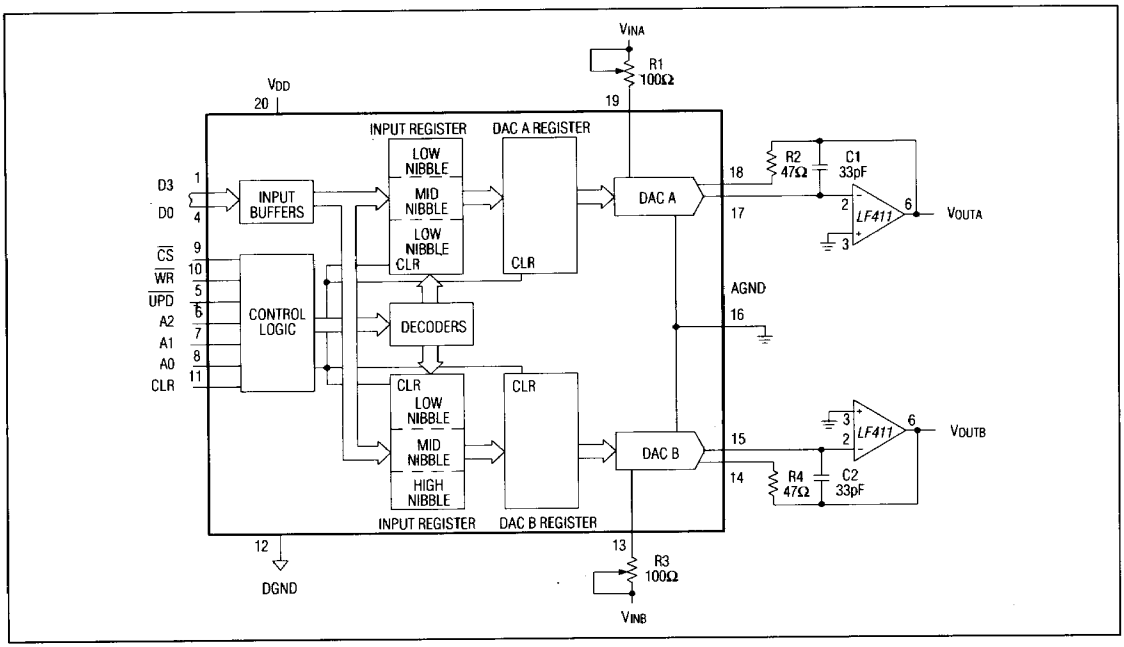

Figure 3. Dual DAC Unipolar Binary Operation (Two-Quadrant Multiplication)

Table 2. Unipolar Binary Code Table for MX7549

DIGITAL INPUT	ANALOG OUTPUT
1111 1111 1111	$-V_{IN}\frac{4095}{4096}$
1000 0000 0000	$-V_{IN}\frac{2048}{4096} = -\frac{1}{2}V_{IN}$
0000 0000 0001	$-V_{IN}\frac{1}{4096}$
0000 0000 0000	0V

Note 1: Use R1, R2, R3, and R4 only if gain adjustment is required.

Note 2: C1 and C2 capacitors prevent oscillations when using high-speed amplifiers.

Bipolar Operation

Figure 4 shows bipolar operation (four-quadrant multiplication) using offset-binary code. Adjust zero error as follows: with the appropriate DAC register loaded to 1000 0000 0000, adjust R1 (R3) so VOUTA (VOUTB) = 0V. Alternatively, omit R1 and R2 (R3, R4), and vary R6 and R7 (R9, R10) ratios for VOUTA = 0V. For full-scale trimming, adjust the VIN amplitude, or vary the R5 (R8) value. Select resistors R5, R6, and R7 (R8, R9, R10) so all ratios match to 0.01% and have low-temperature coefficients (e.g. RN-type metal film).

Table 3. Bipolar Binary Code Table for MX7549

DIGITAL INPUT	ANALOG OUTPUT
1111 1111 1111	$+V_{IN}\frac{2047}{2048}$
1000 0000 0001	$+V_{IN}\frac{1}{2048}$
1000 0000 0000	0V
0111 1111 1111	$-V_{IN}\frac{1}{2048}$
0000 0000 0000	$-V_{IN}\frac{2048}{2048} = -V_{IN}$

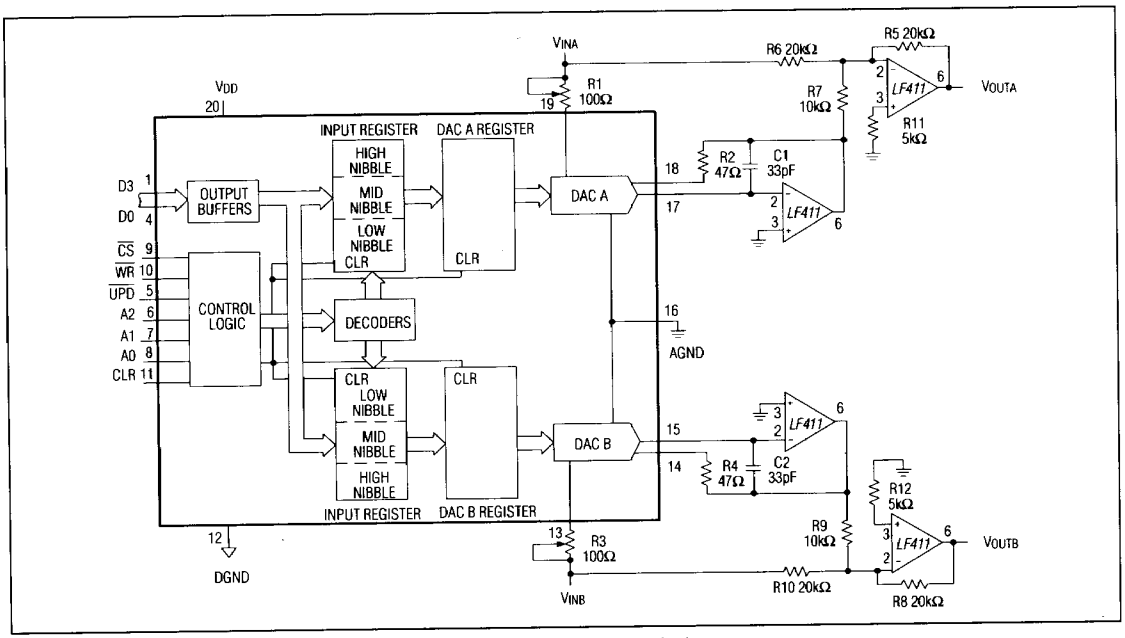

Figure 4. Dual DAC Bipolar Offset Binary Operation (Four-Quadrant Multiplication)

Application Hints

Temperature Coefficients

The MX7549 has a maximum gain temperature coefficient (TC) of ±5ppm/°C. If the trim resistors in Figures 3 or 4 are used to adjust full-scale gain error, consider their TC as part of total gain error over the temperature range. Select resistors R5, R6, and R7 (R8, R10, R9) so all ratios match to 0.01% and have low-temperature coefficients (e.g. RN-type metal film).

Digital Feedthrough

The digital inputs to the MX7549 are normally connected directly to the µP bus. Even when the device is not selected, these inputs will be constantly changing. The high-frequency logic activity on the bus can feed through the DAC package capacitance to show up as noise on the DAC output. Care should be taken in routing the PC board layout and selecting decoupling components to minimize noise.

Output Amplifier

The output amplifier's offset voltage (V_{OS}) adds to the DAC's nonlinearity. To minimize the effect of V_{OS} and maintain monotonicity, V_{OS} should be less than $(25 \times 10^{-6})(V_{REF})$ over the operating temperature range. The LF430 has a maximum V_{OS} of 5µV over temperature and is ideal for low-bandwidth applications. The LF411 has a 15V/sec slew rate with a wide bandwidth and is recommended for multiplying applications.

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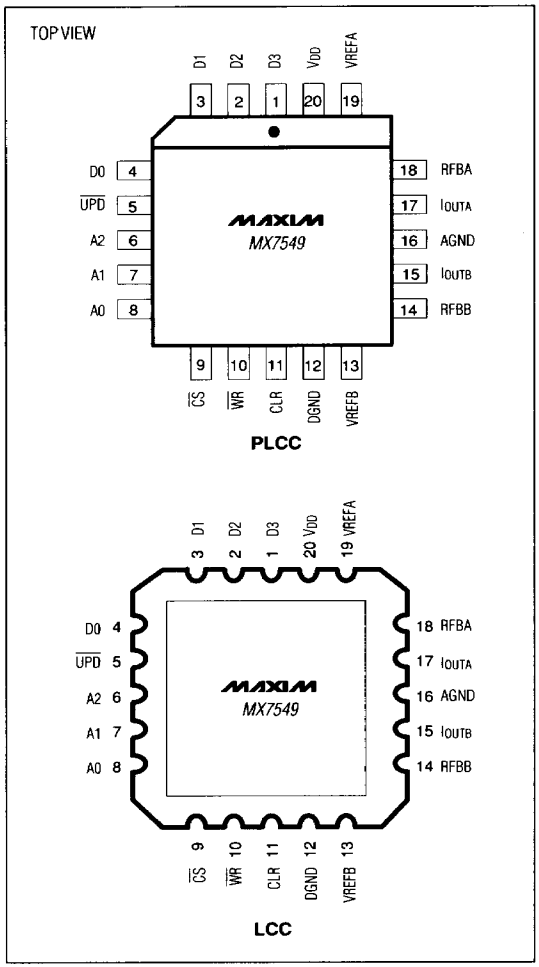
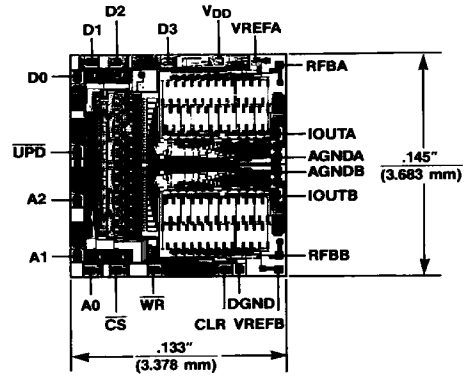
Pin Configurations (continued)



Chip Topography



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