Central™
Semiconductor Corp.

PROCESS CP701

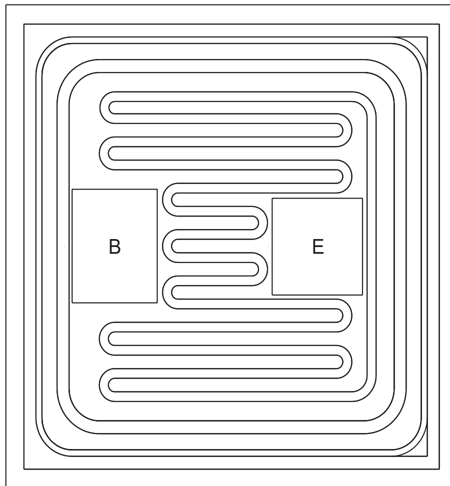
Small Signal Transistors

PNP - High Voltage Transistor Chip

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	26 x 26 MILS
Die Thickness	9.0 MILS
Base Bonding Pad Area	6.1 x 4.9 MILS
Emitter Bonding Pad Area	5.2 x 5.2 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Au - 18,000Å

GEOMETRY



BACKSIDE COLLECTOR

GROSS DIE PER 4 INCH WAFER

16,880

PRINCIPAL DEVICE TYPES

CMPT6520
CMPTA92
CXTA92
CZTA92
MPSA92

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