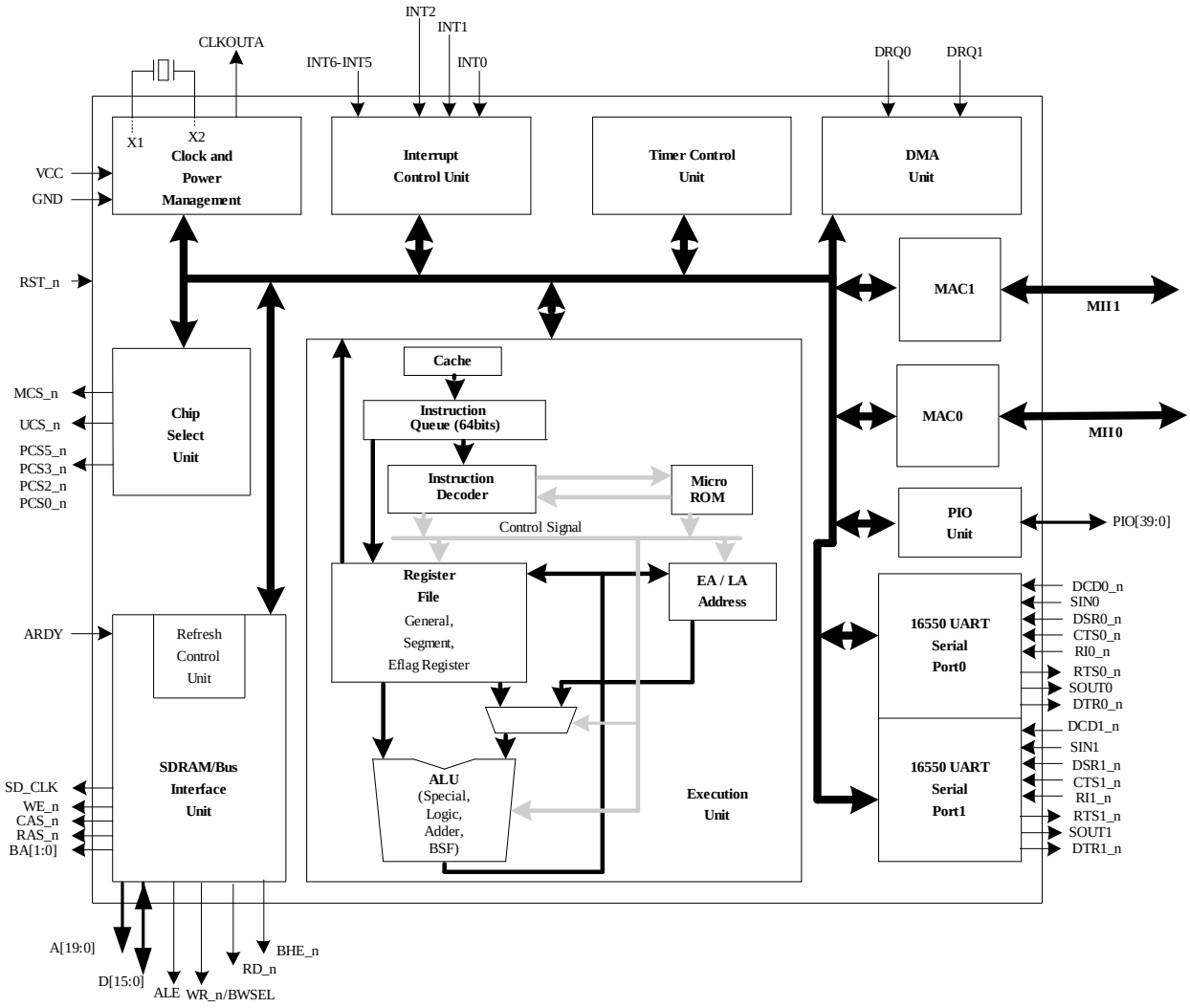
R1621
Brief Sheet
FAST ETHERNET RISC PROCESSOR

1. Features

- CPU Core
  - RDC's proprietary RISC architecture
  - Five-stage pipeline
  - Operation frequency: 100MHz
  - Supports an 8K-byte uniform cache
  - Supports CPU ID
  - Supports 40 PIO pins
- Bus Interface
  - Supports non-multiplexed address bus A[19:0]
  - With 8-bit or 16-bit boot ROM bus size
  - Supports an independent data / address bus for external I / O devices
  - 8-bit or 16-bit external bus dynamic access
- PCMCIA Bus Interface
  - Supports a glueless and simplified 16-bit PCMCIA bus interface
- ROM/RAM/SDRAM Controller and Addressing Space
  - Supports 16-bit data bus [15:0]
  - 1M-byte memory address space Address[19:0]
  - SDRAM control interface
  - 64K-byte I / O space
- Compatible UART Channels
  - Supports two compatible UART serial channels with 16-byte FIFOs and hardware flow-control
- Two independent DMA channels
- Fast Ethernet MAC Ports
  - 2-port Fast Ethernet MAC with MII interface
  - The MAC packet buffer is cacheable with snooping function
- Interrupt Controller
  - The interrupt controller with five maskable external interrupts
- Programmable Chip-select Logic
  - Programmable chip-select logic for memory or I / O bus cycle decoder
- Programmable Wait-state Generators
- Counter/Timers
  - Three independent 16-bit timers and one independent programmable watchdog timer
- Operating Voltage Range
  - Core voltage: 2.5V ± 5%
  - I / O voltage: 3.3V ± 10%
- Package Type

  128-pin PQFP

2. Block Diagram



3. Package Information

PQFP 128 pins