silicon systems®
A TDK Group Company

SSI 32R2512R
+5V, 4-Channel Thin Film Read/Write Device

Advance Information

January 1996

3

DESCRIPTION

The SSI 32R2512R is a BiCMOS monolithic integrated circuit designed for use with two-terminal recording heads. It provides a low noise read amplifier, write current control, and data protection circuitry for up to four channels. The SSI 32R2512R option provides internal 250Ω damping resistors. Damping resistors are switched in during write mode and switched out during read mode. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by making the read channel outputs high impedance. The device also offers multiple channel "servo bank write" capability to assist in servo writing operations.

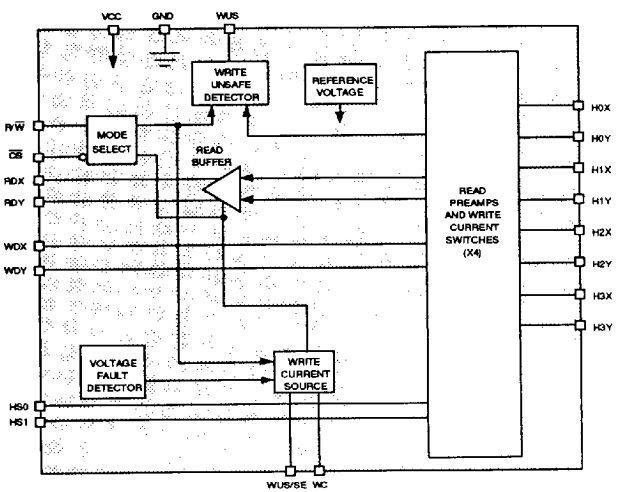
The SSI 32R2512R requires only a +5V power supply and is available in a variety of packages.

FEATURES

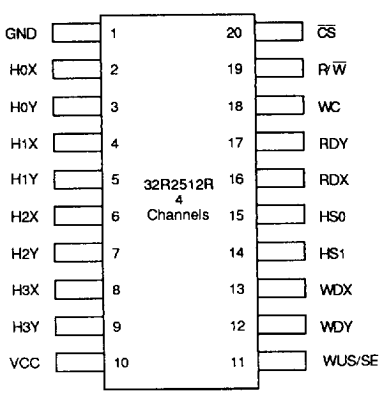
- **+5V ±10% supply**
- **Low power**
  - **PD = 165 mW read mode (Nom)**
  - **PD = 1.0 mW Idle (Max)**
- **High Performance:**
  - **Read mode gain = 350 V/V**
  - **Input noise = 0.45 nV/√Hz (Nom)**
  - **Input capacitance = 8 pF (Nom)**
  - **Write current range = 3-15 mA**
  - **Nominal write current (10 mA) rise/fall time = 3.5 ns (Nom) (typical head)**
  - **Head voltage swing = 7.8 Vp-p (Nom)**
- **Servo bank-write capability**
- **Self switching damping resistance**
- **Write unsafe detection**

(continued)

BLOCK DIAGRAM



PIN DIAGRAM



20-Lead SOV, SOL

CAUTION: Use handling procedures necessary for a static sensitive component.

FEATURES (continued)

- Power supply fault protection
- Head short to ground protection
- Differential ECL-like write data inputs

FUNCTIONAL DESCRIPTION

The SSI 32R2512R has the ability to address up to 4 two-terminal heads and provide write drive or read amplification. Mode control and head selection are described in Tables 1 and 2. The TTL inputs R/$\overline{W}$ and $\overline{CS}$ have internal pull-up resistors to prevent an accidental write condition. HS0 and HS1 have internal pull down resistors. Internal clamp circuitry will protect the IC from a head short to ground condition in any mode.

TABLE 1: Mode Select

$\overline{CS}$	R/$\overline{W}$	WUS/SE	Mode
0	0	*	Single Channel Write. See Table 2.
0	0	**	Servo Write.
0	1	X	Single Channel Read. See Table 2.
1	X	X	Idle.

* WUS/SE is a WUS output unless pulled above Vcc.

** Servo write mode is activated through the WUS pin as described in the servo write mode section.

TABLE 2: Head Select

HS1	HS0	Head
0	0	0
0	1	1
1	0	2
1	1	3

TABLE 3: Head Select in Servo Write Mode

Head Select Address		Head Selected in
HS1*	HS0	Servo Write Mode
0	0	None
0	1	0, 1, 2, 3
1	0	None
1	1	None

* Note: For 2-channel parts, HS1 = 0.

WRITE MODE

Taking both $\overline{CS}$ and R/$\overline{W}$ low selects write mode which configures the SSI 32R2512R as a current switch and activates the Write Unsafe (WUS) detector circuitry. The 32R2512R head current is toggled between the X and Y side of the head on each WDX–WDY transition. When the potential of WDX is higher than WDY, the potential on the X side of the head is higher than the Y-Side (HNY is sinking current). The magnitude of the write current (0-pk) is given by:

$$Iw = Aw \cdot \frac{Vwc}{Rwc} = K/Rwc$$

where Aw is the write current gain.

RWC is connected from pin WC to GND. Note the actual head current Ix, y is given by:

$$Ix, y = \frac{Iw}{1 + Rh/Rd}$$

Where:

Rh = Head resistance plus external wire resistance

Rd = Damping resistance

In write mode a 250Ω damping resistor is switched in across the Hx, Hy ports.

SERVO WRITE MODE

This mode allows for writing to multiple channels at once, which is useful during servo formatting.

To enable servo write mode follow these steps:

(1) Place the device in the read mode (R/W high).

(2) Set the head select lines to an address that corresponds to the bank of heads desired for servo write (See Tables 2 and 3).

(3) Pull the WUS output above Vcc by sourcing 10 mA of current into the pin. Two ways to source this current are: (a) use a voltage source set to Vcc +1.9 volts limited to 10 mA current, or (b) use a resistor tied between WUS and a supply above Vcc to source the current. With 10 mA of current, WUS will rise to approximately Vcc + 1.5 volts.

(4) Allow at least 1 µs setup.

(5) While maintaining steps (2) and (3) above make R/W low, placing the device in servo write mode.

POWER SUPPLY FAULT PROTECTION

A voltage fault detection circuit improves data security by disabling the write current generator during a voltage fault or power startup regardless of mode. Note that WUS does not necessarily turn on to flag a power supply fault condition.

HEAD SHORT TO GROUND PROTECTION

The SSI 32R2512R provides a head short to ground protection circuit in write mode. If the selected head is shorted to ground the write current generator will turn off, the WUS flag will go high, and current will be limited to less than 1 mA out of the head port. Note that any unselected head is pulled to ground through internal circuitry. In the idle mode, all heads are similarily pulled to ground.

In read mode, current out of the selected head port will not exceed 3 mA if the head is shorted to ground.

WRITE UNSAFE

Upon entering write mode, WUS is initialized low. Any of the following conditions will be indicated as a high level on the Write Unsafe, WUS, open collector output.

- Write data frequency too low
- Device in read mode
- Device not selected
- No head current
- Open head
- Head short to ground

To insure no false WUS trigger, the product of head current and head resistance (Iw • Rh) should be less than [0.14 (Iw) - 0.2] V, where Iw is in mA, for Iw range from 3 mA to 15 mA. The open head detect circuit is also disabled when write data frequency is above 10 MHz to prevent false WUS detect.

WD frequency too low is detected if the write data frequency falls below 500 kHz. Consult the WUS Safe to Unsafe timing for range of frequency detection.

Device in read mode, Device in servo write mode and **Chip disabled** will flag WUS if R/$\overline{W}$ is high, if servo write mode is activated, or $\overline{CS}$ is high.

No head current will flag WUS if Rwc = ∞ and the selected head is present.

WRITE UNSAFE (continued)

Head opened will flag WUS if Rh = ∞ and the write data frequency is less than 10 MHz.

Head short to ground is described in the preceding paragraph.

READ MODE

The read mode configures the SSI 32R2512R as a low noise differential amplifier and deactivates the write current generator. The damping resistor is switched out of the circuit allowing a high impedance input to the read amplifier. The RDX and RDY output are driven by emitter followers. They should be AC coupled to the load. The HnX, HnY inputs are non-inverting to the RDX, RDY outputs.

Note that in idle or write mode, the read amplifier is deactivated and RDX, RDY outputs become high impedance. This facilitates multiple R/W applications (wired-OR RDX, RDY) and minimizes voltage change when switching from write to read mode. Note also that the write current source is deactivated for both the read and idle mode.

IDLE MODE

Taking $\overline{CS}$ high selects the idle mode which switches the RDX and RDY outputs into a high impedance state and deactivates the device. Power consumption in this mode is held to a minimum.

PIN DESCRIPTION

CONTROL/STATUS

NAME	TYPE	DESCRIPTION
$\overline{CS}$	I	Chip Select Input: A logical low level enables the device. This pin has an internal pull up.
R/$\overline{W}$†	I	Read/Write: A logical high level enables read mode. A logical low level enables write mode. This pin has an internal pull up.
HS0, HS1	I	Head Select: Decoded address (internal pull down) selects one of 4 channels. See Table 2.
WUS/SE†	I/O	Write Unsafe/Servo Enable: When in Servo Bank write mode, pulling this pin above Vcc enables servo bank write. See Servo write mode section. Otherwise, a high level indicates an unsafe writing condition. See WUS section.
WC†	I	Write Current: A resistor to ground from WC sets the write current through the recording head.

HEAD TERMINAL CONNECTIONS

H0X-H3X H0Y-H3Y	I	X, Y Head Connections

DATA INPUT/OUTPUT

WDX, WDY	I	Differential Write Data In: Each transition of WDX–WDY changes the direction of current in the recording head.
RDX, RDY†	O	Differential Read Data Out: Emitter follower output.

POWER

VCC	I	+5V power supply
GND	I	Ground

† When more than one Read/Write device is used, signals can be wire OR'ed.

ELECTRICAL SPECIFICATIONS

Current maximums are currents with the highest absolute value.

ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may damage the device.

PARAMETER			RATING
DC Supply Voltage		VCC	-0.3 to 6 VDC
Write Current		Iw	65 mA
Digital Input Voltage		Vin	-0.3 to VCC + 0.3 VDC
Head Port Voltage		VH	-0.3 to VCC + 0.3 VDC
WUS Pin Voltage		Vwus	7.5 VDC
Output Current	RDX,RDY	Io	-10 mA
	WUS	Iwus	+15 mA
Junction Operating Temperature		Tj	+125°C
Storage Temperature			-65 to +150°

RECOMMENDED OPERATING CONDITIONS

DC Supply Voltage	VCC	5 ± 10%V
Ambient Operating Temperature	Ta	0°C < Ta < 70°C

TEST CONDITIONS

Recommended operating conditions apply.

Write Current	Iw	10 mA
Head Inductance	Lh	0.625 µH
Head Resistance	Rh	35Ω
WD Frequency		5 MHz
WDX, WDY rise/fall time		1 ns

POWER DISSIPATION

Recommended operating conditions apply.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
VCC Supply Current	Read mode		33	44	mA
	Write mode* Iw = 10 mA		32	45	mA
	Idle mode		0.04	0.2	mA
Power Dissipation	Read mode		165	242	mW
	Write mode Iw = 10 mA		160	248	mW
	Idle mode		0.2	1	mW

DIGITAL INPUTS

Input High Voltage HSX, $\overline{CS}$, R/$\overline{W}$	Vih		2		VDC
Input Low Voltage HSX, $\overline{CS}$, R/$\overline{W}$	Vil			0.8	VDC
Input High Current HSX, $\overline{CS}$, R/$\overline{W}$	Iih	Vih = 2V		100	µA
Input Low Current HSX, $\overline{CS}$, R/$\overline{W}$	Iil	Vil = 0.8V	-0.4		mA
WDX, WDY, Input High Voltage	Vih		Vcc - 1.1	Vcc - 0.4	VDC
WDX, WDY, Input Low Voltage	Vil		Vih - 2	Vih - 0.25	VDC
WDX, WDY, Input High Current		Vih = Vcc-0.4V		2	50	µA
WDX, WDY, Input Low Current		Vih = Vcc-1.45V	-50	0	50	µA
WUS Output Low Voltage	Vol	Iol = 2 mA max		0.2	0.5	VDC

* Icc = 20 + 1.1 • Iw

ELECTRICAL SPECIFICATIONS (continued)

WRITE CHARACTERISTICS

Test conditions apply unless otherwise specified.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Write Current Range		3		15	mA
Write Current Voltage Vwc		2.25	2.5	2.75	V
Write Current Gain Aw	Iw = Aw • Vwc/Rwc		20		mA/mA
Write Current Constant "K"	Iw = K/Rwc	45	50	55	V
Differential Head Voltage Swing	Open Head, Iw =10 mA	6.5	7.8		Vp-p
Head Differential Load Resistance Rd		200	250	300	Ω
WD Pulse Width (See Figure 1)	PWH	1			ns
	PWL	1			ns
Unselected Head Transient Current				1.5	mA (pk)
Unselected Head Voltage			0	0.1	VDC
Unselected Head Current	DC	-0.1	0	0.1	mA
VCC Fault Voltage	Iw ≤ 0.2 mA	3.5	3.9	4.2	V
Head Current HnX, HnY	Vcc fault condition	-200		200	µA

SERVO WRITE CHARACTERISTICS

Write Current Range		3		15	mA
Write Current Matching	Between channels		±10%		
WUS/SE Voltage	Servo Bank Write Enabled		Vcc + 1.5	Vcc + 1.9	V
WUS/SE Sink Current	Servo Bank Write Enabled	10			mA

READ CHARACTERISTICS

Test conditions apply unless otherwise specified. CL (RDX, RDY) < 20 pF, RL (RDX, RDY) = 1 kΩ.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Differential Voltage Gain	Vin = 1 mVp-p @1 MHz	280	350	420	V/V
Voltage BW -1 dB	|Zs| < 5Ω, Vin = 1 mVp-p	45	55		MHz
-3 dB		95	110		MHz
Input Noise Voltage	BW = 15 MHz, Lh = 0, Rh = 0		0.45	0.60	nV/√Hz
Input Noise Current			4	20	pA/√Hz
Differential Input Capacitance	Vin = 1 mVp-p, f = 5 MHz	8	10	12	pF
Differential Input Resistance	Vin = 1 mVp-p, f = 5 MHz	500	850		Ω
Dynamic Range	AC input voltage where gain falls to 90% of its small signal gain value, f = 5 MHz	2	9		mVp-p
Common Mode Rejection Ratio	Vin = 0 VDC + 100 mVp-p @ 5 MHz	50	70		dB
Power Supply Rejection Ratio	100 mVp-p @ 5 MHz on Vcc	50	70		dB
Channel Separation	Unselected channels driven with Vin = 0 VDC + 100 mVp-p	50	60		dB
Output Offset Voltage	Lh = 0, Rh = 0	-350		+350	mV
Single Ended Output Resistance	f = 5 MHz		35	50	Ω
Output Current	AC coupled load, RDX to RDY	2	2.8		mA
RDX, RDY Common Mode Output Voltage			Vcc - 2.7		VDC

ELECTRICAL SPECIFICATIONS (continued)

SWITCHING CHARACTERISTICS

Test conditions apply unless otherwise specified.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Read to Write	R/$\overline{W}$	R/$\overline{W}$ to 90% of write current		0.06	0.2	µs
Write to Read		R/$\overline{W}$ to 90% of 100 mV Read signal envelope		0.1	0.2	µs
Unselect to Select	$\overline{CS}$	CS to 90% of 100 mV 10 MHz Read signal envelope		0.08	0.2	µs
Select to Unselect		CS to 10% of write current		0.04	0.2	µs
HS0,1 to any Head		To 90% of 100 mV 10 MHz Read signal envelope		0.06	0.2	µs
Safe to Unsafe (TD1)	WUS	Write mode, loss of WDI, WD transitions; Defines max WDI, WD period for WUS operation	1.4	2	2.6	µs
Unsafe to Safe (TD2)		Fault cleared: from first negative WDI transition		0.17	0.6	µs
WD to Ix - Iy (TD3)		From 50% points (Lh = 0, Rh = 0)		4.5	7	ns
Asymmetry		WDI has 1 ns rise/fall time (Lh = 0, Rh = 0)		0.1	0.5	ns
Rise/fall Time		10% to 90% points Iw = 15 mA, Rh = 0, Lh = 0		1	2	ns
		Iw = 10 mA, Rh = 35Ω, Lh = 0.625 µH		3.5	4.5	ns
		Iw = 12 mA, Rh = 32Ω, Lh = 0.48 µH		3.0	4.0	ns

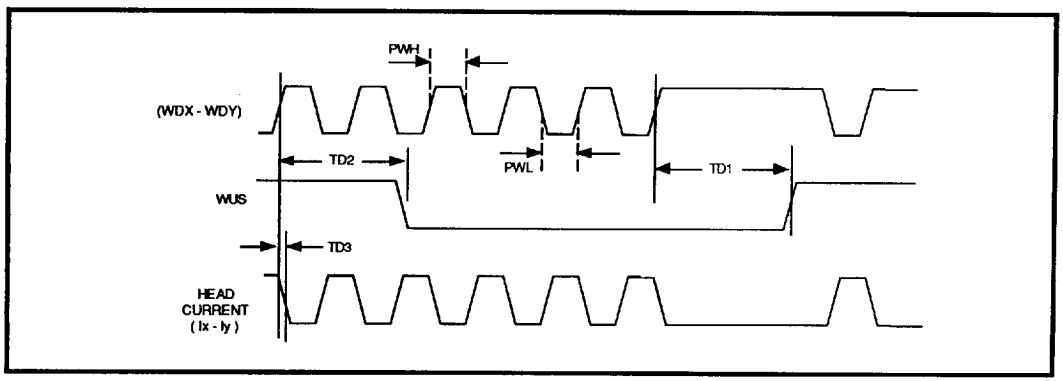
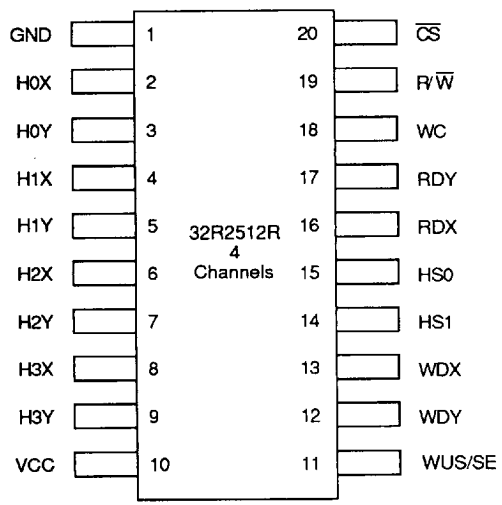


FIGURE 1: 32R2512R Write Mode Timing Diagram

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.

3



20-Lead SOV, SOL

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914