IC WORKS

700-782

W42C70

Zero Delay Buffer

ADVANCE INFORMATION, JANUARY 1995

FEATURES

- On chip Phase Locked Loop for clock synchronization
- Synchronizes frequencies up to 120 MHz (output)
- ±1ns skew (max) between input and output clocks
- Can recover poor duty cycle clocks
- CLK1 and CLK2 skew controlled to within ±1ns
- Single 5 volt power supply
- Low power CMOS technology
- Small 8 pin DIP or SOIC package
- On chip loop filter
- W42C70-01, -04 for output clocks 10-120 MHz
- W42C70-02, -05 for output clocks 2.5-30 MHz

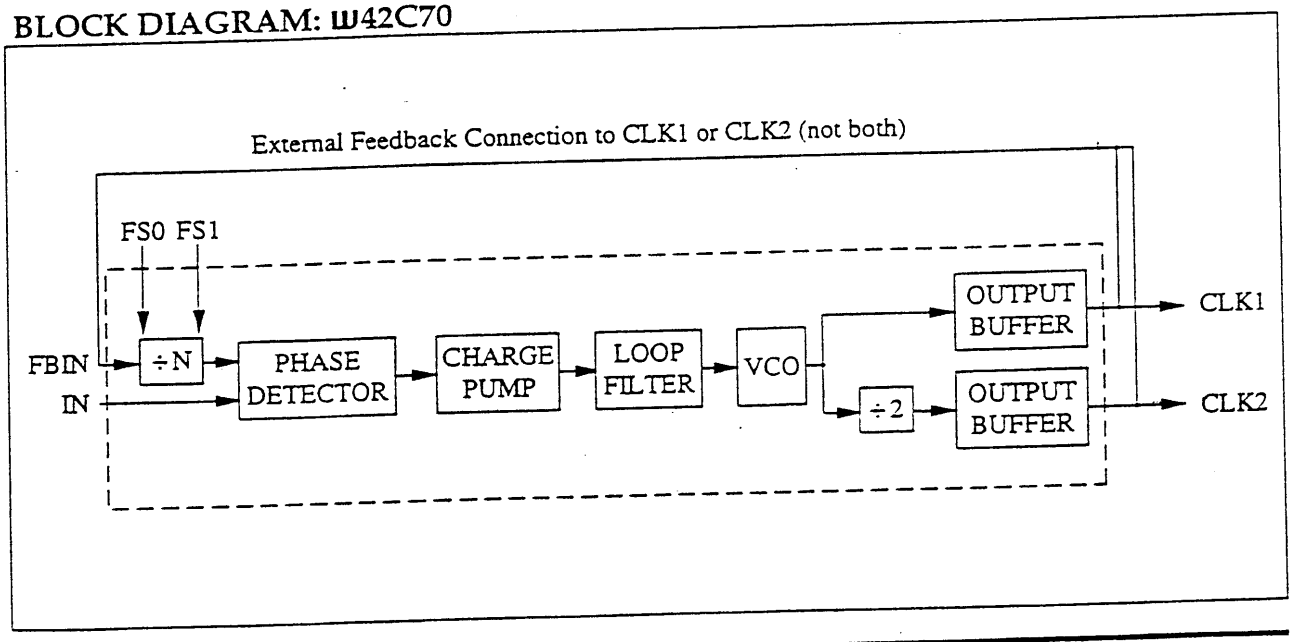
DESCRIPTION

The W42C70 generates an output clock which is synchronized to a given continuous input clock with zero delay (±1ns). Using IC WORKS' proprietary phase locked loop (PLL) analog CMOS technology, the W42C70 is useful for regenerating clocks in high speed systems where skew is a major concern. By the use of the two select pins, multiples or divisions of the input clock can be generated with zero delay (see Tables 2 and 3). The standard versions produce two outputs, where CLK2 is always a divide by two version of CLK1.

The W42C70 is also useful to recover poor duty cycle clocks. A 50 MHz signal with a 20/80% duty cycle, for example, can be regenerated to the 48/52% typical of the part.

The W42C70 allows the user to control the PLL feedback, making it possible, with an additional 74F240 octal buffer (or other such device that offers controlled skew outputs), to synchronize up to 8 output clocks with zero delay compared to the input (see Figure 1).

BLOCK DIAGRAM: W42C70



PIN DESCRIPTIONS

Pin Name	Pin #	Type	Description
FBIN	1	Input	FEEDBACK INPUT
IN	2	Input	INPUT for reference clock
GND	3	-	GROUND
FS0	4	Input	FREQUENCY SELECT 0
FS1	5	Input	FREQUENCY SELECT 1
CLK1	6	Output	CLOCK output 1 (See Tables 1, 2, 3, 6, 7 for values)
VCC	7	-	Power Supply (+5V)
CLK2	8	Output	CLOCK output 2 (See Tables 1, 2, 3, 6, 7 for values)

PIN CONFIGURATION: W42C70

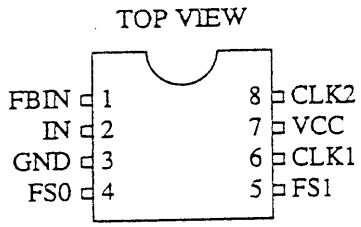


TABLE 1

FS1	FS0	f_{FBIN}(-01,-02)	f_{FBIN}(-04,-05)
0	0	$2 \cdot f_{IN}$	$3 \cdot f_{IN}$
0	1	$4 \cdot f_{IN}$	$5 \cdot f_{IN}$
1	0	f_{IN}	$6 \cdot f_{IN}$
1	1	$8 \cdot f_{IN}$	$10 \cdot f_{IN}$

USING THE W42C70

The W42C70 has the following characteristics:

1. Rising edges at IN and FBIN are lined up. Falling edges are not synchronized.
2. The relationship between the frequencies at FBIN and IN is shown in Table 1.
3. The frequency of CLK2 is half the CLK1 frequency.
4. The CLK1 frequency ranges are:

W42C70-01, 04 $10 < f_{CLK1} < 120MHz$
W42C70-02, -05 $2.5 < f_{CLK1} < 30MHz$

The W42C70 will only operate correctly within these frequency ranges.

ELIMINATE HIGH SPEED CLOCK ROUTING PROBLEMS

The ɯ42C70 makes it possible to route lower speed clocks over long distances on the PC board, and to place a ɯ42C70 next to the device requiring a higher speed clock. The multiplied output can then be used to produce a phase locked, higher speed output clock.

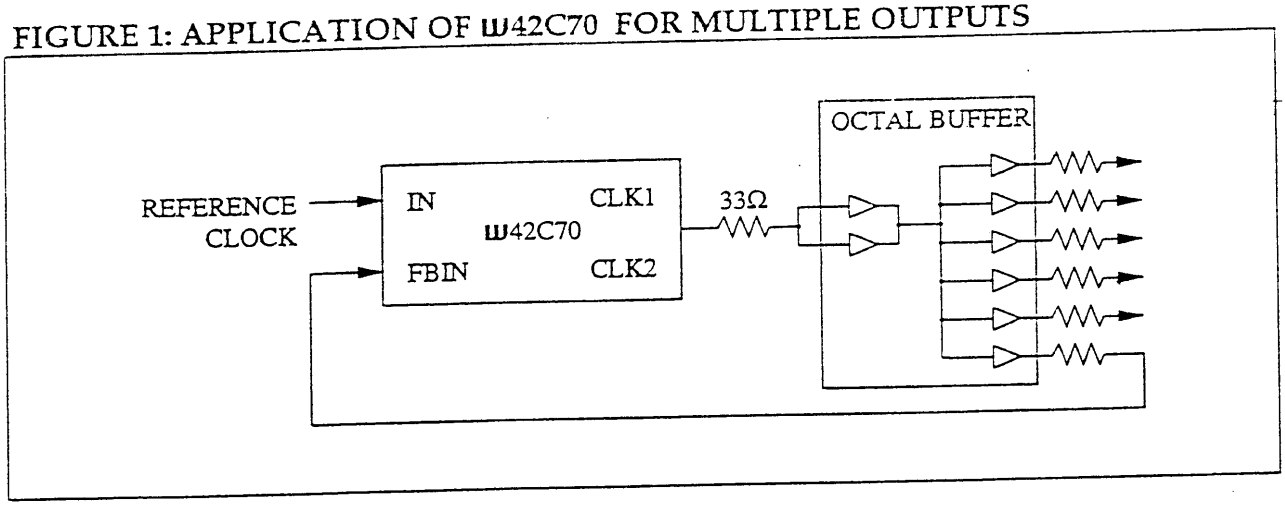
COMPENSATE FOR PROPAGATION DELAYS

Including ɯ42C70 in a timing loop allows the use of PALs, gate arrays, etc., with loose timing specifications. The ɯ42C70 compensates for the delay through the PAL and synchronizes the output to the input reference clock.

OPERATING FREQUENCY RANGE

The ɯ42C70 is offered in versions optimized for operation in two frequency ranges. The -01 and -04 cover high frequencies, 10 to 120 MHz. The -02 and -05 operate from 2.5 to 30 MHz. The ɯ42C70 can be supplied with custom multiplication factors and operating ranges. Consult IC WORKS for details.

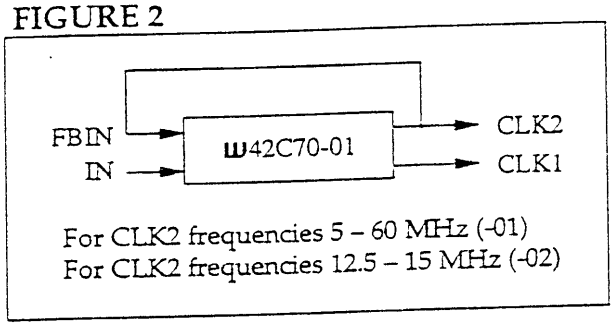
FIGURE 1: APPLICATION OF ɯ42C70 FOR MULTIPLE OUTPUTS



USING CLK2 FEEDBACK

Connecting CLK2 to FBIN as shown in Figure 2 will cause all of the rising edges to be aligned (Fig. 3).

FIGURE 2

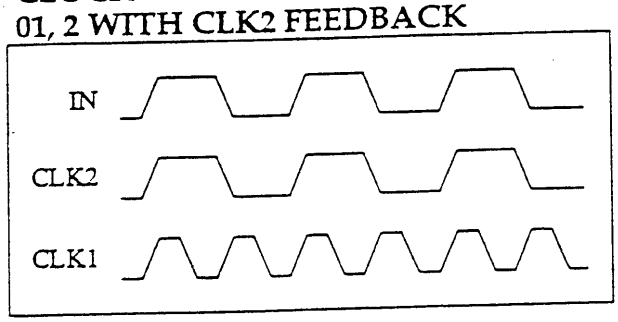


For CLK2 frequencies 5 – 60 MHz (-01)
For CLK2 frequencies 12.5 – 15 MHz (-02)

TABLE 2: DECODING TABLE FOR ω42C70-01, 2 WITH CLK2 FEEDBACK

FS1	FS0	CLK1	CLK2
0	0	INx4	INx2
0	1	INx8	INx4
1	0	INx2	IN
1	1	INx16	INx8

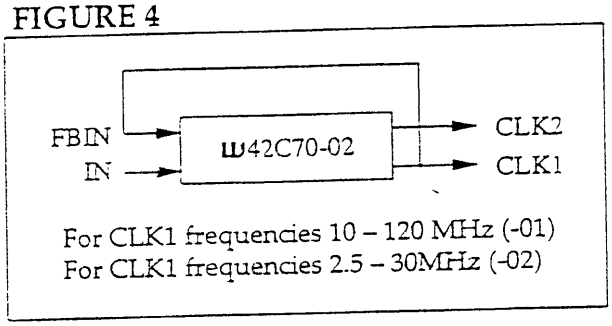
FIGURE 3: INPUT AND OUTPUT CLOCK WAVEFORMS FOR ω42C70-01, 2 WITH CLK2 FEEDBACK



USING CLK1 FEEDBACK

With CLK1 connected to FBIN as shown in Figure 4, the input and CLK1 output will be aligned on the rising edge, but CLK2 can be either rising or falling (Fig. 5).

FIGURE 4

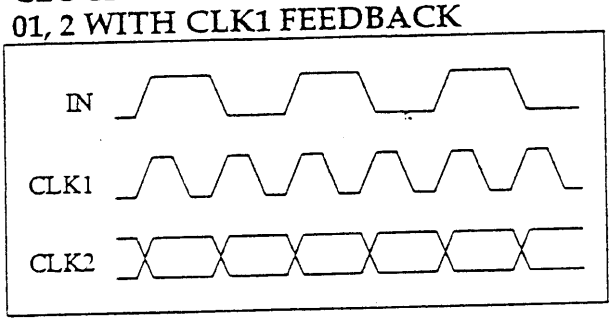


For CLK1 frequencies 10 – 120 MHz (-01)
For CLK1 frequencies 2.5 – 30MHz (-02)

TABLE 3: DECODING TABLE FOR ω42C70-01, 2 WITH CLK1 FEEDBACK

FS1	FS0	CLK1	CLK2
0	0	INx2	IN
0	1	INx4	INx2
1	0	IN	IN÷2
1	1	INx8	INx4

FIGURE 5: INPUT AND OUTPUT CLOCK WAVEFORMS FOR ω42C70-01, 2 WITH CLK1 FEEDBACK



USING CLK2 FEEDBACK

Connecting CLK2 to FBIN as shown in Figure 6 will cause all of the rising edges to be aligned (Fig. 7).

FIGURE 6

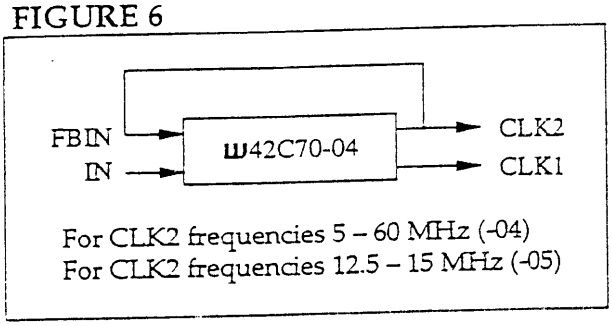
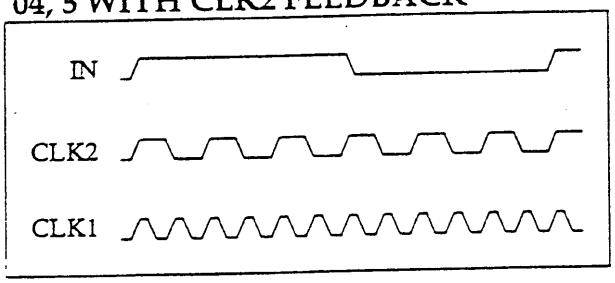


TABLE 4: DECODING TABLE FOR ɯ42C70-04, 5 WITH CLK2 FEEDBACK

FS1	FS0	CLK1	CLK2
0	0	INx6	INx3
0	1	INx10	INx5
1	0	INx12	INx6
1	1	INx20	INx10

FIGURE 7: INPUT AND OUTPUT CLOCK WAVEFORMS FOR ɯ41C70-04, 5 WITH CLK2 FEEDBACK



USING CLK1 FEEDBACK

With CLK1 connected to FBIN as shown in Figure 8, the input and CLK1 output will be aligned on the rising edge, but CLK2 can be either rising or falling (Fig. 9).

FIGURE 8

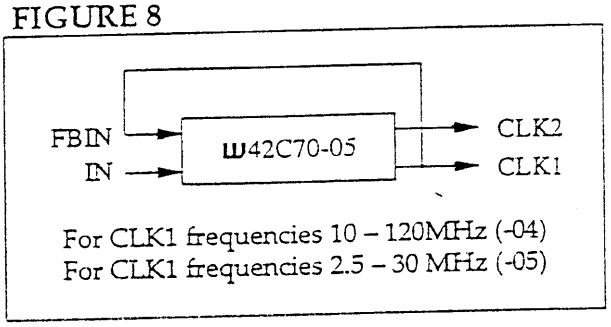
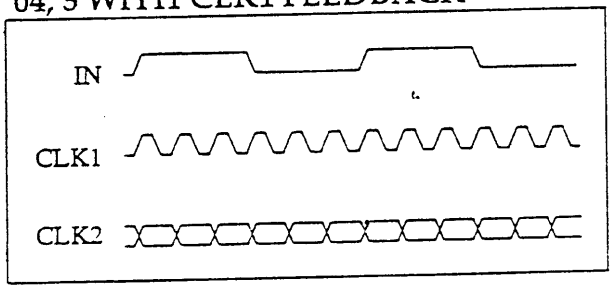


TABLE 5: DECODING TABLE FOR ɯ42C70-04, 5 WITH CLK1 FEEDBACK

FS1	FS0	CLK1	CLK2
0	0	INx3	INx1.5
0	1	INx5	INx2.5
1	0	INx6	INx3
1	1	INx10	INx5

FIGURE 9: INPUT AND OUTPUT CLOCK WAVEFORMS FOR ɯ42C70-04, 5 WITH CLK1 FEEDBACK



ABSOLUTE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Rating	Unit
VCC referenced to GND	T_{STG}	7	V
Operating Temperature Under Bias		0 to +70	°C
Storage Temperature		-65 to +150	°C
Voltage on I/O Pins Referenced to Ground		-0.5 to +0.5	V
Power Dissipation		0.5	Watts

Note 1: Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A=0°C to 70°C unless otherwise stated)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Low Voltage	V_{IL}	V_{CC} = 5V	-	-	0.8	V
Input High Voltage	V_{IH}	V_{CC} = 5V	2.0	-	-	V
Input Low Current (FS0, FS1)	I_{IL}	V_{IN} = 0V	-30 (1)	-	5	µA
Input High Current (FS0, FS1)	I_{IH}	V_{IN} = V_{CC}	-5	-	5	µA
Input Low Current (IN, FBIN)	I_{IL}	V_{IN} = 0V	-5	-	5	µA
Input High Current (IN, FBIN)	I_{IH}	V_{IN} = V_{CC}	-5	-	5	µA
Output Low Voltage	V_{OL}	I_{OL} = 12 mA	-	-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -1 mA, V_{DD} = 5.0V	V_{CC}-.4V	-	-	V
Output High Voltage	V_{OH}	I_{OH} = -4 mA, V_{DD} = 5.0V	V_{CC}-.8V	-	-	V
Output High Voltage	V_{OH}	I_{OH} = -12 mA	2.4	-	-	V
Supply Current	I_{CC}	Unloaded, 100MHz	-	20	50	mA

Note 1: Pins FS0, FS1 include an internal pull-up resistor.

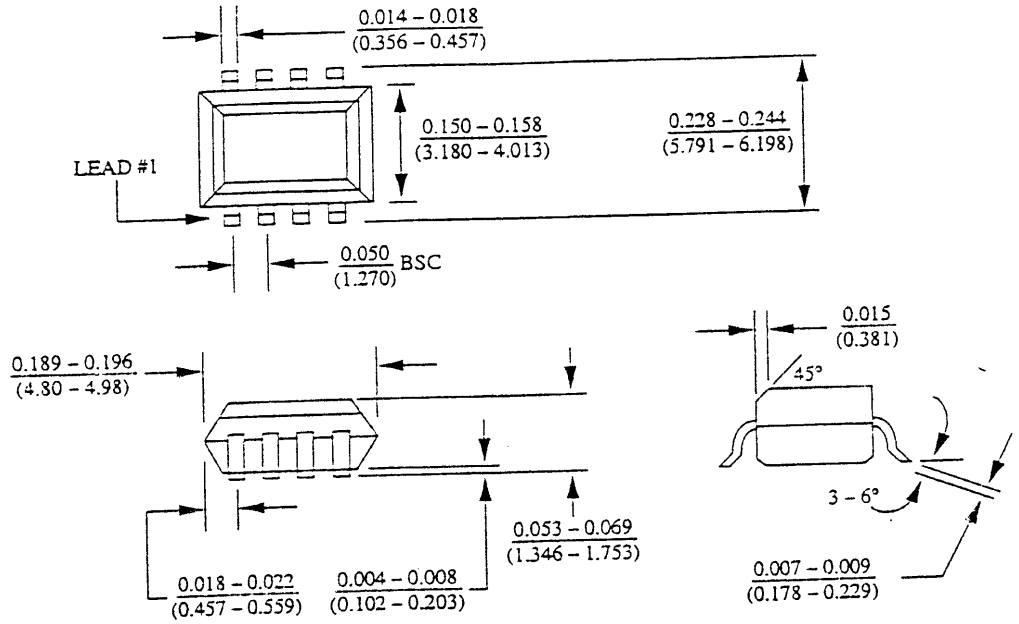
ARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
lock Rise Time. Note 1	$ICLK_r$		-	-	10	ns
lock Fall Time. Note 1	$ICLK_f$		-	-	10	ns
Rise time, 0.8 to 2.0V	t_r	15 pf load	-	1	2	ns
e, 20% to 80% V_{CC}	t_r	15 pf load	-	2	4	ns
Fall time, 2.0 to 0.8V	t_f	15 pf load	-	1	2	ns
, 80% to 20% V_{CC}	t_f	15 pf load	-	2	4	ns
Duty cycle, ω42C70-01	d_t	15 pf load. Note 2, 3	40	48/52	60	%
Duty cycle, ω42C70-02	d_t	15 pf load. Note 2, 3	45	49/51	55	%
gma	T_{1s}		-500	±120	300	ps
olute	T_{abs}	For CLK1 > 10MHz	-2%	±250	500	ps
olute	T_{abs}	For CLK1 < 10MHz			2	%
quency. Note 4	f_i		1		120	MHz
requency CLK1. Note 5	f_o	ω42C70-01, -04	10		120	MHz
requency CLK1. Note 5	f_o	ω42C70-02, -05	2.5		30	MHz
N skew	t_{skew1}	Note 2, 6. Input rise time <5ns	-1	0.4	1	ns
N skew	t_{skew1}	Note 2, 6. Input rise time <10ns	-2	0.6	2	ns
LK2 skew	t_{skew2}	Note 2, 4	-1	0.4	1	ns

ger input rise and fall time will degrade skew and jitter performance.
a.c. specifications are measured with a 50Ω transmission line, load terminated with 50Ω to 1.4V
y Cycle is measured at 1.4 V.
it frequency is limited by output frequency range and input to output frequency multiplication factor
ch is determined by circuit configuration).
ay be possible to operate the ω42C70 outside of these ranges. Consult IC WORKS for your specific
ication.
measured at 1.4V on rising edges.

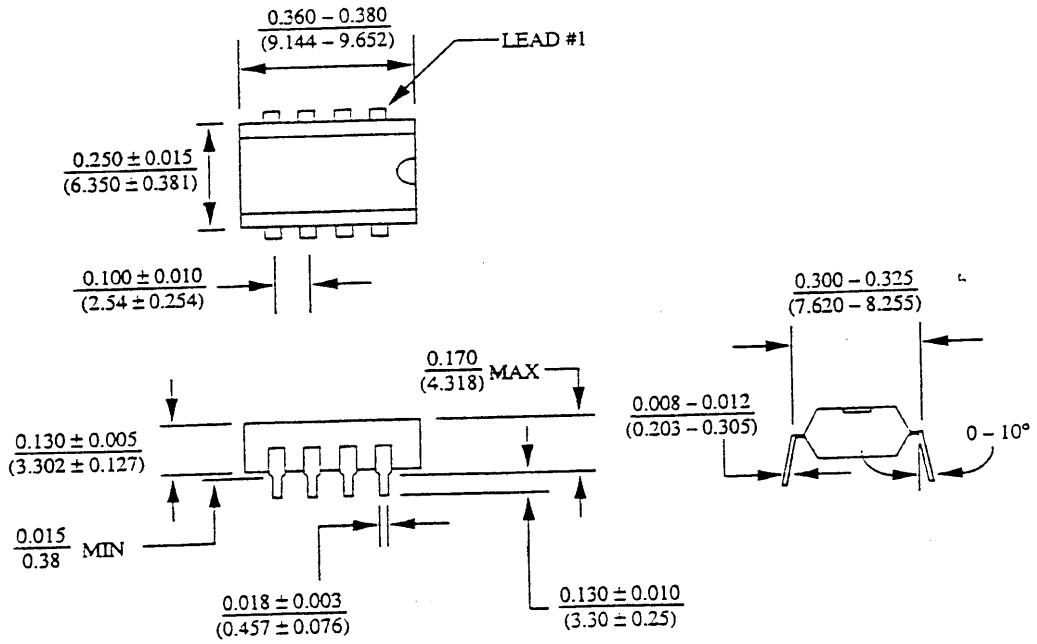
PACKAGING INFORMATION

Plastic SOIC (8 pin, 150 mil)



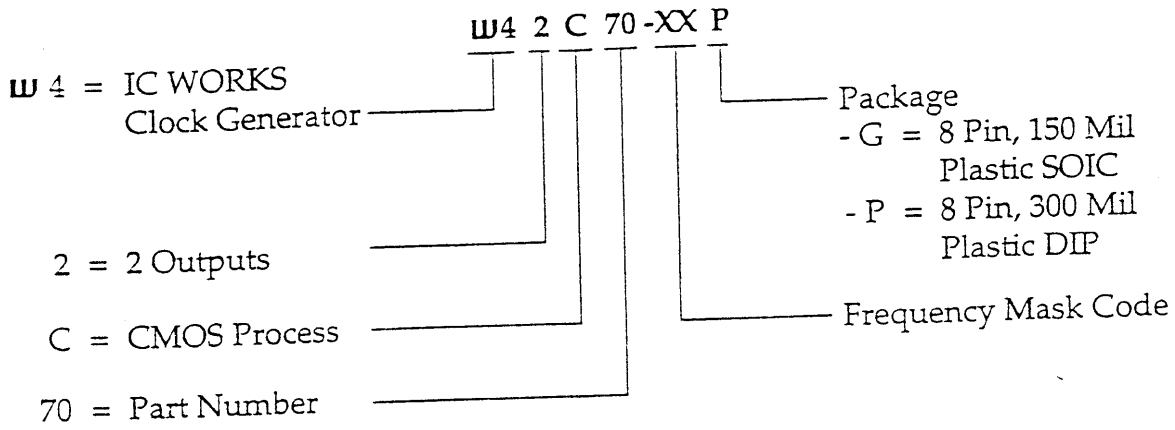
Note: All linear dimensions are in inches and parenthetically in millimeters, min–max

Plastic DIP (8 pin, 300 mil)



Note: All linear dimensions are in inches and parenthetically in millimeters, min–max

ORDERING INFORMATION



VALID PART NUMBERS

W42C70-01G	W42C70-02G	W42C70-03G	W42C70-04G	W42C70-05G
W42C70-01P	W42C70-02P	W42C70-03P	W42C70-04P	W42C70-05P

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Document No. 42C70/00/0195