REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Added device types 03 and 04. Technicial changes to 1.3 and table I. Changes to table III, and changes to reflect MIL-H-38534 processing. Editorial changes throughout.	90-10-10	G. Lude
B	Made correction to the lead length on figure 2 for case outline Y. Editorial changes throughout.	91-11-25	G. Lude
C	Add case outline Z. Make technical changes to table I. Change dimensions for case outlines X and Y. Make technical changes to figure 2, terminal connections. Editorial changes throughout.	93-03-10	K. Cottongim
D	Add case outline T. Make changes to paragraph 1.4. Make technical changes to table I. Changed package heigth for case outline X from .25 inches to .20 inches. Made corrections to the terminal connections.	93-07-27	K. Cottongim
E	Changes in accordance with NOR 5962-R077-94.	93-12-22	K. Cottongim
F	Changes in accordance with NOR 5962-R036-95.	94-11-16	K. Cottongim
G	Changes in accordance with NOR 5962-R119-95.	95-04-27	K. Cottongim
H	Correct case outline T package height dimension from .150 inches to .145 inches. Make changes to table I.	97-03-04	K. A. Cottongim

REV																				
SHEET																				
REV	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	

REV STATUS OF SHEETS	REV	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Steve L. Duncan

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APPROVED BY
Gregory A. Lude

DRAWING APPROVAL DATE
89-06-02

REVISION LEVEL
H

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216-5000

MICROCIRCUIT, HYBRID, LINEAR, MIL-STD-1553, BC/RTU/MT, MULTIPLEXED TERMINAL

SIZE	CAGE CODE	
A	**67268**	**5962-88692**

SHEET 1 OF 33

DESC FORM 193
JUL 94

1. SCOPE

1.1 Scope. This drawing describes device requirements for class H hybrid microcircuits to be processed in accordance with MIL-PRF-38534 and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN).

1.2 PIN. The PIN shall be as shown in the following example:

5962-88692	01	X	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	BUS61553, BUS61563	MIL-STD-1553, BC/RTU/MT, transceiver multiplexed terminal
02	BUS61554, BUS61564	MIL-STD-1553, BC/RTU/MT, transceiver multiplexed terminal
03	BUS61555, BUS61565	MIL-STD-1553, BC/RTU/MT, transceiver multiplexed terminal
04	BUS61556	MIL-STD-1553, BC/RTU/MT, transceiverless multiplexed terminal

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
T	See figure 1	82	Flat pack
X	See figure 1	78	Dual-in-line
Y	See figure 1	82	Flat pack
Z	See figure 1	78	Flat pack

1.2.3 Lead finish. The lead finish shall be as specified in MIL-PRF-38534.

1.3 Absolute maximum ratings. 1/

Supply voltage range:	
V_{CC} (device types 01 through 03)	-0.5 V dc to +7.0 V dc
V_{EE} (device types 01 and 02)	+0.3 V dc to -18 V dc
Logic input voltage range (V_{DD})	-0.5 V dc to +7.0 V dc
Power dissipation (P_D): 2/ 3/	
Devices type 01 and 02	810 mW
Device type 03	120 mW
Device type 04	100 mW
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}): 3/	
Devices types 01 and 02	5.7°C/W
Device type 03	112°C/W
Device type 04	11.6°C/W

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Applies up to T_C = +125°C.
3/ Hottest die.

1.4 Recommended operating conditions.

Supply voltage range:	
V_{CC} (device types 01 and 02)	+4.5 V dc to +5.5 V dc
V_{CC} (device type 03)	+4.75 V dc to +5.5 V dc
V_{EE} (device type 01)	-14.25 V dc to -15.75 V dc
V_{EE} (device type 02)	-11.40 V dc to -12.60 V dc
Logic input voltage range:	
V_{DD} (device types 01, 02, and 04)	+4.5 V dc to +5.5 V dc
V_{DD} (device type 03)	+4.75 V dc to +5.5 V dc
Minimum logic high input voltage (V_{IH})	2.2 V dc
Maximum logic low input voltage (V_{IL})	0.8 V dc
Operating frequency (F_{OP})	16.0 MHz
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbook. The following specification, standards, and handbook form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOK

DEPARTMENT OF DEFENSE

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbook are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item performance requirements for device classes D, E, G, H, and K shall be in accordance with MIL-PRF-38534. Compliance with MIL-PRF-38534 may include the performance of all tests herein or as designated in the device manufacturer's Quality Management (QM) plan or as designated for the applicable device class. Therefore, the tests and inspections herein may not be performed for the applicable device class (see MIL-PRF-38534). Futhermore, the manufacturers may take exceptions or use alternate methods to the tests and inspections herein and not perform them. However, the performance requirements as defined in MIL-PRF-38534 shall be met for the applicable device class.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram(s). The block diagram(s) shall be as specified on figure 3.

3.2.4 Timing diagram(s). The timing diagram(s) shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking of Device(s). Marking of device(s) shall be in accordance with MIL-PRF-38534. The device shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's vendor similar PIN may also be marked as listed in QML-38534.

3.6 Data. In addition to the general performance requirements of MIL-PRF-38534, the manufacturer of the device described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, for each device type listed herein. Also, the data should include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DSCC-VA) upon request.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance (original copy) submitted to DSCC-VA shall affirm that the manufacturer's product meets the performance requirements of MIL-PRF-38534 and herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Logic supply current, idle 2/	I_{DD}	V_{CC} = 5.5 V, V_{DD} = 5.5 V V_{EE} = -15 V for device type 01 and -12 V for device type 02, I_{OL1} = 3.6 mA, I_{OH1} = -400 µA, I_{OL2} = 2.0 mA, I_{OL3} = 4.0 mA, f_{IN} = 16 MHz	1,2,3	01,02	5.0	170	mA
				03	50.0	170	
				04	5.0	60	
Positive supply current, idle 3/	I_{CC1}			01,02	5.0	170	mA
				03	50.0	170	
Negative supply current, idle 4/	I_{EE1}			01,02	-5.0	-80	mA
Positive supply current, channel A = 25 percent duty cycle, channel B = idle 3/	I_{CC2}			01,02	5.0	170	mA
				03	50.0	170	
Positive supply current, channel B = 25 percent duty cycle, channel A = idle 3/	I_{CC3}			01,02	5.0	170	mA
				03	50.0	170	
Negative supply current, channel A = 25 percent duty cycle, channel B = idle 4/	I_{EE2}			01,02	-25	-130	mA
Negative supply current, channel B = 25 percent duty cycle, channel A = idle 4/	I_{EE3}			01,02	-25	-130	mA
High level output voltage 5/	V_{OH}	V_{CC} = 4.5 V, V_{DD} = 4.5 V, V_{IH} = 2.7 V, V_{IL} = 0.4 V, V_{EE} = -15 V for device type 01 and -12 V for device type 02, I_{OH} = -400 µA 6/		All	2		V

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Low level output voltage 7/	V_{OL1}	V_{CC} = 4.5 V, V_{DD} = 4.5 V, V_{IH} = 2.7 V, V_{IL} = 0.4 V, V_{EE} = -15 V for device type 01 and -12 V for device type 02 6/	I_{OL1} = 3.6 mA	1,2,3	All		0.4	V
Low level output voltage 8/	V_{OL2}		I_{OL2} = 2.0 mA				0.4	V
Low level output voltage 9/	V_{OL3}		I_{OL3} = 4.0 mA				0.4	V
High level input current 10/	I_{IH1}	V_{CC} = 5.5 V, V_{DD} = 5.5 V, V_{IN} = 2.7 V, V_{EE} = -15 V for device type 01 and -12 V for device type 02				-30	-220	µA
High level input current 11/	I_{IH2}					-20	-630	µA
High level input current 12/	I_{IH3}					-50	-200	µA
High level input current 13/	I_{IH4}					-10	10	µA
High level input current 14/	I_{IH5}					-20	20	µA
High level input current 15/	I_{IH6}					-40	-220	µA
Low level input current 7/	I_{IL1}	V_{CC} = 5.5 V, V_{DD} = 5.5 V, V_{IN} = 0.4 V, V_{EE} = -15 V for device type 01 and -12 V for device type 02				-100	-400	µA
Low level input current 11/	I_{IL2}					-35	-700	µA
Low level input current 12/	I_{IL3}					-100	-400	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Low level input current 13/	I_{IL4}	V_{CC} = 5.5 V, V_{DD} = 5.5 V, V_{IN} = 0.4 V V_{EE} = -15 V for device type 01 and -12 V for device type 02	1,2,3	All	-10	10	µA
Low level input current 14/	I_{IL5}				-20	20	µA
Receiver differential input impedance 16/ 17/	Z_{IN}	DC to 1.0 MHz	4,5,6	01,02,03	5.0		kΩ
Receiver input threshold voltage	V_{TH}	Transformer coupled			650	860	mV p-p
Receiver differential input voltage 16/ 17/	V_{IN}	DC to 1.0 MHz				40	V p-p
Receiver common mode rejection 17/ ratio	CMRR	DC to 2.0 MHz			40		dB
Transmitter differential output voltage	V_O	Transformer coupled, measured across the stub			18	27	V p-p
Transmitter sinusoidal output rise and fall time	t_r, t_f				100	300	ns
Output offset 17/ voltage	V_{OS}				-250	250	mV
Transmitter overshoot	V_{OVRSHT}				-900	900	mV
Functional test		V_{CC} = 4.5 V, V_{DD} = 4.5 V, V_{IH} = 2.7 V, V_{IL} = 0.4 V V_{EE} = -15 V for 01 and -12 V for device type 02, 6/	7,8	All			pass/fail

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Delay timing							
$\overline{\text{READYD}}$ low delay (CPU handshake) 17/	t_{d1}	V_{CC} = 4.5 V, V_{DD} = 4.5 V, V_{IH} = 2.7 V, V_{IL} = 0.4 V, V_{EE} = -15 V for device type 01 and -12 V for device type 02, I_{OH} = -400 µA, I_{OL1} = 2.6 mA, I_{OL2} = 2.0 mA, I_{OL3} = 4.0 mA, see figure 4 6/ 18/	9,10,11	All		150	ns
$\overline{\text{IOEN}}$ high delay (CPU handshake) 17/	t_{d2}					20	ns
CPU $\overline{\text{MEMWR}}$ low 17/ delay	t_{d3}					100	ns
CPU $\overline{\text{MEMOE}}$ low 17/ delay	t_{d4}					100	ns
$\overline{\text{EXTLD}}$ low delay 17/	t_{d5}				50		ns
Internal register 17/ delay (read)	t_{d6}					60	ns
Internal register 17/ delay (write)	t_{d7}					60	ns
Register data/address 17/ setup time	t_{d8}					30	ns
Register data/address 17/ hold time	t_{d9}					0	ns
Other timing							
$\overline{\text{READYD}}$ pulse width (CPU handshake)	t_{pw1}	V_{CC} = 4.5 V, V_{DD} = 4.5 V, V_{IH} = 2.7 V, V_{IL} = 0.4 V, V_{EE} = -15 V for device type 01 and -12 V for device type 02, I_{OH} = -400 µA, I_{OL1} = 2.6 mA, I_{OL2} = 2.0 mA, I_{OL3} = 4.0 mA, see figure 4 6/ 18/	9,10,11	All	50		ns
CPU $\overline{\text{MEMWR}}$ low pulse width	t_{pw2}				50		ns
$\overline{\text{EXTLD}}$ low pulse width	t_{pw3}				50		ns
$\overline{\text{READYD}}$ to $\overline{\text{STRBD}}$ release time	t_r					1.37	ns
($\overline{\text{SELECT}}$ X $\overline{\text{STRBD}}$) to IOEN 17/	t_z					1.80	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

1/ All group A subgroup testing of the same temperature may be performed concurrently.

2/ Measured at the following pins:
Case X:
Device types 01 through 04: Pin 14.
Case Y and T:
Device types 01 through 03: Pin 28.
Case Z:
Device types 01 through 03: Pin 27.

3/ Measured at the following pins:
Case X:
Device types 01 and 03: Pins 58 and 77.
Case Y and T:
Device types 01 through 03: Pins 37 and 46.
Case Z:
Device types 01 through 03: Pins 36 and 43.

4/ Measured at the following pins:
Case X:
Device types 01 and 02: Pins 18 and 39.
Case Y and T:
Device types 01 and 02: Pins 36 and 45.
Case Z:
Device types 01 through 03: Pins 35 and 42.

5/ Measured at the following pins:
Case X:
Device types 01 through 03: Pins 1 through 8, 13, 15 through 17, 22 through 31, 35, 37, 41 through 48, 52 through 57, 60 through 68, 70, 72, 73, 75, and 76.
Device type 04: Pins 1 through 8, 13, 15 through 19, 22 through 31, 35, 37 through 39, 41 through 48, 52 through 58, 60 through 68, 70, 72, 73, and 77.
Case Y and T:
Device types 01 through 03: Pins 2 through 17, 25 through 27, 29 through 35, 48 through 50, 53, 54, 56, 60, 61, 63 through 80.
Case Z:
Device types 01 through 03: Pins 1 through 16, 24 through 26, 28 through 34, 45 through 47, 50, 51, 53, 57, 58, 60 through 77.

6/ For device type 03, V_{CC} = 4.75 V and V_{DD} = 4.75 V.

7/ Measured at the following pins:
Case X:
Device types 01 through 04: Pins 1 through 8, 22 through 29, 41 through 48, and 60 through 67.
Case Y and T:
Device types 01 through 03: Pins 2 through 17 and 65 through 80.
Case Z:
Device types 01 through 03: Pins 1 through 16, and 62 through 77.

TABLE I. Electrical performance characteristics - Continued.

8/ Measured at the following pins:
Case X:
Device types 01 through 03: Pins 13, 15 through 17, 52 through 57, and 70.
Device type 04: Pins 13, 15 through 17, 52 through 58, 70, and 77.
Case Y and T:
Device types 01 through 03: Pins 25 through 27, 29 through 35, and 60.
Case Z:
Device types 01 through 03: Pins 24 through 26, 28 through 34, and 57.

9/ Measured at the following pins:
Case X:
Device types 01 through 03: Pins 30, 31, 35, 37, 68, 72, 73, 75, and 76.
Device type 04: Pins 18, 19, 30, 31, 35, 38, 39, 68, 72, 73, 75, and 76.
Case Y and T:
Device types 01 through 03: Pins 48 through 50, 53, 54, 56, 61, 63, and 64.
Case Z:
Device types 01 through 03: Pins 45 through 47, 50, 51, 53, 58, 60, and 61.

10/ Measured at the following pins:
Case X:
Device types 01 through 04: Pins 1 through 8 and 41 through 48.
Case Y and T:
Device types 01 through 03: Pins 2 through 17.
Case Z:
Device types 01 through 03: Pins 1 through 16.

11/ Measured at the following pins:
Case X:
Device types 01 through 04: Pins 33, 34, 36, 71, and 74.
Case Y and T:
Device types 01 through 03: Pins 51, 52, 55, 57, and 58.
Case Z:
Device types 01 through 03: Pins 48, 49, 52, 54, and 55.

12/ Measured at the following pins:
Case X:
Device types 01 through 04: Pins 9 through 11 and 49 through 51.
Case Y and T:
Device types 01 through 03: Pins 18 through 23.
Case Z:
Device types 01 through 03: Pins 17 through 22.

13/ Measured at the following pins:
Case X:
Device types 01 through 03: Pin 12.
Device type 04: Pins 12, 20, 40, 59, and 78.
Case Y and T:
Device types 01 through 03: Pin 24.
Case Z:
Device types 01 through 03: Pin 23.

TABLE I. Electrical performance characteristics - Continued.

14/ Measured at the following pins:
Case X:
Device types 01 through 04: Pins 32 and 69.
Case Y and T:
Device types 01 through 03: Pins 59 and 62.
Case Z:
Device types 01 through 03: Pins 56 and 59.

15/ Measured at the following pins:
Case X:
Device types 01 through 04: Pins 22 through 29 and 60 through 67.
Case Y and T:
Device types 01 through 03: Pins 65 through 80.
Case Z:
Device types 01 through 03: Pins 62 through 77.

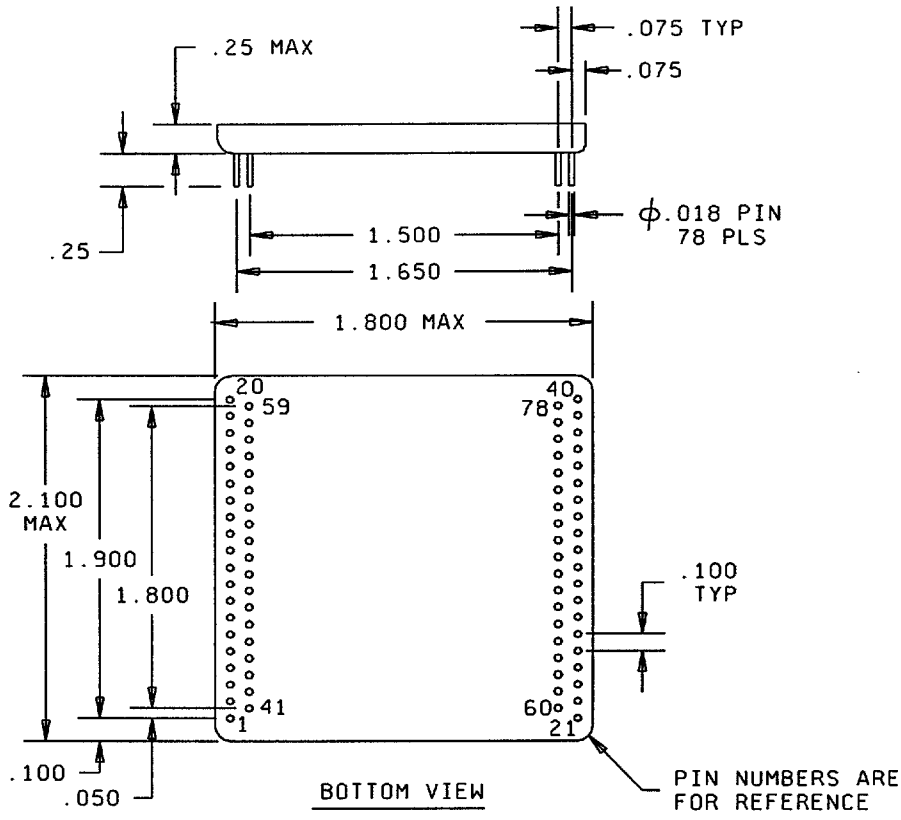
16/ Measured at the following pins:
Case X:
Device types 01 through 04: Pins 20, 40, 59, and 78.
Case Y and T:
Device types 01 through 03: Pins 39, 40, 43, and 44.
Case Z:
Device types 01 through 03: Pins 38 through 41.

17/ Parameter shall be tested as part of the initial characterization of this device and after design and process changes. Parameter shall be guaranteed to limits specified in table I for all lots not specifically tested.

18/ All timing parameters are measured at the 50 percent level of the waveform.

Device types 01 through 04.

Case outline X.



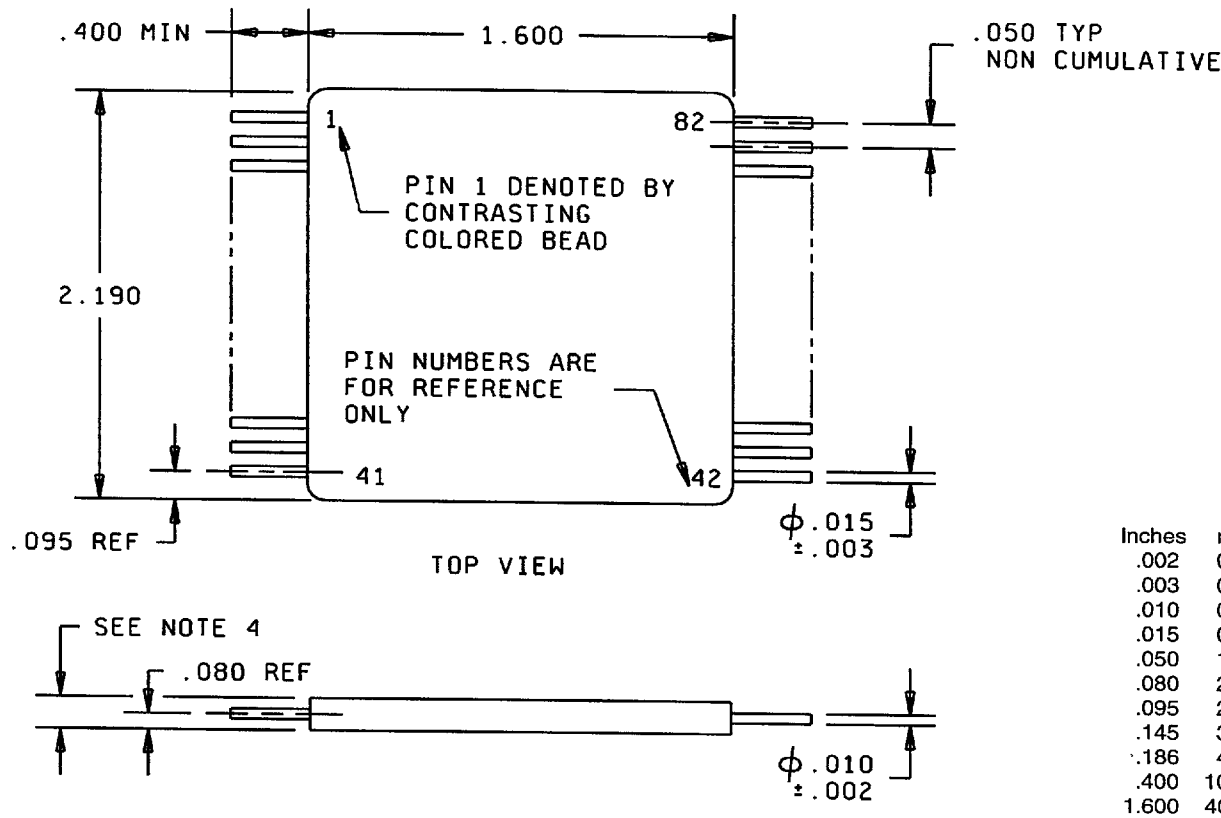
Inches	mm
.018	0.45
.050	1.27
.075	1.91
.100	2.54
.25	6.4
1.500	38.10
1.650	41.91
1.800	45.72
1.900	48.26
2.100	53.34

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Unless otherwise specified, tolerance is ±.005 (0.13 mm) for three place decimals and ±.01 (0.3 mm) for two place decimals.

FIGURE 1. Case outline(s).

Device types 01 through 03.

Case outlines Y and T.



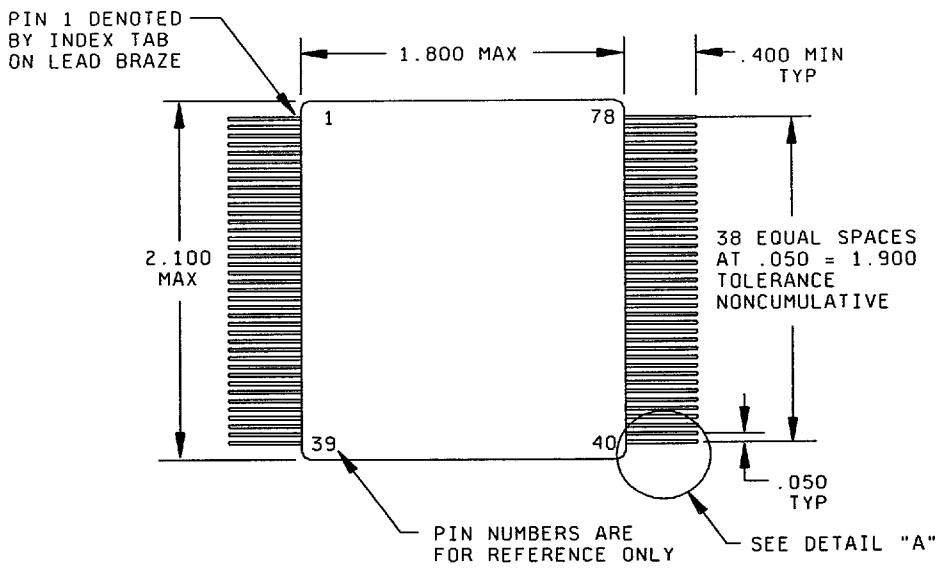
Inches	mm
.002	0.05
.003	0.08
.010	0.25
.015	0.38
.050	1.27
.080	2.03
.095	2.41
.145	3.68
.186	4.72
.400	10.16
1.600	40.64
2.190	55.63

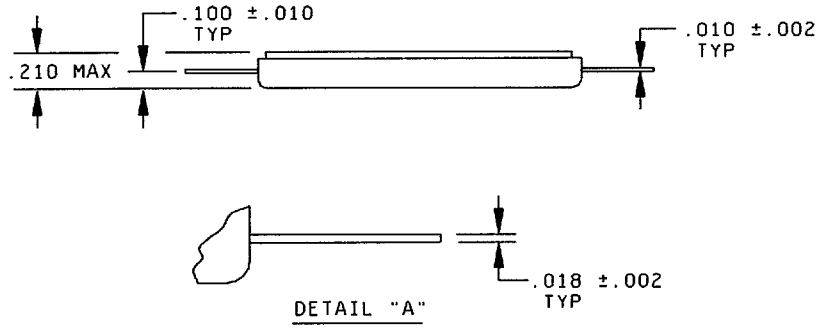
NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Unless otherwise specified, tolerance is ±.005 (0.13 mm) for three place decimals and ±.01 (0.3 mm) for two place decimals.
4. The case outline Y the package height is .186 inches (4.72 mm) maximum and the case outline T package height is .145 inches (3.68 mm) maximum.

FIGURE 1. Case outline(s) - Continued.

Device types 01 through 04.

Case outline Z.





Inches	mm
.002	0.05
.010	0.25
.018	0.46
.050	1.27
.100	2.54
.210	5.33
.400	10.16
1.800	45.72
1.900	48.26
2.100	53.34

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Unless otherwise specified, tolerance is ±.005 (0.13 mm) for three place decimals and ±.01 (0.3 mm) for two place decimals.

FIGURE 1. Case outline(s) - Continued.

Device types	01 through 03		Device types	01 through 03	
Case outlines	X	Y and T	Case outlines	X	Y and T
Terminal number	Terminal symbol		Terminal number	Terminal symbol	
1	D00	No connection	22	A01	RTAD4
2	D02	D00	23	A03	RTADP
3	D04	D01	24	A05	$\overline{\text{ILLCMD}}$
4	D06	D02	25	A07	SA/MC-2
5	D08	D03	26	A09	SA/MC-0
6	D10	D04	27	A11	SA/MC-4
7	D12	D05	28	A13	V_{DD}
8	D14	D06	29	A15	SA/MC-3
9	RTAD1	D07	30	MEMOE	SA/MC-1
10	RTAD0	D08	31	MEMENA-OUT	THIS-RT
11	RTAD4	D09	32	CLOCK IN	BCSTRCV
12	ILLCMD	D10	33	MEM/REG	RTPARRER
13	SA/MC-0	D11	34	STRBD	LMC
14	V_{DD}	D12	35	EXTEN	T/R
15	SA/MC-1	D13	36	RD/WR	V_{EE} (CH B) (SEE NOTE)
16	$\overline{\text{BCSTRCV}}$	D14	37	$\overline{\text{EXTLD}}$	V_{CC} (CH B)
17	LMC	D15	38	GNDA	GNDB
18	V_{EE} (CH B) (SEE NOTE)	RTAD1	39	V_{EE} (CH A) (SEE NOTE)	TX/RX-B
19	GNDB	RTAD3	40	TX/RX-A	TX/RX-B
20	TX/RX-B	RTAD0	41	D01	No connection
21	LOGIC GND	RTAD2	42	D03	No connection

NOTE: For device type 03, no connection.

FIGURE 2. Terminal connections.

Device types	01 through 03		Device types	01 through 03	
Case outlines	X	Y and T	Case outlines	X	Y and T
Terminal number	Terminal symbol		Terminal number	Terminal symbol	
43	DO5	TX/RX-A	63	A06	$\overline{\text{MEMOE}}$
44	DO7	$\overline{\text{TX/RX-A}}$	64	A08	$\overline{\text{MEMWR}}$
45	DO9	V_{EE} (CH A) (SEE NOTE)	65	A10	A15
46	D11	V_{CC} (CH A)	66	A12	A14
47	D13	GNDA	67	A14	A13
48	D15	$\overline{\text{TAGEN}}$	68	$\overline{\text{MEMWR}}$	A12
49	RTAD3	$\overline{\text{EXTLD}}$	69	$\overline{\text{MEMENA-IN}}$	A11
50	RTAD2	$\overline{\text{READYD}}$	70	$\overline{\text{INCMD}}$	A10
51	RTADP	RD/$\overline{\text{WR}}$	71	$\overline{\text{MSTRCLR}}$	A09
52	SA/MC-2	$\overline{\text{SELECT}}$	72	$\overline{\text{INT}}$	A08
53	SA/MC-4	$\overline{\text{EXTEN}}$	73	$\overline{\text{IOEN}}$	A07
54	SA/MC-3	$\overline{\text{IOEN}}$	74	$\overline{\text{SELECT}}$	A06
55	$\overline{\text{THIS-RT}}$	$\overline{\text{STRBD}}$	75	$\overline{\text{READYD}}$	A05
56	$\overline{\text{RTPARERR}}$	$\overline{\text{INT}}$	76	$\overline{\text{TAGEN}}$	A04
57	T/$\overline{\text{R}}$	MEM/$\overline{\text{REG}}$	77	V_{CC} (CH A)	A03
58	V_{CC} (CH B)	$\overline{\text{MSTRCLR}}$	78	$\overline{\text{TX/RX-A}}$	A02
59	$\overline{\text{TX/RX-B}}$	CLOCK IN	79	------	A01
60	AO0	$\overline{\text{INCMD}}$	80	------	A00
61	AO2	$\overline{\text{MEMENA-OUT}}$	81	------	LOGIC GND
62	AO4	$\overline{\text{MEMENA-IN}}$	82	------	No connection

NOTE: For ddevice type 03, no connection.

FIGURE 2. Terminal connections - Continued.

Device type	04				
Case outline	X				
Terminal number	Termibal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	D00	27	A11	53	SA/MC-4
2	D02	28	A13	54	SA/MC-3
3	D04	29	A15	55	$\overline{\text{THIS-RT}}$
4	D06	30	MEMOE	56	RTPARERR
5	D08	31	$\overline{\text{MEMENA-OUT}}$	57	$\overline{\text{T/R}}$
6	D10	32	CLOCK IN	58	TXINH-B
7	D12	33	MEM/$\overline{\text{REG}}$	59	RX-B
8	D14	34	$\overline{\text{STRBD}}$	60	A00
9	RTAD1	35	$\overline{\text{EXTEN}}$	61	A02
10	RTAD0	36	RD/$\overline{\text{WR}}$	62	A04
11	RTAD4	37	$\overline{\text{EXTLD}}$	63	A06
12	$\overline{\text{ILLCMD}}$	38	TX-A	64	A08
13	SA/MC-0	39	$\overline{\text{TX-A}}$	65	A10
14	V_{DD}	40	$\overline{\text{RX-A}}$	66	A12
15	SA/MC-1	41	D01	67	A14
16	$\overline{\text{BSCTRCV}}$	42	D03	68	$\overline{\text{MEMWR}}$
17	LMC	43	D05	69	$\overline{\text{MEMENA-IN}}$
18	TX-B	44	D07	70	$\overline{\text{INCMD}}$
19	$\overline{\text{TX-B}}$	45	D09	71	$\overline{\text{MSTRCLR}}$
20	$\overline{\text{RX-B}}$	46	D11	72	$\overline{\text{INT}}$
21	LOGIC GND	47	D13	73	$\overline{\text{IOEN}}$
22	A01	48	D15	74	$\overline{\text{SELECT}}$
23	A03	49	RTAD3	75	$\overline{\text{READYD}}$
24	A05	50	RTAD2	76	TAGEN
25	A07	51	RTADP	77	TXINH-A
26	A09	52	SA/MC-2	78	RX-A

FIGURE 2. Terminal connections - Continued.

Device type	01, 02, and 03				
Case outline	Z				
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	D00	27	V_{DD}	53	$\overline{INT}$
2	D01	28	SA/MC-3	54	MEM/$\overline{REG}$
3	D02	29	SA/MC-1	55	$\overline{MSTRCLR}$
4	D03	30	$\overline{THIS-RT}$	56	CLOCK-IN
5	D04	31	$\overline{BCSTRCV}$	57	$\overline{INCMD}$
6	D05	32	$\overline{RTPARERR}$	58	$\overline{MEMENA-OUT}$
7	D06	33	LMC	59	$\overline{MEMENA-IN}$
8	D07	34	T/$\overline{R}$	60	$\overline{MEMOE}$
9	D08	35	V_{EE} (CH B)	61	$\overline{MEMWR}$
10	D09	36	V_{CC} (CH B)	62	A15
11	D10	37	GNDB	63	A14
12	D11	38	$\overline{TX/RX-B}$	64	A13
13	D12	39	TX/RX-B	65	A12
14	D13	40	TX/RX-A	66	A11
15	D14	41	$\overline{TX/RX-A}$	67	A10
16	D15	42	V_{EE} (CH A)	68	A09
17	RTAD1	43	V_{CC} (CH A)	69	A08
18	RTAD3	44	GNDA	70	A07
19	RTAD0	45	$\overline{TAGEN}$	71	A06
20	RTAD2	46	$\overline{EXTLD}$	72	A05
21	RTAD4	47	$\overline{READYD}$	73	A04
22	RTADP	48	RD/$\overline{WR}$	74	A03
23	$\overline{ILLCMD}$	49	$\overline{SELECT}$	75	A02
24	SA/MC-2	50	$\overline{EXTEN}$	76	A01
25	SA/MC-0	51	$\overline{IOEN}$	77	A00
26	SA/MC-4	52	$\overline{STRBD}$	78	GND

FIGURE 2. Terminal connections - Continued.

Device types 01 through 03.

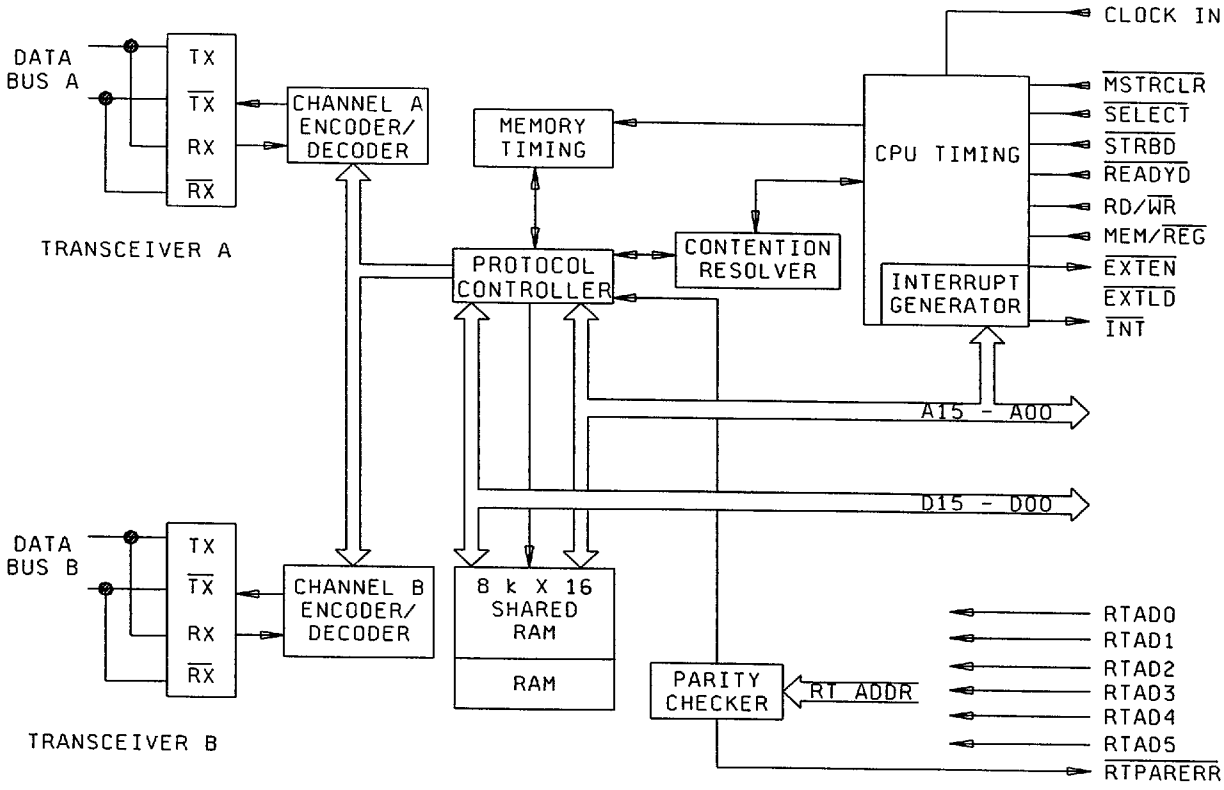


FIGURE 3. Block diagrams.

Device type 04.

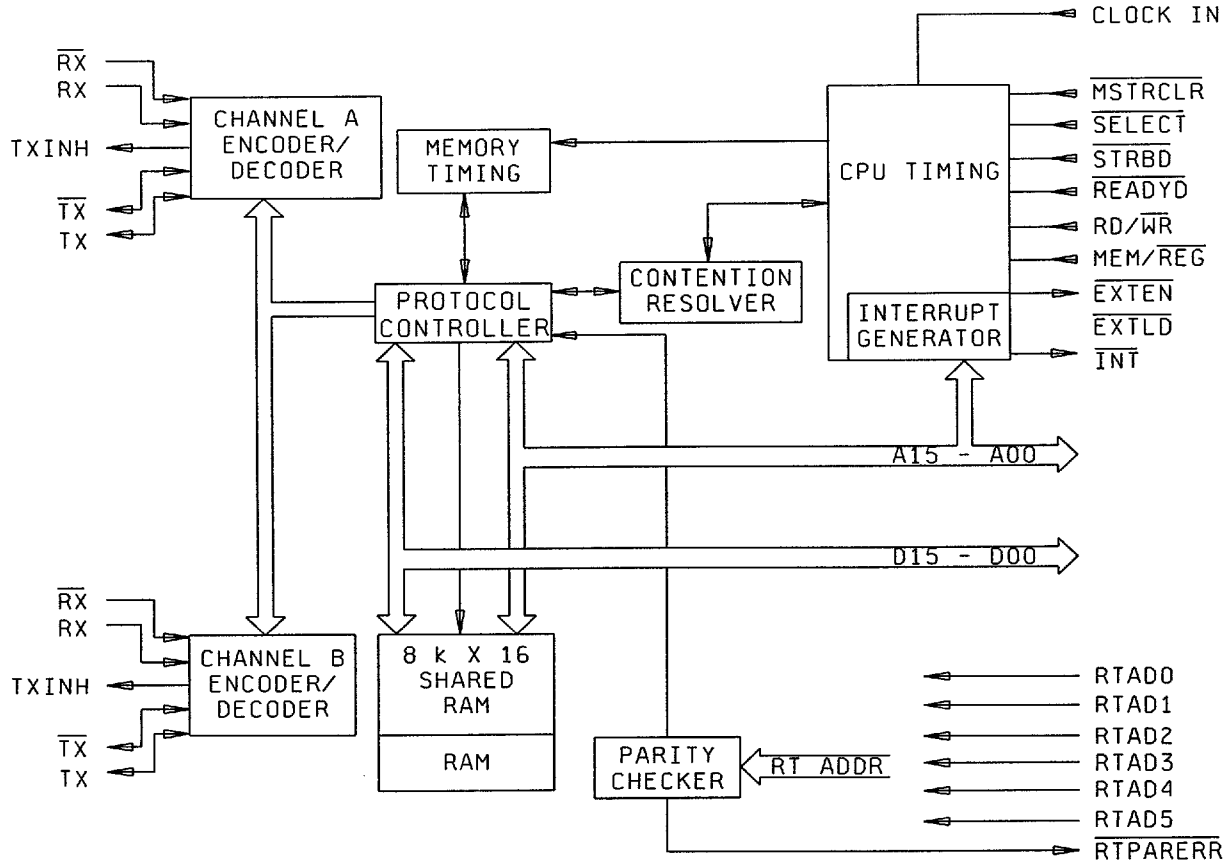
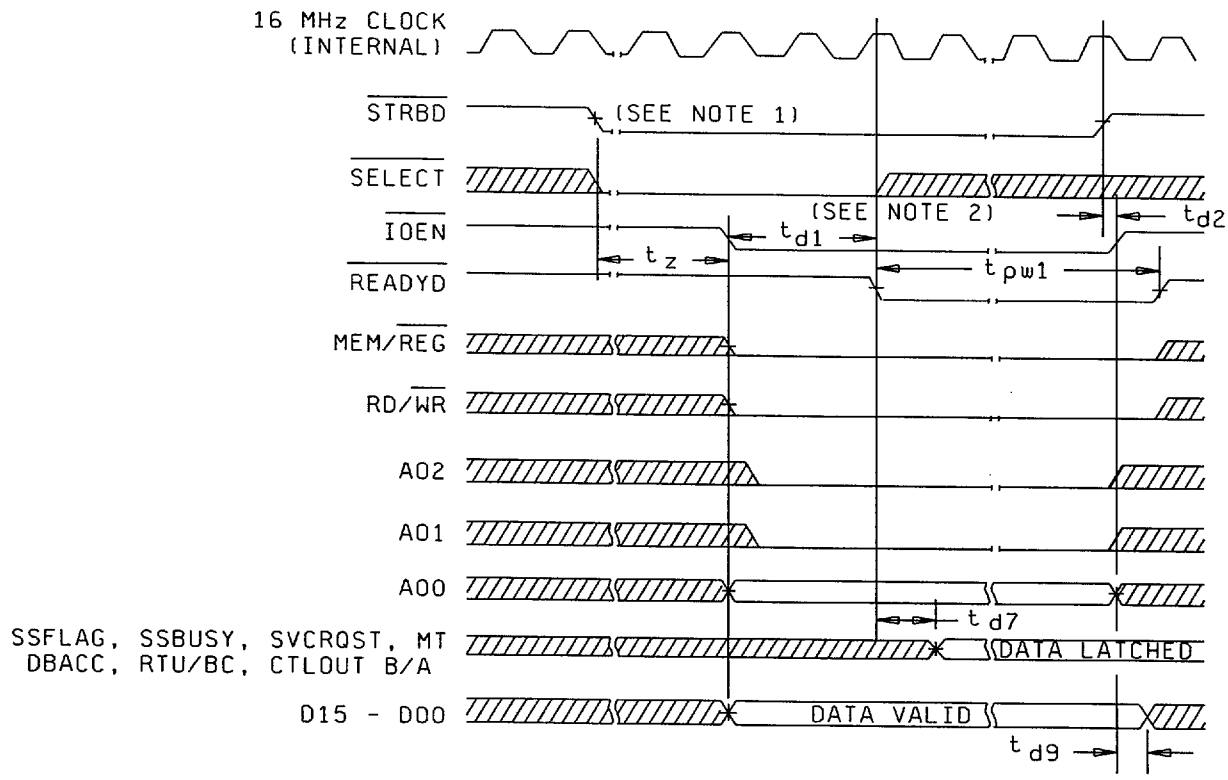


FIGURE 3. Block diagrams - Continued.

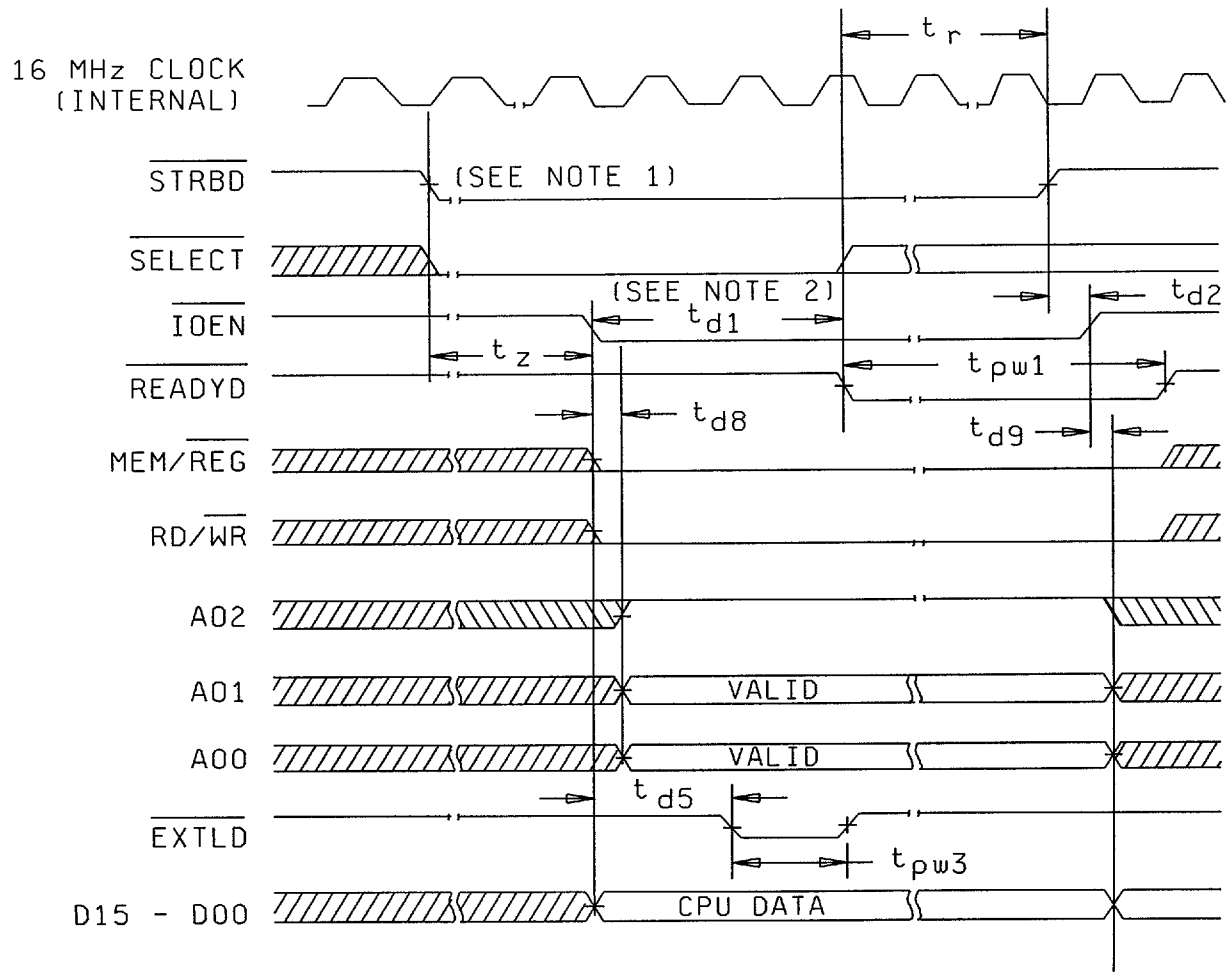
CPU writes to internal register.



NOTES:
1. STRBD to IOEN (low) delay is two clock cycles. If contention occurs, delay is two clock cycles following release of bus (1.8 µs maximum).
2. CPU must release STRBD within 1.5 µs of IOEN going active.

FIGURE 4. Timing diagram(s).

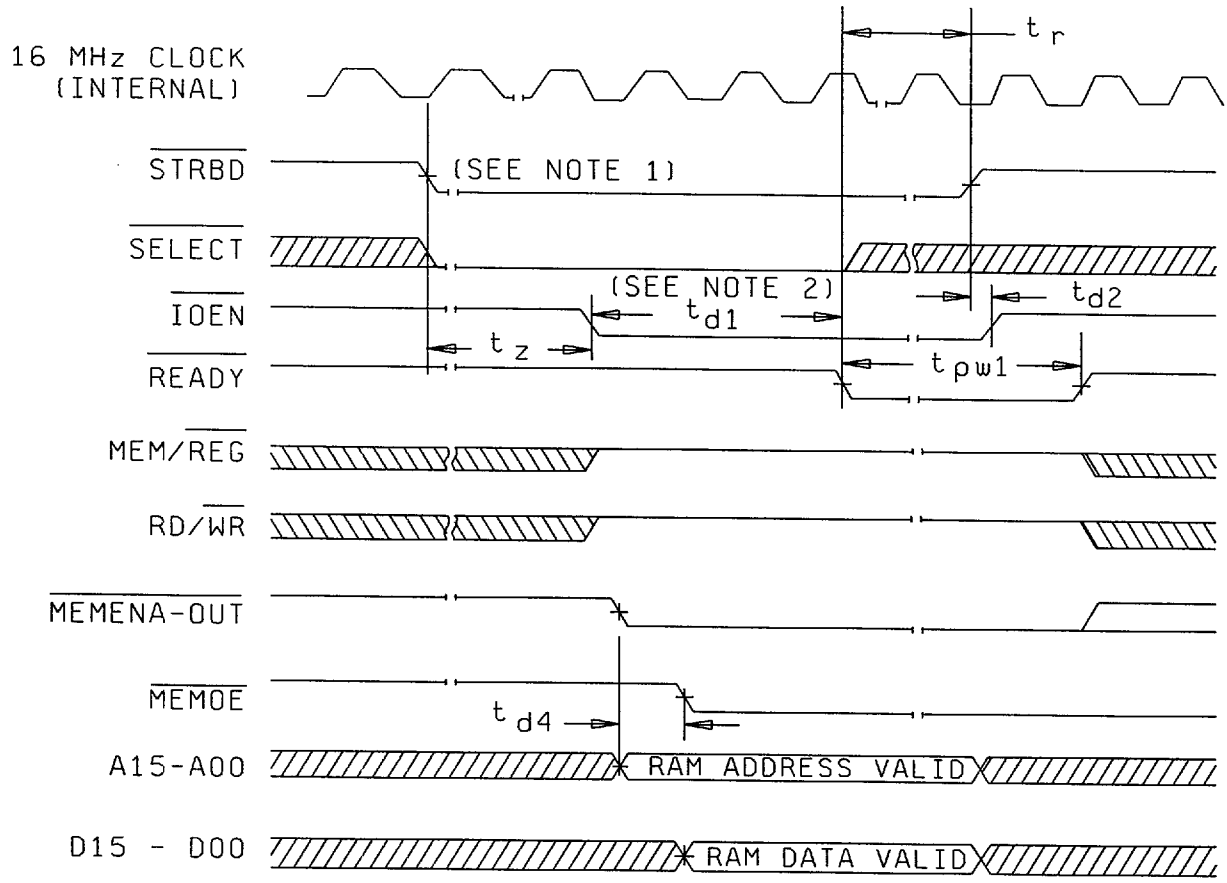
CPU writes to external register.



NOTES:
1. STRBD to IOEN (low) delay is two clock cycles. If contention occurs, delay is two clock cycles following release of bus (1.8 µs maximum).
2. CPU must release STRBD within 1.5 µs of IOEN going active.

FIGURE 4. Timing diagram(s) - Continued.

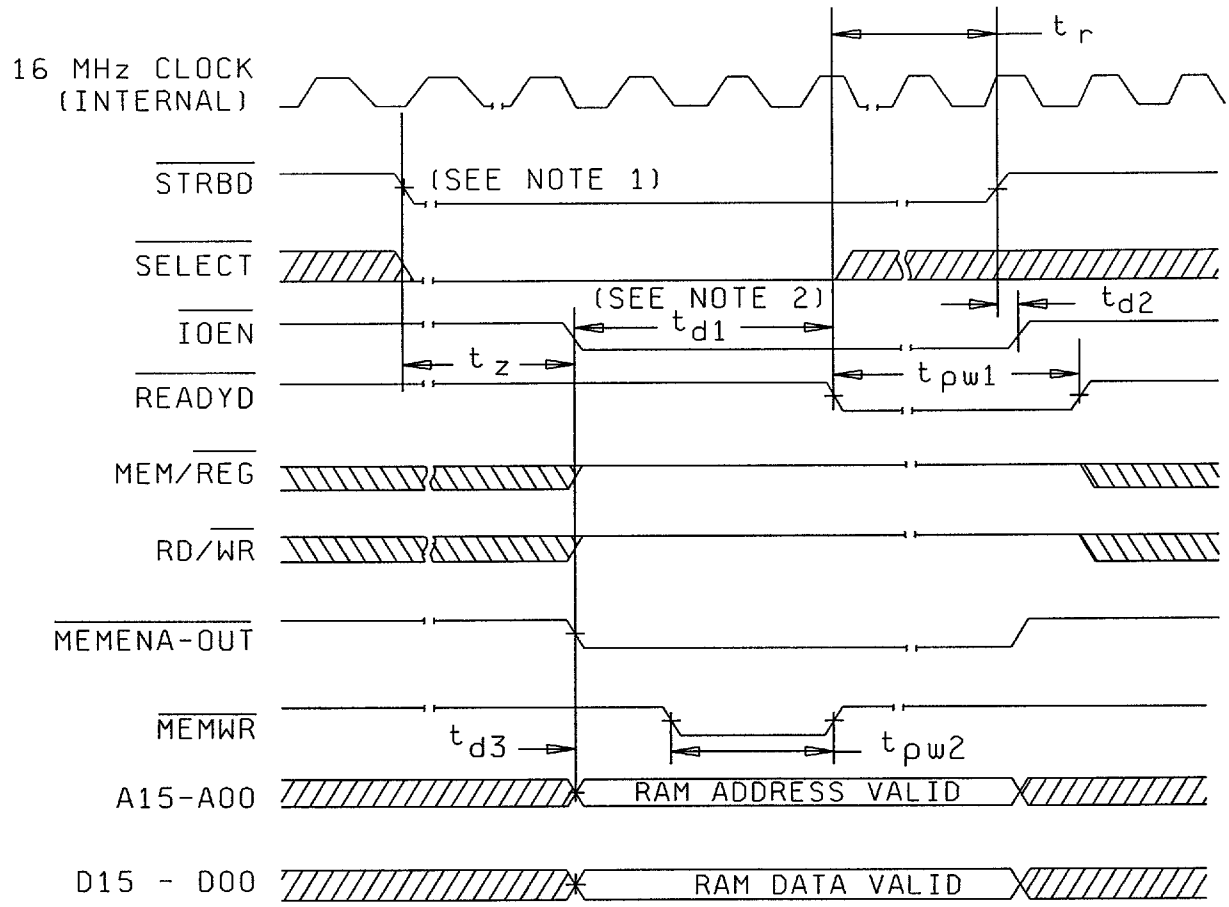
CPU reads from RAM.



NOTES:
1. STRBD to IOEN (low) delay is two clock cycles. If contention occurs, delay is two clock cycles following release of bus (1.8 µs maximum).
2. CPU must release STRBD within 1.5 µs of IOEN going active.

FIGURE 4. Timing diagram(s) - Continued.

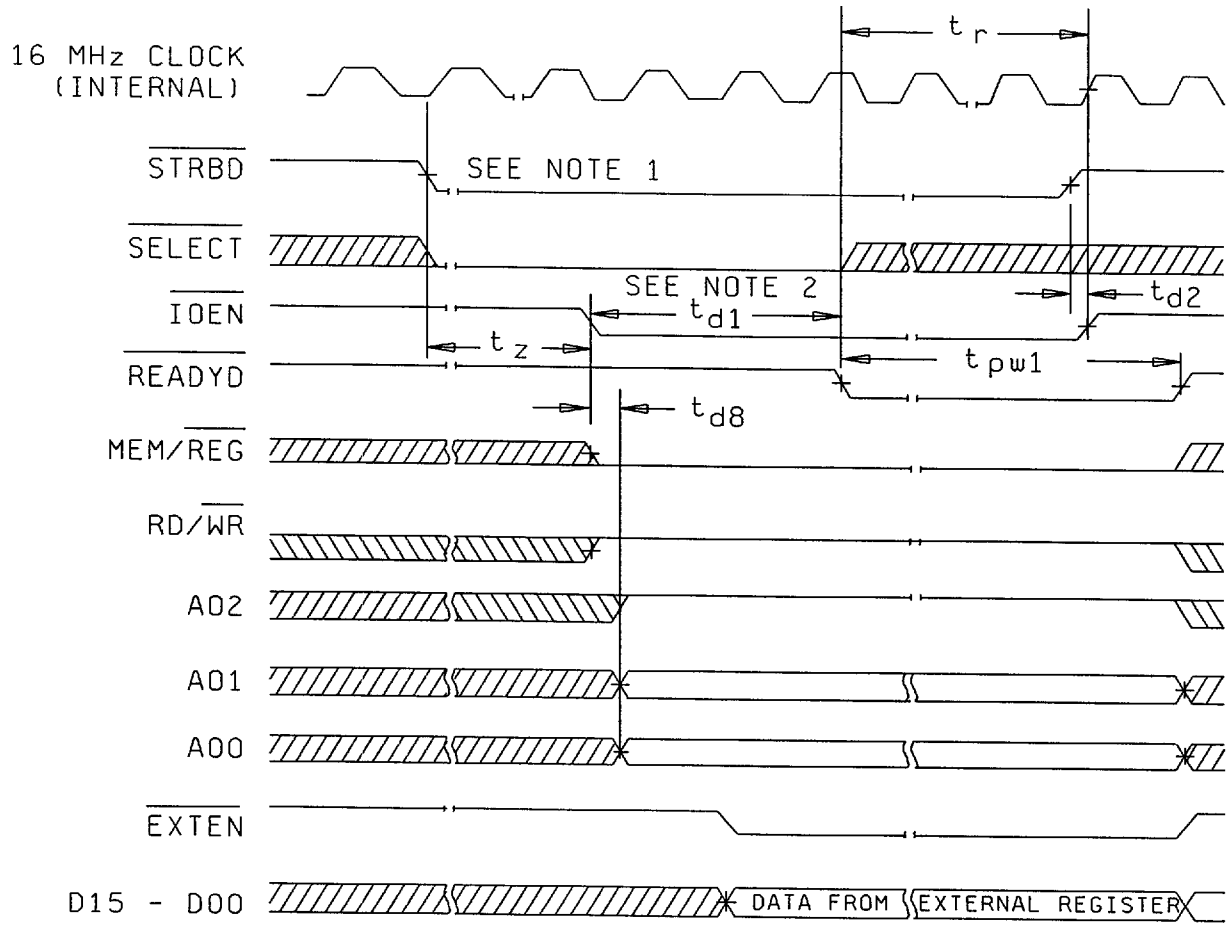
CPU writes to RAM.



NOTES:
1. STRBD to IOEN (low) delay is two clock cycles. If contention occurs, delay is two clock cycles following release of bus (1.8 µs maximum).
2. CPU must release STRBD within 1.5 µs of IOEN going active.

FIGURE 4. Timing diagram(s) - Continued.

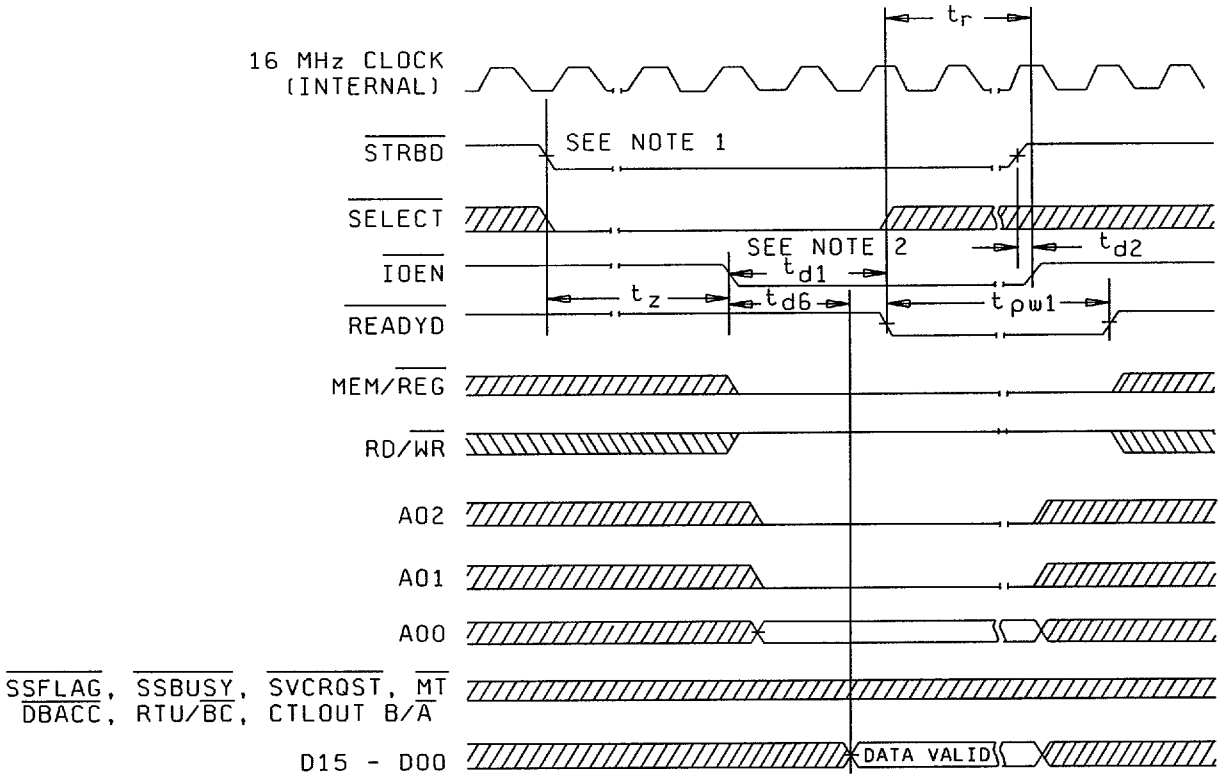
CPU reads from external register.



NOTE:
1/ STRBD to IOEN (low) delay is two clock cycles. If contention occurs, delay is two clock cycles following release of bus.

FIGURE 4. Timing diagram(s) - Continued.

CPU read from internal register.



NOTES:
1. STRBD to IOEN (low) delay is two clock cycles. If contention occurs, delay is two clock cycles following release of bus (1.8 µs maximum).
2. CPU must release STRBD within 1.5 µs of IOEN going active.

FIGURE 4. Timing diagram(s) - Continued.

TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534, group A test table)
Interim electrical parameters	1,2,3,4,5,6,7,8,9,10,11
Final electrical parameters	1*,2,3,4,5,6,7,8,9,10,11
Group A test requirements	1,2,3,4,5,6,7,8,9,10,11
Group C end-point electrical parameters	1,2,3,4,5,6,7,8,9,10,11
MIL-STD-883, group E end-point electrical parameters for RHA devices	Subgroups** (in accordance with method 5005, group A test table)

* PDA applies to subgroup 1.
** When applicable to this standard microcircuit drawing, the subgroups shall be defined.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38534. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Conformance and periodic inspections. Conformance inspection (CI) and periodic inspection (PI) shall be in accordance with MIL-PRF-38534 and as specified herein.

4.3.1 Group A inspection (CI). Group A inspection shall be in accordance with MIL-PRF-38534. Tests shall be as specified in table II herein.

4.3.2 Group B inspection (PI). Group B inspection shall be in accordance with MIL-PRF-38534.

4.3.3 Group C inspection (PI). Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1005 of MIL-STD-883.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.3.4 Group D inspection (PI). Group D inspection shall be in accordance with MIL-PRF-38534.

4.3.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels shall be M, D, R, and H. RHA quality conformance inspection sample tests shall be performed at the RHA level specified in the acquisition document.

a. RHA tests for levels M, D, R, and H shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

b. End-point electrical parameters shall be as specified in table II herein.

c. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table II herein.

d. The devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38534 for RHA level being tested, and meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5 percent, after exposure.

e. Prior to and during total dose irradiation testing, the devices shall be biased to establish a worst case condition as specified in the radiation exposure circuit.

f. For device classes H and K, subgroups 1 and 2 in table V, method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.

g. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-7603.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0512.

6.6 Sources of supply. Sources of supply are listed in QML-38534. The vendors listed in QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DSCC-VA and have agreed to this drawing.

TABLE III. Pin functions.

Terminal symbol	I/O	Description
D00	I/O	Data bus bit 0 (LSB).
D02	I/O	Data bus bit 2.
D04	I/O	Data bus bit 4.
D06	I/O	Data bus bit 6.
D08	I/O	Data bus bit 8.
D10	I/O	Data bus bit 10.
D12	I/O	Data bus bit 12.
D14	I/O	Data bus bit 14.
RTAD1	I	Remote terminal address bit 1.
RTAD0	I	Remote terminal address bit 0 (LSB).
RTAD4	I	Remote terminal address bit 4 (MSB).
$\overline{\text{ILLCMD}}$	I	Illegal command. Defines the received command as illegal.
SA/MC-0	O	Subaddress/mode command bit 0. Multiplexed output bit-0 of subaddress/word count field of the current command word. SA/MC determined by the state of LMC.
V_{DD}	I	+5 V supply input for digital logic section.
SA/MC-1	O	Subaddress/mode command bit 1. In MT mode, pulses every time 32 words have been stored.
$\overline{\text{BCSTRCV}}$	O	Broadcast received. Indicates current command is a 1553 broadcast command.
LMC	O	Latched mode command. Logic 1 indicates current command word is a mode code and selects MC0-MC4. Logic 0 indicates nonmode command and selects SA0-SA4.
V_{EE} (CH B)	I	Input power supply connection for the B channel transceiver. -15 V for device type 01, -12 V for device type 02. For device type 03 no connection (NC).
GNDB	-	Ground B. Power supply return connection for the B channel transceiver.
TX/RX-B	I/O	Transmit/receive transceiver-B. Input/output to the coupling transformer that connects to the B channel of the 1553 bus.
LOGIC GND	-	Logic ground. Power supply return for the digital logic section.

TABLE III. Pin functions - Continued.

Terminal symbol	I/O	Description
A01	I/O	Address bus bit 1.
A03	I/O	Address bus bit 3.
A05	I/O	Address bus bit 5.
A07	I/O	Address bus bit 7.
A09	I/O	Address bus bit 9.
A11	I/O	Address bus bit 11.
A13	I/O	Address bus bit 13.
A15	I/O	Address bus bit 15.
$\overline{\text{MEMOE}}$	O	Memory output enable. Output to enable RAM output data.
$\overline{\text{MEMENA-OUT}}$	O	Memory enable out. Logic 0 output enables external RAM. Used with $\overline{\text{MEMOE}}$ to read data or with MEMWR to write data into external RAM.
CLOCK-IN	I	Clock input. 16 MHz TTL clock.
MEM/$\overline{\text{REG}}$	I	Memory/register. Input from CPU to select memory or register data transfer.
$\overline{\text{STRBD}}$	I	Strobe data. Used in conjunction with $\overline{\text{SELECT}}$ to initiate a data transfer cycle to/from CPU.
$\overline{\text{EXTEN}}$	O	External enable. Used to load data into external devices.
D11	I/O	Data bus bit 11.
D13	I/O	Data bus bit 13.
D15	I/O	Data bus bit 15.
RTAD3	I	Remote terminal address bit 3.
RTAD2	I	Remote terminal address bit 2.
RTADP	I	Remote terminal address parity input.
SA/MC-2	O	Subaddress/mode command bit 2.
SA/MC-4	O	Subaddress/mode command bit 4.
SA/MC-3	O	Subaddress/mode command bit 3.

TABLE III. Pin functions - Continued.

Terminal symbol	I/O	Description
$\overline{\text{THIS-RT}}$	O	Logic 0 pulse indicates receipt of a valid command word which contains the remote terminal address equivalent to the RTAD0-RTAD4 inputs.
$\overline{\text{RTPARERR}}$	O	RTU (address) parity error. Logic 0 indicates RTU address parity (odd parity: RTAD0-RTAD4, RTADP) has been violated.
$\overline{\text{T/R}}$	O	Transmit/receive 1553 data. Latched T/R bit from current command word.
RD/$\overline{\text{WR}}$	I	Read/write. Input from the CPU which defines the data bus transfer as a read or write operation.
$\overline{\text{EXTLD}}$	O	External load. Used to load data into external devices.
GNDA	-	Ground A. Power supply return connection for the A channel transceiver.
V_{EE} (CH A)	I	Input power supply connection for the A channel transceiver. -15 V for device type 01, -12 V for device type 02. For device type 03 no connection (NC).
$\overline{\text{TX/RX-A}}$	I/O	Transmit receive transceiver-a. Input/output to the coupling transformer that connects to the A channel of the 1553 bus.
D01	I/O	I/O data bus bit 1.
D03	I/O	Data bus bit 3.
D05	I/O	Data bus bit 5.
D07	I/O	Data bus bit 7.
D09	I/O	Data bus bit 9.
V_{CC} (CH B)	I	+5 V power supply connection for the B channel transceiver.
TX/RX-B	I/O	Transmit/receive transceiver-B. Inverted I/O to coupling transformer that connects to channel B of the 1553 bus.
A00	I/O	Address bit 0 (LSB).
A02	I/O	Address bit 2.
A04	I/O	Address bit 4.
A06	I/O	Address bit 6.
A08	I/O	Address bit 8.
A10	I/O	Address bit 10.
A12	I/O	Address bit 12.
A14	I/O	Address bit 14.

TABLE III. Pin functions - Continued.

Terminal symbol	I/O	Description
$\overline{\text{MEMWR}}$	O	Memory write. Output pulse to write data into memory.
$\overline{\text{MEMENA-IN}}$	I	Memory enable in. Enables internal RAM only; connect directly to $\overline{\text{MEMENA-OUT}}$.
$\overline{\text{INCMD}}$	O	In command. Indicates BC to RTU currently in message transfer sequence.
$\overline{\text{MSTRCLR}}$	I	Master clear. Power-on reset from CPU.
$\overline{\text{INT}}$	O	Interrupt. Interrupt pulse line to CPU.
$\overline{\text{IOEN}}$	O	Input/output enable. Output to enable external buffers/latches connecting the hybrid to the address/data bus.
$\overline{\text{SELECT}}$	I	Select. Input from the CPU. When active selects device for operation.
$\overline{\text{READYD}}$	O	Ready data. When active indicates data has been received from, or is available to, the CPU.
$\overline{\text{TAGEN}}$	O	Tag enable. Enables an external time to counter for transferring the time tag word into memory.
V_{CC} (CH A)	I	+5 V input power supply connection for the channel A transceiver.
$\overline{\text{TX/RX-A}}$	I/O	Transmit/receive transceiver-A. Inverted I/O to the coupling transformer that connect to channel A of the 1553 bus.
TX-B	O	Channel B transmit data, output signal connection to the 1553 bus transceiver (channel B) for data to be transmitted.
$\overline{\text{TX-B}}$	O	Channel B transmit $\overline{\text{data}}$, output signal connection to the 1553 bus transceiver (channel B) for data to be transmitted.
TXINH-B	O	Channel B transmitter inhibit, normally high level output signal which goes low to enable a transmission on channel B.
RX-B	I	Channel B received data, input signal connection from 1553 bus transceiver (channel B) for the data being received.
$\overline{\text{RX-B}}$	I	Channel B received $\overline{\text{data}}$, input signal connection from 1553 bus transceiver (channel B) for the data being received.
TX-A	O	Same as TX-B, except for channel A.
$\overline{\text{TX-A}}$	O	Same as $\overline{\text{TX}}$-B, except for channel A.
TXINH-A	O	Same as TXINH-B, except for channel A.
RX-A	I	Same as RX-B, except for channel A.
$\overline{\text{RX-A}}$	I	Same as $\overline{\text{RX}}$-B, except for channel A.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 97-03-04

Approved sources of supply for SMD 5962-88692 are listed below for immediate acquisition only and shall be added to QML-38534 during the next revision. QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of QML-38534.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8869201XA	S7631	BUS61553II-140
5962-8869201XC	S7631	BUS61553II-110
5962-8869201TA	19645	BUS61563IV-140
5962-8869201TC	19645	BUS61563IV-110
5962-8869201XA	19645	BUS61553II-140
5962-8869201XC	19645	BUS61553II-110
5962-8869201YA	3/	BUS61563II-140
5962-8869201YC	3/	BUS61563II-110
5962-8869201ZA	3/	BUS61563II-618
5962-8869201ZC	3/	BUS61563II-617
5962-8869202XA	S7631	BUS61554II-140
5962-8869202XC	S7631	BUS61554II-110
5962-8869202TA	19645	BUS61564IV-140
5962-8869202TC	19645	BUS61564IV-110
5962-8869202XA	19645	BUS61554II-140
5962-8869202XC	19645	BUS61554II-110
5962-8869202YA	3/	BUS61564II-140
5962-8869202YC	3/	BUS61564II-110
5962-8869202ZA	3/	BUS61564II-602
5962-8869202ZC	3/	BUS61564II-601
5962-8869203XA	19645	BUS61555II-140
5962-8869203XC	19645	BUS61555II-110
5962-8869203YA	19645	BUS61565II-140
5962-8869203YC	19645	BUS61565II-110
5962-8869203ZA	19645	BUS61565II-603
5962-8869203ZC	19645	BUS61565II-604
5962-8869204XA	19645	BUS61556II-140
5962-8869204XC	19645	BUS61556II-110

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. The device manufacturers listed herein are authorized to supply alternate lead finishes "A", "B", or "C" at their discretion. Contact the listed approved source of supply for further information.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ These SMD device types are not available from a QML supplier. Case outline T can be used as a replacement for case outline Y.

Vendor CAGE number	Vendor name and address
S7631	DDC Ireland LTD. Cork Business and Technology Park Model Farm Road Cork, Ireland
19645	ILC Data Device Corporation 105 Wilbur Place Bohemia, NY 11716-2482