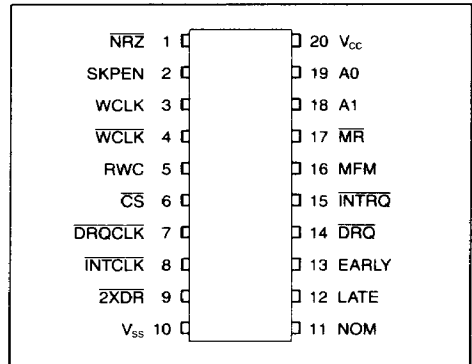


Hard Disk Improved MFM Generator

FEATURES

- Single +5 Volt Power Supply
- Write Precompensation
- Address Mark Generation
- 5 Mbit Data Rate
- Converts NRZ to MFM
- 20 Pin DIP
- n-Channel COPLAMOS® Silicon Gate Technology

PIN CONFIGURATION



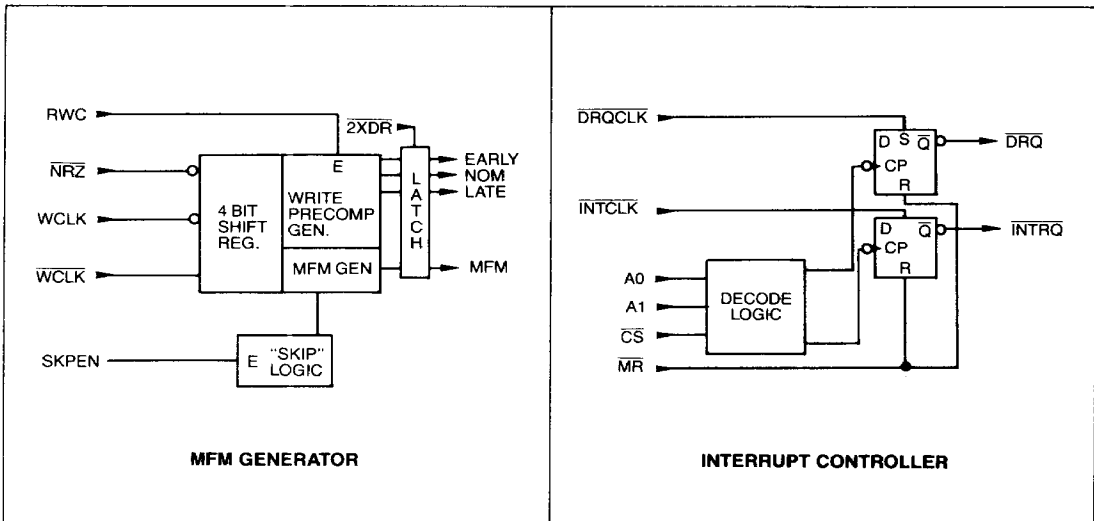
GENERAL DESCRIPTION

The HDC 1100-12 "improved" MFM Generator converts serial NRZ data into an MFM (Modified Frequency Modulated) data stream. The MFM signal may be used to record information on a Winchester Disk.

In addition, the HDC 1100-12 generates Write Precompensation signals required to compensate for bit shift effects on the recording medium.

The HDC 1100-12 has the ability to delete clock pulses in the outgoing data stream in order to record Address Marks.

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DESCRIPTION OF PIN FUNCTIONS

| PIN NUMBER | SYMBOL | NAME | FUNCTION |
|------------|---------------------------------|-------------------------|---|
| 1 | NRZ | NON-RETURN-TO ZERO | NRZ data input that is strobed into the MFM generator by WCLK (1). |
| 2 | SKPEN | SKIP ENABLE | This input arms the SKIP logic for recording Address Marks when set to a logic 1. |
| 3 | WCLK | WRITE CLOCK | Complimentary clock inputs. NRZ data is clocked into the MFM Generator on the high-to-low transition of WCLK (pin 3). |
| 4 | WCLK | WRITE CLOCK | |
| 5 | RWC | REDUCED WRITE CURRENT | This signal when high, enables EARLY, LATE and NOM outputs. |
| 9 | 2 x DR | 2 TIMES DATA RATE | This input is used to latch EARLY, LATE, NOM and MFM outputs. |
| 10 | V _{SS} | V _{SS} | Ground. |
| 11 | NOM | NOMINAL | Output signal from the Write Precompensation Logic used to signify that data is to be written nominal. |
| 12 | LATE | LATE | Output signal from the Write Precompensation Logic used to signify that data is to be shifted LATE before writing. |
| 13 | EARLY | EARLY | Output signal from the Write Precompensation Logic used to signify that data is to be shifted EARLY before writing. |
| 16 | MFM | MFM DATA | This output contains the MFM encoded data derived from the NRZ (pin 1) line. |
| 6 | CS | CHIP SELECT | Low input signal used to enable the Address decode logic. |
| 8 | INTCLK | INTERRUPT REQUEST CLOCK | A high-to-low transition on this line will latch the INTRQ (pin 15) at a logic 0. |
| 7 | DRQCLK | DATA REQUEST CLOCK | A high-to-low transition on this line will latch the DRQ (pin 14) at a logic 0. |
| 15 | INTRQ | INTERRUPT REQUEST | This output is latched at a logic 0 when INTCLK (pin 8) makes a high-to-low transition while the decode logic is disabled. |
| 14 | DRQ | DATA REQUEST | This output is latched at a logic 0 when DRQCLK (pin 7) makes a high-to-low transition while the decode logic is disabled. |
| 17 | MR | MASTER RESET | A low level on this line causes DRQ and INTRQ to set at a logic 1. |
| 18, 19 | A ₀ , A ₁ | ADDRESS 1, 0 | When CS is low and the address lines are high, INTRQ is cleared; if the address lines are low then DRQ gets cleared. (i.e. set at a logic 1). |
| 20 | V _{CC} | V _{CC} | + 5V power supply input. |

OPERATION

The HDC 1100-12 is divided into two sections: MFM Generator and Interrupt Logic. The MFM Generator converts NRZ data into MFM data and provides Write Precompensation signals. The Interrupt Logic may be used to generate Interrupt signals. The two sections of the device are isolated and have no common input or output signals.

Prior to entering data, the SKPEN line must be set to a logic 0 to enable only clocks in the data stream. Data is entered on the NRZ line and strobed on the high-to-low transition of WCLK. The encoded NRZ data appears on the MFM (pin 16) output lagging by one clock cycle.

Write Precompensation signals EARLY, LATE, and NOM are generated as each data or clock pulse becomes available at the input when RWC is logic 1.

The SKPEN signal is used to record a unique data/clock pattern as an Address Mark, using A1 data with 0A clock. This pattern is used for synchronization prior to data or ID fields that are read from the disk.

When the SKPEN signal is set to a logic 1, the internal skip

logic is enabled. As long as zeroes are being shifted into the NRZ line, the device generates normal MFM data. On receipt of the first non-zero bit (typically the MSB of the A1 16) the skip logic begins to count WCLK cycles. When the MFM generator tries to produce a clock between data bits 2 and 3, the skip logic disables the MFM generator during that time. The result for A1₁₆ data is a clock pattern of 0A₁₆ instead of 0E₁₆. Although other data patterns may be used,

| MR | A ₁ | A ₀ | CS | DRQ | INTRQ |
|----|----------------|----------------|----|----------------|----------------|
| 0 | X | X | X | H | H |
| 1 | X | X | 1 | Q _N | Q _N |
| 1 | 0 | 0 | 0 | H | Q _N |
| 1 | 1 | 1 | 0 | Q _N | H |
| 1 | 1 | 0 | 0 | Q _N | Q _N |
| 1 | 0 | 1 | 0 | Q _N | Q _N |

X = Don't care

Q_N = remains at previous state

INTERRUPT REQUEST LOGIC TABLE

the MSB of the pattern must be a 1 (80₁₆ or higher) in order to enable the skip logic at the proper time. After the skip logic has performed, it then disables itself and MFM data is recorded normally starting with the succeeding byte. To re-enable the skip logic again, the SKPEN line must be strobed.

The Interrupt Logic is used to clear Data Requests ($\overline{\text{DRQ}}$)

and Interrupt Requests ($\overline{\text{INTRQ}}$) by selecting $\overline{\text{CS}}$ (pin 6) in combination with A0 and A1. The $\overline{\text{MR}}$ (Master Reset) signal is used to clear both $\overline{\text{DRQ}}$ and $\overline{\text{INTRQ}}$ simultaneously. $\overline{\text{DRQ}}$ and $\overline{\text{INTRQ}}$ can be set to a logic 0 only by a low level or $\overline{\text{DRQCLK}}$ and $\overline{\text{INTCLK}}$ respectively. The signal will remain at a logic 0 until cleared by a $\overline{\text{MR}}$ or proper address selection via $\overline{\text{CS}}$, A1 and A0.

| LAST DATA SENT | SENDING | TO BE SENT NEXT | EARLY | LATE | NOM |
|-------------------|---------|-----------------|-------|------|-----|
| X | 1 | 0 | H | L | L |
| X | 0 | 1 | L | H | L |
| 0 | 0 | 0 | H | L | L |
| 1 | 0 | 0 | L | H | L |
| ANY OTHER PATTERN | | | L | L | H |

WRITE PRECOMPENSATION LOGIC TABLE

MAXIMUM GUARANTEED RATINGS*

| | |
|---|----------------------|
| Operating Temperature Range | 0°C to +50°C |
| Storage Temperature Range | -55° to +150°C |
| Lead Temperature (soldering, 10 sec.) | +300°C |
| Positive Voltage on any I/O Pin, with respect to ground | +7.0V |
| Negative Voltage on any I/O Pin, with respect to ground | -0.2V |
| Power Dissipation | 1.0 watt |

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and the device at these or at any other condition above those indicated in the operational sections of this specification is

DC ELECTRICAL CHARACTERISTICS: $T_A = 0^\circ\text{C to } 50^\circ\text{C}; V_{CC} = +5V \pm 10\%; V_{SS} = 0V$

| SYMBOL | PARAMETER | MIN | TYP ¹ | MAX | UNIT | CONDITION |
|----------|---------------------|------|------------------|-----|------|-----------------------------|
| V_{IL} | Input Low Voltage | -0.2 | | 0.8 | V | |
| V_{IH} | Input High Voltage | 2.4 | | | V | |
| V_{OL} | Output Low Voltage | | | 0.4 | V | $I_{OL} = 3.2 \text{ mA}$ |
| V_{OH} | Output High Voltage | 2.4 | | | V | $I_{OH} = -200 \mu\text{A}$ |
| V_{CC} | Supply Voltage | 4.5 | 5.0 | 5.5 | V | |
| I_{CC} | Supply Current | | | 100 | mA | All Outputs Open |

PRELIMINARY
 Note: This is not a final specification.
 Some parameters limits are subject to change.

AC ELECTRICAL CHARACTERISTICS: $T_A = 0^\circ\text{C to } 50^\circ\text{C}; V_{CC} = +5V \pm 10\%; V_{SS} = 0V$

| SYMBOL | PARAMETER | MIN | TYP ¹ | MAX | UNIT | CONDITION |
|----------|---|-----|------------------|------|------|-----------|
| f_{FR} | WCLK FREQUENCY | | | 5.25 | MHZ | |
| t_{DS} | Data Setup w.r.t. \downarrow WCLK | 10 | | | nsec | |
| t_{DH} | Data hold w.r.t. \downarrow WCLK | 25 | | | nsec | |
| t_{MF} | \downarrow WCLK to \uparrow MFM delay | | | 210 | nsec | Pin 1 LOW |
| t_{FM} | \downarrow WCLK to \downarrow MFM delay | | | 230 | nsec | Pin 1 LOW |
| t_{WN} | Data delay to NOM from \downarrow WCLK | | | 240 | nsec | |
| t_{WE} | Data delay to EARLY from \downarrow WCLK | | | 230 | nsec | |
| t_{WL} | Data delay to LATE from \downarrow WCLK | | | 230 | nsec | |
| t_{MR} | Master reset pulse width | 50 | | | nsec | |
| t_{MD} | \downarrow MR to \uparrow DRQ | | | 150 | nsec | |
| t_{MI} | \downarrow MR to \uparrow INTRQ | | | 150 | nsec | |
| t_{DD} | $\overline{\text{DRQCLK}}$ pulse width | 50 | | | nsec | |
| t_{ID} | $\overline{\text{INTCLK}}$ pulse width | 50 | | | nsec | |
| t_{OD} | \downarrow DRQCLK to DRQ | | | 120 | nsec | |
| t_{II} | \downarrow INTCLK to INTRQ | | | 120 | nsec | |
| t_{AD} | \downarrow AX to \uparrow DRQ | | | 145 | nsec | |
| t_{AI} | \uparrow AX to \uparrow INTRQ | | | 160 | nsec | |
| t_{CD} | \downarrow CS to \uparrow DRQ | | | 145 | nsec | |
| t_{CI} | \downarrow CS to \uparrow INTRQ | | | 180 | nsec | |
| t_{RN} | \uparrow RWC to . NOM | | | 145 | nsec | |
| t_{TE} | \downarrow 2XDR to \uparrow EARLY | | | 75 | nsec | |
| t_{TN} | \downarrow 2XDR to \uparrow NOM | | | 75 | nsec | |
| t_{TL} | \downarrow 2XDR to \uparrow LATE | | | 75 | nsec | |

Notes: 1. Typical Values are for $T_A = 25^\circ\text{C}$ and $V_{CC} = +5.0V$.

