MK2069-04

VCXO-Based Universal Clock Translator

Description

The MK2069-04 is a VCXO (Voltage Controlled Crystal Oscillator) based clock generator that features a PLL (Phase-Locked Loop) input reference divider and feedback divider that have a wide numeric range selectable by the user. This enables a complex PLL multiplication ratio that can be used for translation between clock frequency standards.

The on-chip VCXO produces a stable, low jitter output clock using a phase detector frequency down to 8 kHz or lower. This means the MK2069-04 can translate between clock frequencies that have a low common denominator, such as the 8 kHz frame clock common with telecom standards. The MK2069-04 also provides jitter attenuation of the input clock and can accept a low input frequency as well.

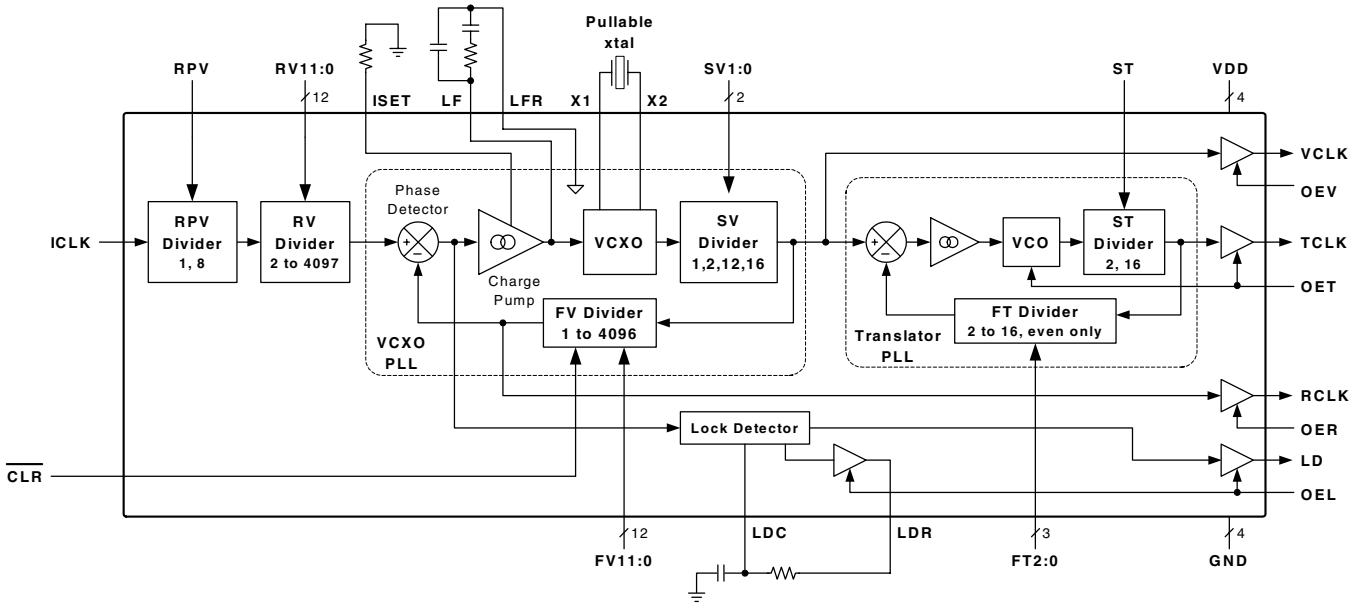
The device is optimized for user configurability by providing access to all major PLL divider functions. No power-up programming is needed as configuration is pin selected. External VCXO loop filter components provide an additional level of user configurability.

The MK2069-04 includes a lock detector (LD) output that serves as a clock status monitor. The clear ($\overline{CLR}$) input enables rapid synchronization to the phase of a newly selected input clock.

Features

- Input clock frequency <1kHz to 170MHz
- Output clock frequency of 500kHz to 160MHz
- Clock translation examples:
  - T1 (1.544MHz) to/from E1 (2.048MHz)
  - T3 (44.736MHz) to/from E3 (34.368MHz)
  - OC-3 (155.52MHz) to/from T1 (1.544 MHz)
  - CCIR-601 (27MHz) to/from SMPTE 274M (74.125MHz)
- Jitter attenuation of input clock provided by VCXO circuit. Jitter transfer characteristics user configured through external loop filter component selection.
- Low jitter and phase noise generation.
- PLL lock status output
- PLL Clear function allows seamless synchronizing to an altered input clock phase
- 2nd PLL provides frequency translation of VCXO PLL output (VCLK) to a higher or alternate output frequency (TCLK).
- Device will free-run in the absence of an input clock based on VCXO frequency.
- 56 pin TSSOP package
- Single 3.3V power supply
- 5V tolerant clock input

Block Diagram



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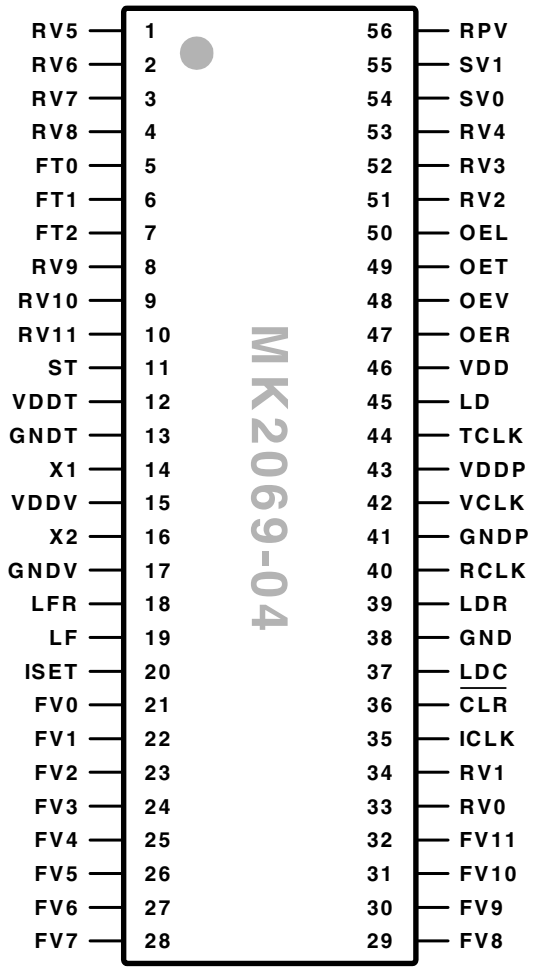
Pin Assignment



Input Selection Tables

VCXO PLL Reference Pre-Divider Selection Table

RPV	RPV Pre-Divider Ratio
0	1
1	8

VCXO PLL Reference Divider Selection Table

RV11:0	RV Divider Ratio	Notes
0...00	2	RV Divide Value = Address + 2
0...01	3	
:	:	
1...11	4097	

VCXO PLL Feedback Divider Selection

FV11:0	FV Divider Ratio	Notes
0...00	2	For FV addresses 0 to 4094, FV Divide Value = Address + 2
0...01	3	
:	:	
1...10	4096	
1...11	1	

VCXO PLL Scaling Divider Selection Table

SV1	SV0	SV Divider Ratio
0	0	12
0	1	2
1	0	16
1	1	1

Translator PLL Feedback Divider Selection

FT2	FT1	FT0	FT Divider Ratio
0	0	0	4
0	0	1	6
0	1	0	8
0	1	1	10
1	0	0	12
1	0	1	14
1	1	0	16
1	1	1	2

Translator PLL Scaling Divider Selection Table

ST	ST Divider Ratio
0	2
1	16

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Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	RV5	Input	Reference Divider bit 5 input, VCXO PLL, internal pull-up.
2	RV6	Input	Reference Divider bit 6 input, VCXO PLL, internal pull-up.
3	RV7	Input	Reference Divider bit 7 input, VCXO PLL, internal pull-up.
4	RV8	Input	Reference Divider bit 8 input, VCXO PLL, internal pull-up.
5	FT0	Input	Feedback Divider bit 0 input, Translator PLL, internal pull-up.
6	FT1	Input	Feedback Divider bit 1 input, Translator PLL, internal pull-up.
7	FT2	Input	Feedback Divider bit 2 input, Translator PLL, internal pull-up.
8	RV9	Input	Reference Divider bit 9, VCXO PLL, internal pull-up.
9	RV10	Input	Reference Divider bit 10, VCXO PLL, internal pull-up.
10	RV11	Input	Reference Divider bit 11, VCXO PLL, internal pull-up.
11	ST	Input	Scaling Divider selection bit, Translator PLL, internal pull-up.
12	VDDT	Power	Power Supply connection for translator PLL.
13	GNDT	Ground	Ground connection for translator PLL.
14	X1	-	Crystal oscillator input. Connect this pin to the external quartz crystal.
15	VDDV	Power	Power Supply connection for VCXO PLL.
16	X2	-	Crystal oscillator output. Connect this pin to the external quartz crystal.
17	GNDV	Ground	Ground connection for VCXO PLL.
18	LFR	-	Loop filter connection, reference node. Refer to loop filter circuit on page 6.
19	LF	-	Loop filter connection, active node. Refer to loop filter circuit on page 6.
20	ISET	-	Charge pump current setting pin. Refer to loop filter circuit on page 6.
21	FV0	Input	Feedback Divider bit 0 input, VCXO PLL, internal pull-up.
22	FV1	Input	Feedback Divider bit 1input, VCXO PLL, internal pull-up.
23	FV2	Input	Feedback Divider bit 2 input, VCXO PLL, internal pull-up.
24	FV3	Input	Feedback Divider bit 3 input, VCXO PLL, internal pull-up.
25	FV4	Input	Feedback Divider bit 4 input, VCXO PLL, internal pull-up.
26	FV5	Input	Feedback Divider bit 5 input, VCXO PLL, internal pull-up.
27	FV6	Input	Feedback Divider bit 6 input, VCXO PLL, internal pull-up.
28	FV7	Input	Feedback Divider bit 7 input, VCXO PLL, internal pull-up.
29	FV8	Input	Feedback Divider bit 8 input, VCXO PLL, internal pull-up.
30	FV9	Input	Feedback Divider bit 9 input, VCXO PLL, internal pull-up.
31	FV10	Input	Feedback Divider bit 10 input, VCXO PLL, internal pull-up.
32	FV11	Input	Feedback Divider bit 11 input, VCXO PLL, internal pull-up.
33	RV0	Input	Reference Divider bit 0, VCXO PLL, internal pull-up.
34	RV1	Input	Reference Divider bit 1, VCXO PLL, internal pull-up.
35	ICLK	Input	Reference clock input, 5V tolerant input
36	$\overline{CLR}$	Input	Clear input, allows VCXO to free-run when low, internal pull-up.
37	LDC	-	Lock detector threshold setting circuit connection. Refer to circuit on page 10.
38	GND	Ground	Ground connection for internal digital circuitry.
39	LDR	Power	Lock detector threshold setting circuit connection. Refer to circuit on page 10.
40	RCLK	-	VCXO PLL phase detector Reference Clock output.
41	GNDP	Ground	Ground connection for output drivers (VCLK, TCLK, RCLK, LD, LDR).

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Pin Number	Pin Name	Pin Type	Pin Description
42	VCLK	Output	Clock output from VCXO PLL
43	VDDP	Power	Power Supply for output drivers (VCLK, TCLK, RCLK, LD, LDR).
44	TCLK	Output	Clock output from Translator PLL
45	LD	Output	Lock detector output.
46	VDD	Power	Power Supply connection for internal digital circuitry.
47	OER	Input	Output enable for RCLK. RCLK is tri-stated when low, internal pull-up.
48	OEV	Input	Output enable for VCLK. VCLK is tri-stated when low, internal pull-up.
49	OET	Input	Output enable for TCLK. TCLK is tri-stated when low, internal pull-up.
50	OEL	Input	Output enable for LD. LD is tri-stated when low, internal pull-up.
51	RV2	Input	Reference Divider bit 2 input, VCXO PLL, internal pull-up.
52	RV3	Input	Reference Divider bit 3 input, VCXO PLL, internal pull-up.
53	RV4	Input	Reference Divider bit 4 input, VCXO PLL, internal pull-up.
54	SV0	Input	Scaler Divider bit 0 input, VCXO PLL, internal pull-up.
55	SV1	Input	Scaler Divider bit 1 input, VCXO PLL, internal pull-up.
56	RPV	Input	RPV divider, VCXO PLL, internal pull-up.

Functional Description

The MK2069-04 is a PLL (Phase Locked Loop) based clock generator that generates output clocks synchronized to an input reference clock. It contains two cascaded PLL's with user selectable divider ratios.

The first PLL is VCXO-based and uses an external pullable crystal as part of the normal "VCO" (voltage controlled oscillator) function of the PLL. The use of a VCXO assures a low phase noise clock source even when a low PLL loop bandwidth is implemented. A low loop bandwidth is needed when the input reference frequency at the phase detector is low, or when jitter attenuation of the input reference is desired.

The second PLL is used to translate or multiply the frequency of the VCXO PLL which has a maximum output frequency of 27 MHz. This second PLL, or Translator PLL, uses an on-chip VCO circuit that can provide an output clock up to 160 MHz. The Translator PLL uses a high loop bandwidth (typically greater than 1 MHz) to assure stability of the clock output generated by the VCO. It requires a stable, high frequency input reference which is provided by the VCXO.

The divide values of the divider blocks within both PLLs are set by device pin configuration. This enables the system designer to define the following:

- Input clock frequency
- VCXO crystal frequency
- VCLK output frequency
- RCLK output frequency, which is also the phase detector frequency of the VCXO PLL.
- TCLK output frequency

Any unused clock or logic outputs can be tri-stated to reduce interference (jitter, phase noise) on other clock outputs. Outputs can also be tri-stated for system testing purposes.

External components are used to configure the VCXO PLL loop response. This serves to maximize loop stability and to achieve the desired input clock jitter attenuation characteristics.

Application Information

The MK2069-04 is a mixed analog / digital integrated circuit that is sensitive to PCB (printed circuit board) layout and external component selection. Used properly, the device will provide the same high performance expected from a canned VCXO-based hybrid timing device, but at a lower cost. To help avoid unexpected problems, the guidance provided in the sections below should be followed.

Setting VCLK Output Frequency

The frequency of the VCLK output is determined by the following relationship:

$$f(VCLK) = \frac{FV\ Divider}{RPV\ Divider \times RV\ Divider} \times f(ICLK)$$

Where:
FV Divider = 1 to 4096
RPV Divider = 1 or 8
RV Divider = 2 to 4097

Because the RPV divider inherently has a higher speed of operation than the RV divider, the RPV divider should be set to 8 when this factor is included in the RPV x RV divisor combination.

VCLK output frequency range is set by the allowable frequency range of the external VCXO crystal and by the internal VCXO divider selections:

$$f(VCLK) = \frac{f(VCXO)}{SV\ Divider}$$

Where:
F(VCXO) = F(External Crystal) = 8 to 27 MHz
SV Divider = 1,2,4,6,8,10,12 or 16

A higher crystal frequency will generally produce lower phase noise and therefore is preferred. A crystal frequency between 13.5 MHz and 27 MHz is recommended.

Because VCLK is generated by the external crystal, the tracking range of VCLK in a given configuration is limited by the pullable range of the crystal. This is guaranteed to be +/-115 ppm minimum. This tracking range in ppm also applies to the input clock and all clock outputs if the device is to remain frequency locked to the input, which is required for normal operation.

Setting TCLK Output Frequency

The clock frequency of TCLK is determined by:

$$f(TCLK) = FT\ Divider \times f(VCLK)$$

Where:
FT Divider = 2, 4, 6, 8, 10, 12, 14 or 16

The frequency range of TCLK is set by the operational range of the internal VCO circuit and the output divider selections:

$$f(TCLK) = \frac{f(VCO)}{ST\ Divider}$$

Where:
f(VCO) = 40 to 320 MHz
ST Divider = 2,4,8 or 16

A higher VCO frequency will generally produce lower phase noise and therefore is preferred.

MK2069-04 Loop Response and JItter Attenuation Characteristics

The MK2069-04 will reduce the transfer of phase jitter existing on the input reference clock to the output clock. This operation is known as jitter attenuation. The low-pass frequency response of the VCXO PLL loop is the mechanism that provides input jitter attenuation. Clock jitter, more accurately called phase jitter, is the overall instability of the clock period which can be measured in the time domain using an oscilloscope, for instance. Jitter is comprised of phase noise which can be represented in the frequency domain. The phase noise of the input reference clock is attenuated according to the VCXO PLL low-pass frequency response curve. The response curve, and thus the jitter attenuation characteristics, can be established through the selection of external MK2069-04 passive components and other device setting as explained in the following section.

Setting the VCXO PLL Loop Response.

The VCXO PLL loop response is determined both by fixed device characteristics and by variables set by the user. This includes the values of R_S, C_S, C_P and R_{SET} as shown in the External VCXO PLL Components figure on this page.

The VCXO PLL loop bandwidth is approximated by:

$$\text{NBW(VCO PLL)} = \frac{R_S \times I_{CP} \times K_O}{2\pi \times \text{SV Divider} \times \text{FV Divider}}$$

Where:
R_S = Value of resistor R_S in loop filter in Ohms
I_{CP} = Charge pump current in amps
(see table on page 7)
K_O = VCXO Gain in Hz/V
(see table on page 8)
SV Divider = 1,2,12 or 16
FV Divider = 1 to 4096

The above equation calculates the “normalized” loop bandwidth (denoted as “NBW”) which is approximately equal to the - 3dB bandwidth. NBW does not take into account the effects of damping factor or the second pole imposed by C_P. It does, however, provide a useful approximation of filter performance.

To prevent jitter on VCLK due to modulation of the VCXO PLL by the phase detector frequency, the following general rule should be observed:

$$\text{NBW(VCO PLL)} \leq \frac{\text{f(Phase Detector)}}{20}$$

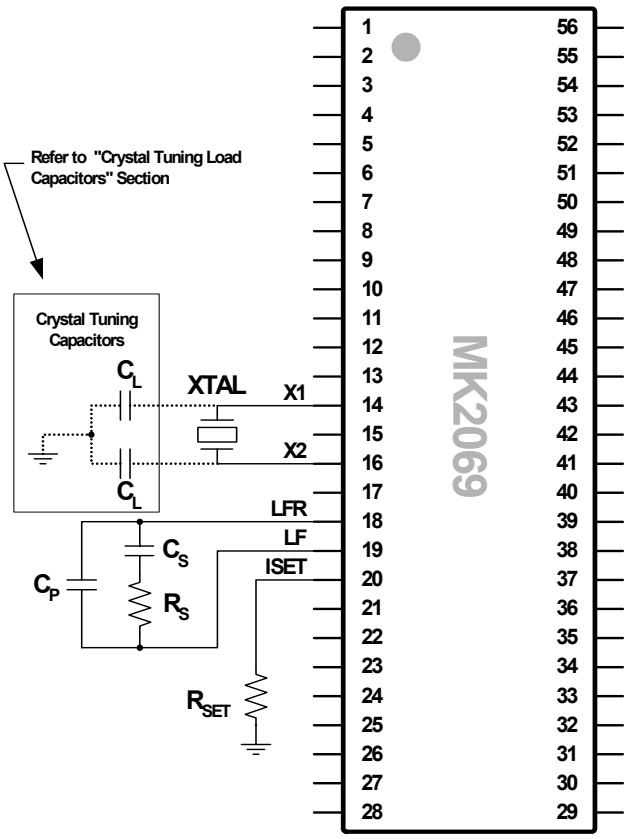
.

The PLL loop damping factor is determined by:

$$\text{DF(VCLK)} = \frac{R_S}{2} \times \sqrt{\frac{I_{CP} \times C_S \times K_O}{\text{SV Divider} \times \text{FV Divider}}}$$

Where:
C_S = Value of capacitor C_S in loop filter in Farads

External VCXO PLL Components



In general, the loop damping factor should be 0.7 or greater to ensure output stability. A higher damping factor will create less peaking in the passband and will further assure output stability with the presence of system and power supply noise. A damping factor of 4 will ensure a passband peak less then 0.2dB which may be required for network clock wander transfer compliance. A higher damping factor may also increase output clock jitter when there is excess digital noise in the system application, due to the reduced ability of the PLL to respond to and therefore compensate for phase noise ingress.

Notes on setting the value of C_P

As another general rule, the following relationship should be maintained between components C_S and C_P in the loop filter:

$$C_P = \frac{C_S}{20}$$

C_P establishes a second pole in the VCXO PLL loop filter. For higher damping factors (> 1), calculate the value of C_P based on a C_S value that would be used for a damping factor of 1. This will minimize baseband peaking and loop instability that can lead to output jitter.

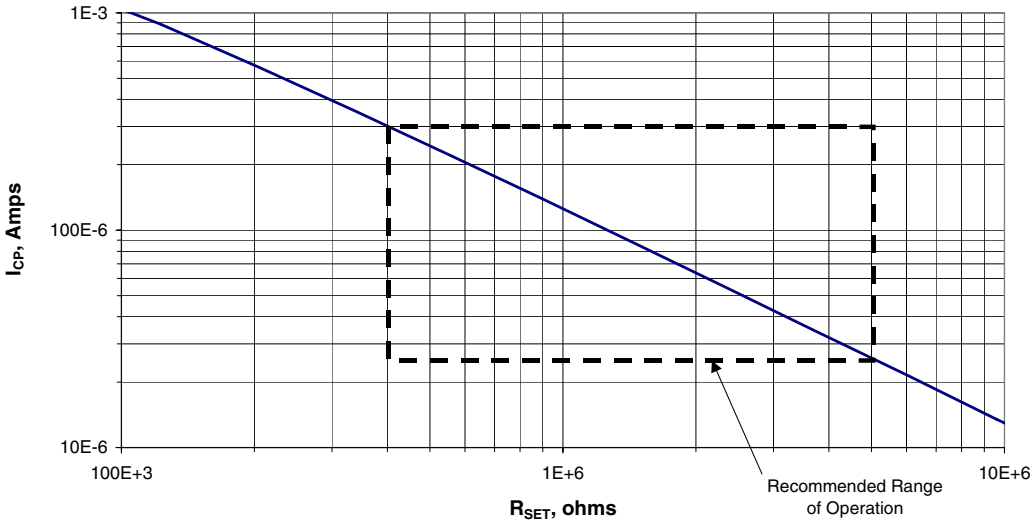
C_P also dampens VCXO input voltage modulation by the charge pump correction pulses. A C_P value that is too low will result in increased output phase noise at the phase detector frequency due to this. In extreme cases where input jitter is high, charge pump current is high, and C_P is too small, the VCXO input voltage can hit the supply or ground rail resulting in non-linear loop response.

The best way to set the value of C_P is to use the filter response software available from ICS (please refer to the following section). C_P should be increased in value until it just starts affecting the passband peak.

Loop Filter Response Software

Online tools to calculate loop filter response can be found at www.icst.com.

Graph of Charge Pump Current vs. Value of R_{SET} (external resistor)



Charge Pump Current, Example Settings from Above Graph

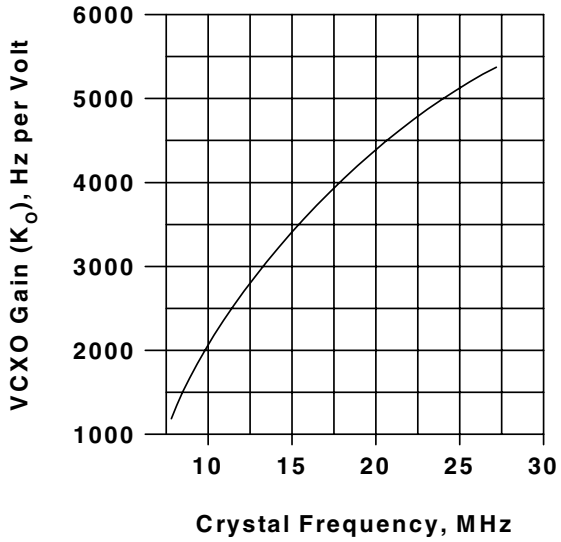
R_{SET}	Charge Pump Current (I_{CP})
5 MΩ	25 µA
3 MΩ	42 µA
2 MΩ	65 µA
1 MΩ	125 µA
480 kΩ	255 µA
400 kΩ	300 µA

Setting Charge Pump Current

The recommended range for the charge pump current is 25 µA to 300 µA. Below 25 µA, loop filter charge leakage, due to PCB or capacitor leakage, can become a problem. This loop filter leakage can cause locking problems, output clock cycle slips, or low frequency phase noise.

As can be seen in the loop bandwidth and damping factor equations or by using the filter response software available from ICS, increasing charge pump current (I_{CP}) increases both bandwidth and damping factor.

VCXO Gain (K_O) vs. XTAL Frequency



Setting the RPV, RV, FV and SV Divider Values in the VCXO PLL

As shown in the loop bandwidth and damping factor equations on page 6, or by using the filter response software available from ICS, increasing FV or SV decreases both bandwidth and damping factor. Many applications require that SV = 1. In these cases, one way to decrease loop bandwidth is to increase the value of FV, which is accompanied by an increase in the value of RPV and/or RV to maintain the same PLL frequency multiplication ratio.

However, the phase detector frequency, F_{PD}, also needs to be considered. F_{PD} is equal to the input frequency divided by the value of the RPV x RV. F_{PD} should be typically at least 20x the loop bandwidth to prevent loop modulation (phase noise) by the phase detector frequency. The phase detector jitter tolerance limit (use 0.4UI) and input phase noise frequency aliasing should be considerations as well.

Example Loop Filter Component Value

Phase Detector Frequency	Xtal Freq (MHz)	SV Div	VCLK (MHz)	FV Div	R_{SET}	R_S	C_S	C_P	Loop BW (-3dB)	Loop Damp.	Passband Peaking	Note
8 kHz	19.44	1	19.44	2430	1 MΩ	560 kΩ	1 µF	4.7 nF	22 Hz	4.0	0.15dB at 1Hz	1
8 kHz	19.44	1	19.44	2430	1 MΩ	560 kΩ	0.1 µF	4.7 nF	27 Hz	1.4	1.2dB at 6Hz	2
8 kHz	22.368	1	22.368	2796	1 MΩ	680 kΩ	1 µF	4.7 nF	20 Hz	4.5	0.12dB at 1Hz	3
19.44 MHz	19.44	1	19.44	128	1 MΩ	27 kΩ	1 µF	47 nF	25 Hz	0.85	1.8dB at 8Hz	4

Notes:

1) This filter configuration assures a passband ripple compliant with Bellcore GR-1244-CORE to satisfy wander transfer requirements (<0.2 dB ripple is required) of a network node. It can be used following a system synchronizer such as the MT9045 to provide clock jitter attenuation while maintaining Stratum 3 compliance. A 155.52 MHz TCLK output generated with the VCXO PLL configuration will be OC-3 and OC-12 timing jitter compliant.

2) This is a reduced cost and size variant of the above filter, due to the decreased size of C_S. It is useful when GR-1244-CORE compliance is not needed.

3) This configuration is used to generate a DS3 clock of 44.768 MHz at the TCLK output. This configuration is GR-1244-CORE compliant when used following a system synchronizer.

4) Lowering the phase detector frequency, by increasing the value of the RPV and/or RV dividers and the FV divider, will lower the loop bandwidth and/or decrease the size of C_S for the same damping factor.

Loop Filter Capacitor Type

Loop filters must use specific types of capacitors. Recommendations for these capacitors can be found at www.icst.com.

Input Phase Compensation Circuit

The VCXO PLL includes a special input clock phase compensation circuit. It is used when changing the phase of the input clock, which might occur when selecting a new reference input through the use of an external clock multiplexer.

The phase compensation circuit allows the VCXO PLL to quickly lock to the new input clock phase without producing extra clock cycles or clock wander, assuming the new clock is at the same frequency.

Input pin $\overline{CLR}$ controls the phase compensation circuit. $\overline{CLR}$ must remain high for normal operation. When used in conjunction with an external multiplexer (MUX), $\overline{CLR}$ should be brought low prior to MUX reselection, then returned high after MUX reselection. This prevents the VCXO PLL from attempting to lock to the new input clock phase associated with the input clock.

When $\overline{CLR}$ is high, the VCXO PLL operates normally.

When $\overline{CLR}$ is low, the VCXO PLL charge pump output is inactivated which means that no charge pump correction pulses are provided to the loop filter. During this time, the VCXO frequency is held constant by the residual charge or voltage on the PLL loop filter, regardless of the input clock condition. However, the VCXO frequency will drift over time, eventually to the minimum pull range of the crystal, due to leak-off of the loop filter charge. This means that $\overline{CLR}$ can provide a holdover function, but only for a very short duration, typically in milliseconds.

Upon bringing $\overline{CLR}$ high, the FV Divider is reset and begins counting upon with the first positive edge of the new input clock, and the charge pump is re-activated. By resetting the FV Divider, the memory of the previous input clock phase is removed from the feedback divider, eliminating the generation of extra VCLK clock cycles that would occur if the loop was to re-lock under normal means. Lock time is also reduced, as is the generation of clock wander.

By using $\overline{CLR}$ in this fashion VCLK will align to the input clock phase with only one or two VCLK cycle slips resulting. When $\overline{CLR}$ is not used, the number of VCLK cycle slips can be as high the FV Divider value.

TCLK is always locked to VCLK regardless of the state of the $\overline{CLR}$ input.

Lock Detection

The MK2069-04 includes a lock detection feature that indicates lock status of VCLK relative to the selected input reference clock. When phase lock is achieved (such as following power-up), the LD output goes high. When phase lock is lost (such as when the input clock stops, drifts beyond the pullable range of the crystal, or suddenly shifts in phase), the LD output goes low.

The definition of a “locked” condition is determined by the user. LD is high when the VCXO PLL phase detector error is below the user-defined threshold. This threshold is set by external components RLD and CLD shown in the Lock Detection Circuit Diagram, below.

To help guard against false lock indications, the LD pin will go high only when the phase error is below the set threshold for 8 consecutive phase detector cycles. The LD pin will go low when the phase error is above the set threshold for only 1 phase detector cycle.

The lock detector threshold (phase error) is determined by the following relationship:

(LD Threshold) = 0.6 x R x C

Where:

1 kΩ < R < 1 MΩ (to avoid excessive noise or leakage)

C > 50 pF (to avoid excessive error due to stray capacitance, which can be as much as 10 pF including Cin of LDC)

Lock Detector Application example:

The desired maximum allowable loop phase error for a generated 19.44MHz clock is 100UI which is 5.1 μs.

Solution: 5.1 μs = (0.001 μf) x (8.5 kΩ)

Under ideal conditions, where the VCXO is phase-locked to a low-jitter reference input, loop phase error is typically maintained to within a few nanoseconds.

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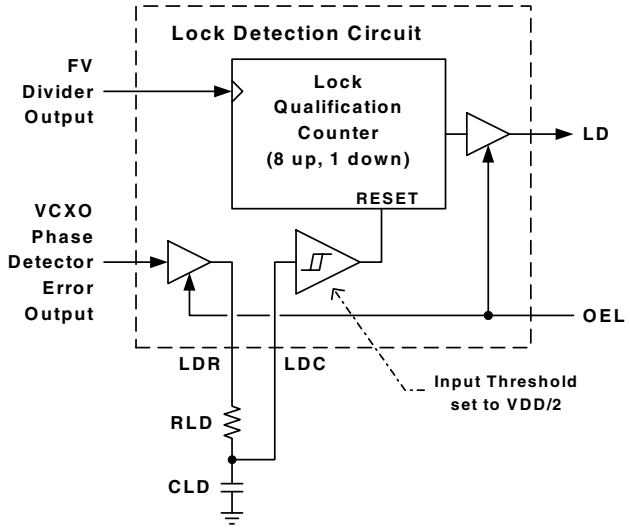
Lock Detection Circuit Diagram



If the lock detection circuit is not used, the LDR output may remain unconnected, however the LDC input should be tied high or low. If the PCB was designed to accommodate the RLD and CLD components but the LD output will not be used, RLD can remain unstuffed and CLD can be replaced with a resistor (< 10 kohm).

Power Supply Considerations

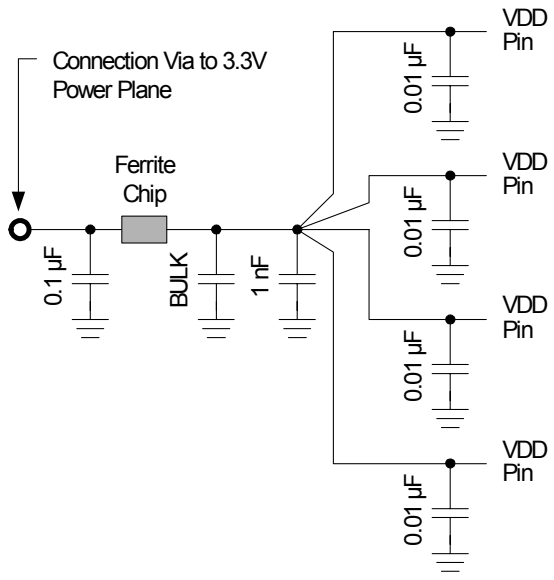
As with any integrated clock device, the MK2069-04 has a special set of power supply requirements:

- The feed from the system power supply must be filtered for noise that can cause output clock jitter. Power supply noise sources include the system switching power supply or other system components. The noise can interfere with device PLL components such as the VCO or phase detector.
- Each VDD pin must be decoupled individually to prevent power supply noise generated by one device circuit block from interfering with another circuit block.
- Clock noise from device VDD pins must not get onto the PCB power plane or system EMI problems may result.

This above set of requirements is served by the circuit illustrated in the Recommended Power Supply Connection (next page). The main features of this circuit are as follows:

- Only one connection is made to the PCB power plane.
- The capacitors and ferrite chip (or ferrite bead) on the common device supply form a lowpass 'pi' filter that remove noise from the power supply as well as clock noise back toward the supply. The bulk capacitor should be a tantalum type, 1 μF minimum. The other capacitors should be ceramic type.
- The power supply traces to the individual VDD pins should fan out at the common supply filter to reduce interaction between the device circuit blocks.
- The decoupling capacitors at the VDD pins should be ceramic type and should be as close to the VDD pin as possible. There should be no via's between the decoupling capacitor and the supply pin.

Recommended Power Supply Connection



Series Termination Resistor

Output clock PCB traces over 1 inch should use series termination to maintain clock signal integrity and to reduce EMI. To series terminate a 50Ω trace, which is a commonly used PCB trace impedance, place a 33Ω resistor in series with the clock line as close to the clock

output pin as possible. The nominal impedance of the clock output is 20Ω.

Quartz Crystal

The MK2069-04 operates by phase-locking the VCXO circuit to the input signal at the selected ICLK input. The VCXO consists of the external crystal and the integrated VCXO oscillator circuit. To achieve the best performance and reliability, a crystal device with the recommended parameters must be used, and the layout guidelines discussed in the following section must be followed.

The frequency of oscillation of a quartz crystal is determined by its cut and by the load capacitors connected to it. The MK2069-04 incorporates variable load capacitors on-chip which “pull” or change the frequency of the crystal. The crystals specified for use with the MK2069-04 are designed to have zero frequency error when the total of on-chip + stray capacitance is 14pF. To achieve this, the layout should use short traces between the MK2069-04 and the crystal.

Recommended Crystal Parameters:

Crystal parameters can be found in application note MAN05 on www.icst.com. Approved crystals can be found at www.icst.com (search “crystal”).

Crystal Tuning Load Capacitors

The crystal traces should include pads for small capacitors from X1 and X2 to ground, shown as C_L in the External VCXO PLL Components diagram on page 6. These capacitors are used to center the total load capacitor adjustment range imposed on the crystal. The load adjustment range includes stray PCB capacitance that varies with board layout. Because the typical telecom reference frequency is accurate to less than 32 ppm, the MK2069-04 may operate properly without these adjustment capacitors. However, ICS recommends that these capacitors be included to minimize the effects of variation in individual crystals, including those induced by temperature and aging. The value of these capacitors (typically 0-4 pF) is determined once for a given board layout, using the procedure described in MAN05.

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed. Please refer to the Recommended PCB Layout drawing on the following page.

1) Each 0.01µF decoupling capacitor (CD) should be mounted on the component side of the board as close to the VDD pin as possible. No via’s should be used between the decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via. Distance of the ferrite chip and bulk decoupling from the device is less critical.

2) The loop filter components must also be placed close to the CHGP and VIN pins. C_P should be closest to the device. Coupling of noise from other system signal traces should be minimized by keeping traces short and away from active signal traces. Use of vias should be avoided.

3) The external crystal should be mounted as close the device as possible, on the component side of the board. This will keep the crystal PCB traces short which will minimize parasitic load capacitance on the crystal and as well as noise pickup. The crystal traces should be spaced away from each other and should use minimum trace width. There should be no signal traces near the crystal or the traces. Also refer to the Optional Crystal Shielding section that follows.

4) To minimize EMI the 33Ω series termination resistor, if needed, should be placed close to the clock output.

5) All components should be on the same side of the board, minimizing vias through other signal layers (the ferrite bead and bulk decoupling capacitor may be mounted on the back). Other signal traces should be routed away from the MK2069-04. This includes signal traces on PCB traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

6) Because each input selection pin includes an internal pull-up device, those inputs requiring a logic high state (“1”) can be left unconnected. The pins requiring a logic low state (“0”) can be grounded.

Optional Crystal Shielding

The crystal and connection traces to pins X1 and X2 are sensitive to noise pickup. In applications that

especially sensitive to noise, such as SONET or G-Bit ethernet transceivers, some or all of the following crystal shielding techniques should be considered. This is especially important when the MK2069-04 is placed near high speed logic or signal traces.

The following techniques are illustrated on the Recommended PCB Layout drawing.

1) The metal layer underneath the crystal section should be the ground layer. Remove all other layers that are above. This ground layer will help shield the crystal circuit from other system noise sources. As an alternative, all layers underneath the crystal can be removed, however this is not recommended if there are adjacent PCBs that can induce noise into the unshielded crystal circuit.

2) Cut a channel in the PCB ground plane around the crystal area as shown. This will eliminate high frequency ground currents that can couple into to crystal circuit.

3) Add a through-hole for the optional third lead offered by the crystal manufacturer (case ground). The requirement for this third lead can be made at prototype evaluation. The crystal is less sensitive to system noise interference when the case is grounded.

4) Add a ground trace around the crystal circuit to shield from other active traces on the component layer.

The external crystal is particularly sensitive to other system clock sources that are at or near the crystal frequency since it will try to lock to the interfering clock source. The crystal should be keep away from these clock sources.

The ICS Applications Note MAN05 may also be referenced for additional suggestions on layout of the crystal section.

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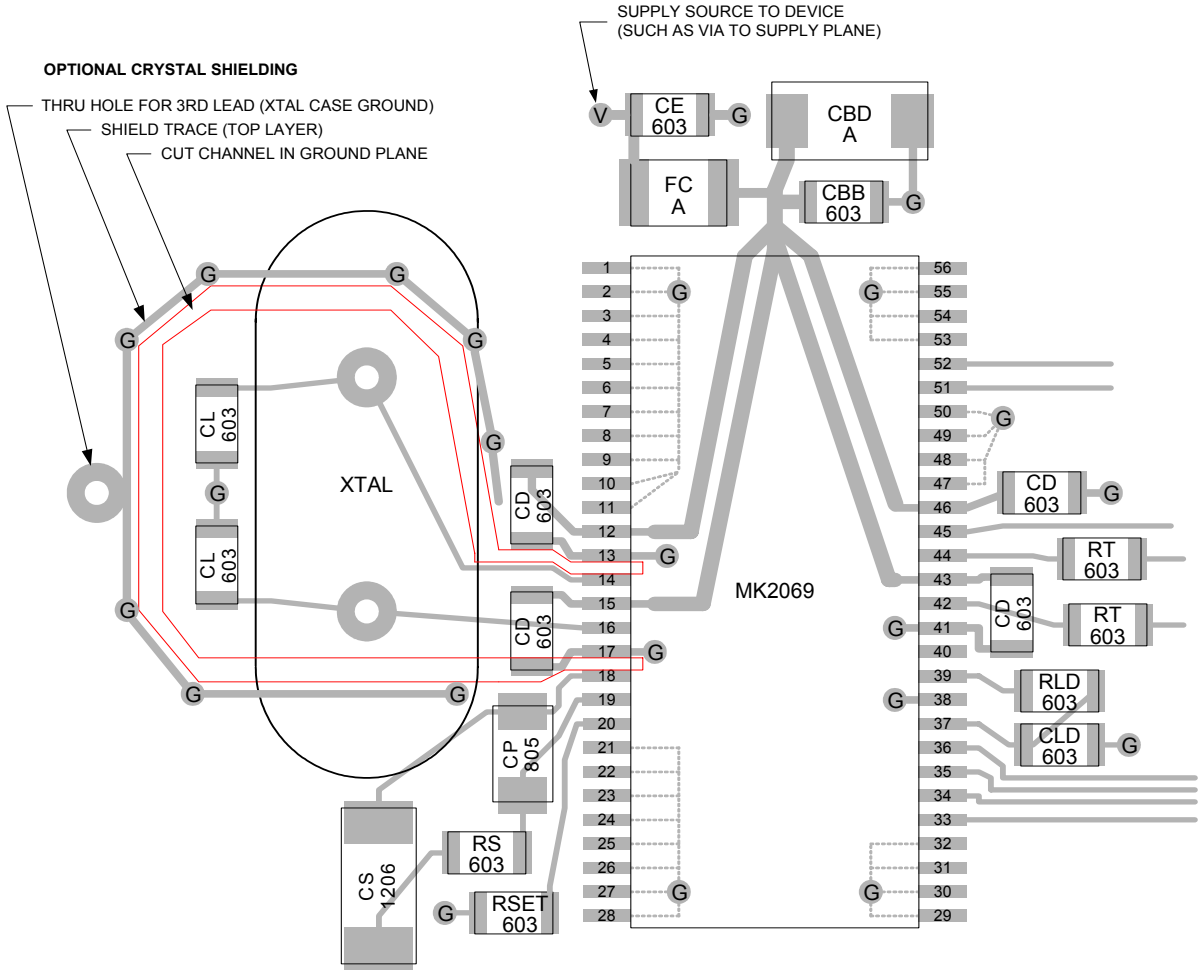
Recommended PCB Layout Diagram



Components are identified by function (top line) and by typical package type (bottom line) which may vary.

Legend:

G = Via to PCB Ground plane

V = Via to PCB Power Plane

CE = EMI suppression cap, typical value 0.1 µF (ceramic)

FC = Ferrite chip

CBD = Bulk decoupling capacitor for chip power supply, 1 µF minimum (tantalum)

CBB = Bulk bypass cap for chip power supply, typical value 1000 nF (ceramic)

CD = Decoupling capacitor for VDD pin (ceramic)

CL = Optional load capacitor for crystal tuning (do not stuff)

C_S = External loop capacitor C_S (film type)

C_P = External loop capacitor C_P (film type)

R_S = External loop resistor R_S

RSET = Resistor RSET used to determine charge pump current

RT = Series termination resistor for clock output, typical value 33 Ω

RLD* = External resistor for lock detector circuit

CLD* = External capacitor for lock detector circuit

*Note: If output LD is not used, RLD and CLD may be omitted. See text on page 10.

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Circuit Troubleshooting

1) IF TCLK or VCLK does not lock to ICLK

First check VCLK to ICLK. It is best to display and trigger the scope with RCLK, especially if a non-integer VCXO PLL multiplication ratio is used.

If VCLK is not locked to ICLK:

1.1) Ensure the proper ICLK input is selected.

1.2) Check RPV, RV, SV, FV Divider settings

1.3) Ensure ICLK is within lock range (within about 100 ppm of the nominal input frequency, limited by pull range of the external crystal). If in doubt, tweak the ICLK frequency up and down to see if VCLK locks.

1.4) Ensure ICLK jitter is not excessive. If ICLK jitter is excessive device may not lock. Also see item 2.1 below.

1.5) Clean the PCB. The VCXO PLL loop filter is very sensitive to board leakage, especially when the VCXO PLL phase detector frequency is in the low kHz. If organic solder flux is used (most common today) scrub the PCB board with detergent and water and then blow and bake dry. Inorganic solder flux (Rosen core) requires solvent. See also section 3 below.

2) If There is Excessive Jitter on VCLK or TCLK

2.1) The problem may be an unstable input reference clock. An unstable ICLK will not appear to jitter when ICLK is used as the oscilloscope trigger source. In this condition, VCLK and TCLK may appear to be unstable since the jitter from ICLK (the trigger source) has been removed by the trigger circuit of the scope.

2.2) The instability may be caused by VCXO PLL loop filter leakage. Refer to item 1.5 above.

2.3) VCLK and TCLK jitter can also be caused by poor power supply decoupling. Ensure a bulk decoupling capacitor is in place.

2.4) Ensure that the VCXO PLL loop bandwidth is sufficiently low. It should be at least 1/20th of the phase detector frequency.

2.5) Ensure that the VCXO PLL loop damping is sufficient. If should be at least 0.7, preferably 1.0 or higher.

2.6) Ensure that the 2nd pole in the VCXO PLL loop filter is set sufficiently. In general, C_P should be equal to $C_S/20$. If C_P is too high, passband peaking will occur and loop instability may occur. If C_P is set too low, excessive VCXO modulation by the charge correction pulses may occur.

3) If There is Excessive Input to Output Skew

3.1) TCLK should track VCLK. The rising edge of TCLK should be within a few nanoseconds of VCLK.

3.1) VCLK should track RCLK. The rising edge of VCLK should be within 5-10 nsec of RCLK (VCLK leads).

3.3) The biggest cause of input to output skew is VCXO PLL loop filter leakage. Skew is best observed by comparing ICLK to RCLK. When no leakage is present the rising edge of RCLK should lag the rising edge of ICLK by about 10 μsec. Loop filter leakage can greatly increase this lag time or cause the loop to not lock. Refer to item 1.5, above.

3.4) Another way to view the loop filter leakage is to observe LDR pin. Use RCLK as the scope trigger. LDR will produce a negative pulse equal in length to the charge pump pulse.

3.5) Filter leakage can also be caused by the use of improper loop capacitors. Refer to the section titled ‘Loop Filter Capacitor Type’ on page 9.

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Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK2069-04. These ratings, which are standard values for ICS industrial rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7V
All Inputs and Outputs	-0.5V to VDD+0.5V
Ambient Operating Temperature	-40 to +85°C
Storage Temperature	-65 to +150°C
Junction Temperature	175°C
Soldering Temperature	260°C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	-40		+85	°C
Power Supply Voltage (measured in respect to GND)	+3.15	+3.3	+3.45	V

DC Electrical Characteristics

Unless stated otherwise, VDD = 3.3V ±5%, Ambient Temperature -40 to +85°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.15	3.3	3.45	V
Supply Current	IDD	All clock outputs loaded with 15 pF, VCLK = 19.44 MHz, TCLK = 155.52 MHz		20	30	mA
Input High Voltage, RPV1:0, RV11:0, FV11:0, SV1:0, FT2:0, ST1:0	V_{IH}		2		VDD + 0.4	V
Input Low Voltage, RPV1:0, RV11:0, FV11:0, SV1:0, FT2:0, ST1:0	V_{IL}		-0.4		0.8	V
Input Pull-Up Resistor (Note 1)	R_{PU}			200		kΩ
Input High Voltage, $\overline{CLR}$	V_{IH}		VDD/2+1		VDD + 0.4	V
Input High Voltage, ICLK (Note 2)	V_{IH}		VDD/2+1		5.5	V
Input Low Voltage, ICLK, $\overline{CLR}$	V_{IL}		-0.4		VDD/2-1	V
Input High Current (Note 1)	I_{IH}	V_{IH} = VDD	-10		+10	µA
Input Low Current (Note 1)	I_{IL}	V_{IL} = 0	-10		+10	µA
Input Capacitance, except X1	C_{IN}			7		pF
Output High Voltage (CMOS Level)	V_{OH}	I_{OH} = -4 mA	VDD-0.4			V
Output High Voltage	V_{OH}	I_{OH} = -8 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 4 mA			0.4	V
Output Short Circuit Current, TCLK	I_{OS}			±50		mA
Output Short Circuit Current, VCLK, RCLK and LD	I_{OS}			±20		mA
VIN, VCXO Control Voltage	V_{XC}		0		VDD	V

Note 1: All logic select inputs (RPV1:0, RV11:0, FV11:0, SV1:0, FT2:0, ST1:0, CLR) have an internal pull-up resistor.

Note 2: ICLK can safely be brought to V_{IH} max prior to the application of VDD, providing utility in hot-plug line card applications.

AC Electrical Characteristics

Unless stated otherwise, VDD = 3.3V ±5%, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Crystal Frequency Range (Note 1)	f_{XTAL}	Using recommended crystal	13.5		27	MHz
VCXO Crystal Pull Range	f_{XP}	Using recommended crystal	±115	±150		ppm
VCXO Crystal Free-Run Frequency (Note 2)	f_{XF}	Input reference = 0 Hz	-300	-150		ppm
Input Clock Frequency when RPV Divider = 8 (Note 3)	f_I		0.008		170	MHz
Input Clock Frequency when RPV Divider = 1 (Note 3, 4)	f_I		0.002		160	MHz
Input Clock Pulse Width	t_{ID}	Positive or Negative Pulse	10			nsec
VCXO PLL Phase Detector Frequency (Note 3)	f_{PD}		0.001		27	MHz
VCXO PLL Phase Detector Jitter Tolerance	t_{JT}	1 UI = phase detector period		0.4		UI
Translator PLL VCO Frequency	f_V		40		320	MHz
Timing Jitter, Filtered 500Hz-1.3MHz (OC-3)	t_{OJf}	Derived from phase noise characteristics, peak-to-peak 6 sigma		95		ps
Timing Jitter, Filtered 65kHz-5MHz (OC-3)	t_{OJf}	Derived from phase noise characteristics, peak-to-peak 6 sigma		85		ps
Timing Jitter, Filtered 1kHz-5MHz (OC-12)	t_{OJf}	Derived from phase noise characteristics, peak-to-peak 6 sigma		105		ps
Timing Jitter, Filtered 250kHz-5MHz (OC-12)	t_{OJf}	Derived from phase noise characteristics, peak-to-peak 6 sigma		80		ps
Output Duty Cycle (% high time), VCLK when SV Divider = 1	t_{OD}	Measured at VDD/2, C_L=15pF	40	50	60	%
Output Duty Cycle (% high time), VCLK when SV Divider > 1, TCLK	t_{OD}	Measured at VDD/2, C_L=15pF	44	50	65	%
Output High Time, RCLK (Note 5)	t_{OH}	Measured at VDD/2, C_L=15pF		0.5 VCLK Period		

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Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output Rise Time, VCLK and RCLK	t_{OR}	0.8 to 2.0V, C_L=15pF		1.5	2	ns
Output Fall Time, VCLK and RCLK	t_{OF}	2.0 to 0.8V, C_L=15pF		1.5	2	ns
Output Rise Time, TCLK	t_{OR}	0.8 to 2.0V, C_L=15pF		0.75	1	ns
Output Fall Time, TCLK	t_{OF}	2.0 to 0.8V, C_L=15pF		0.75	1	ns
Skew, ICLK to VCLK (Note 6)	t_{IV}	Rising edges, C_L=15pF	-5	2.5	+10	ns
Skew, ICLK to RCLK (Note 6)	t_{IV}	Rising edges, C_L=15pF	+5	10	+20	ns
Skew, ICLK to TCLK (Note 6)	t_{VT}	Rising edges, C_L=15pF	-5	1.5	+10	ns
Nominal Output Impedance	Z_{OUT}			20		Ω

Note 1: This is the recommended crystal operating range. A crystal as low as 8 MHz can be used, although this may result in increased output phase noise.

Note 2: The VCXO crystal will be pulled to its minimum frequency when there is no input clock ($\overline{CLR}$ = 1) due to the attempt of the PLL to lock to 0 Hz.

Note 3: The minimum practical phase detector frequency is 1 kHz. Through proper loop filter design lower input frequencies may be possible. Input frequencies as low as 400Hz have been tested.

Note 4: A higher input clock frequency can be used when RPV divider = 8.

Note 5: The output of RCLK is a positive pulse with a duration equal to VCLK high time, or half the VCLK period.

Note 6: Referenced to ICLK, the skews of VCLK, RCLK and TCLK increase together when leakage is present in the external VCXO PLL loop filter.

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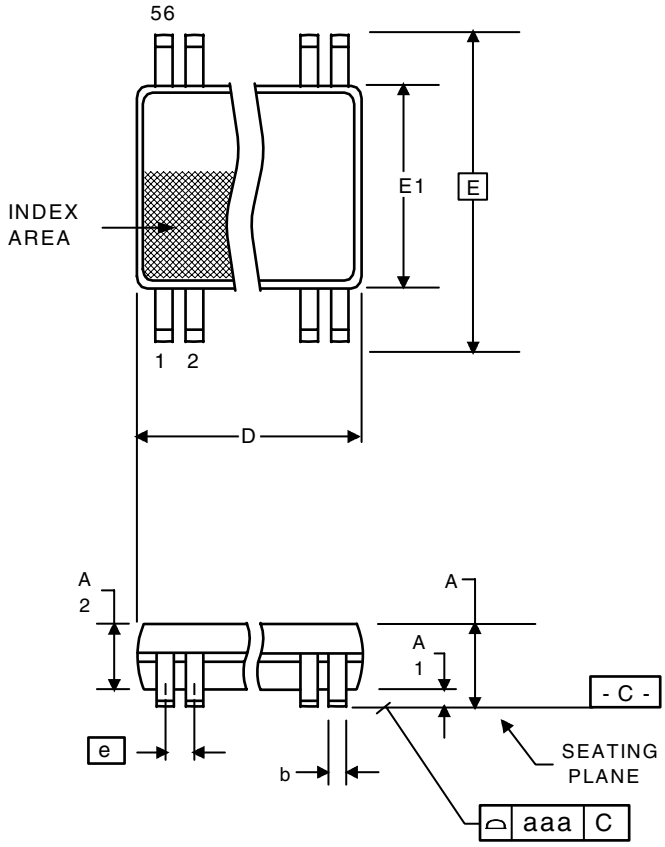
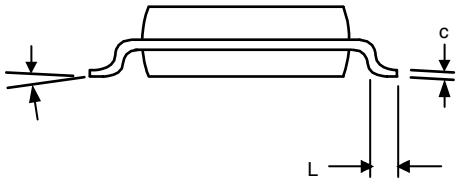
Package Outline and Package Dimensions

56 pin TSSOP 6.10 mm (240 mil) body, 0.50 mm. (20 mil) pitch
Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	--	1.20	--	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
b	0.17	0.27	0.007	0.011
C	0.09	0.20	0.0035	0.008
D	13.90	14.10	0.547	0.555
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	0.236	0.244
e	0.50 Basic		0.020 Basic	
L	0.45	0.75	0.018	0.030
α	0°	8°	0°	8°
aaa	--	0.10	--	0.004



Ordering Information

Part / Order Number	Marking	Shipping packaging	Package	Temperature
MK2069-04GI	MK2069-04GI	Tubes	56 pin TSSOP	-40 to +85° C
MK2069-04GITR	MK2069-04GI	Tape and Reel	56 pin TSSOP	-40 to +85° C