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Defense Electronics Supply Center
Dayton, Ohio

Original date of drawing: 8 DECEMBER 1987

AMSC N/A

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A	67268

REV

MILITARY DRAWING

This drawing is available for use by all Departments and Agencies of the Department of Defense

TITLE: MICROCIRCUITS, LINEAR, 8-BIT A/D CONVERTER, MONOLITHIC SILICON

DWG NO. 5962-87600

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5962-E408

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1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-87600	01	X	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	TDC1048	8-bit A/D converter

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
X	D-10 (28-lead, 1/2" x 1 1/2"), dual-in-line package
3	C-4 (28-terminal, .450" x .450"), square chip carrier package

1.3 Absolute maximum ratings.

V_{CC} to D_{GND}	-0.5 V dc to +7.0 V dc
V_{EE} to A_{GND}	+0.5 V dc to -7.0 V dc
A_{GND} to D_{GND}	-0.5 V dc to +0.5 V dc
$\overline{CONV}$, NMINV, or NLINV to D_{GND}	-0.5 V dc to +5.5 V dc
V_{IN}, V_{RT}, or V_{RB} to A_{GND}	+0.5 V dc to V_{EE}
V_{RT} to V_{RB}	-2.2 V dc to +2.2 V dc
Applied output voltage to D_{GND}	-0.5 V dc to +5.5 V dc 1/
Applied output current, externally forced	-1.0 mA to +6.0 mA 2/ 3/
Output short-circuit duration	1.0 s 4/
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Power dissipation, worst case (P_D)	2.1 W
Thermal resistance, junction-to-case (θ_{JC}):	
Cases X and 3	(See MIL-M-38510, appendix C)

1/ Applied voltage must be current limited to specified range.
2/ Forcing voltage must be limited to specified range.
3/ Current is specified as positive when flowing into the device.
4/ Single output in high state to ground.

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1.4 Recommended operating conditions.

Positive supply voltage (V_{CC})	4.5 V dc to 5.5 V dc
Negative supply voltage (V_{EE})	-4.9 V dc to -5.5 V dc
Analog ground voltage to D_{GND} (V_{AGND})	-0.1 V dc to +0.1 V dc
CONV pulse width, low (t_{PWL})	18 ns minimum
CONV pulse width, high (t_{PWH})	22 ns minimum
Input voltage, logic low (V_{IL})	0.8 V dc maximum
Input voltage, logic high (V_{IH})	2.0 V dc minimum
Output current, logic low (I_{OL})	4.0 mA maximum
Output current, logic high (I_{OH})	-400 µA maximum
Most positive reference input (V_{RT}) 5/	-0.1 V dc to +0.1 V dc
Most negative reference input (V_{RB}) 5/	-1.9 V dc to -2.1 V dc
Voltage reference differential ($V_{RT} - V_{RB}$)	1.8 V dc to 2.1 V dc
Input voltage (V_{IN})	V_{RB} to V_{RT}
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Block diagram. The block diagram shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

5/ V_{RT} must be more positive than V_{RB}, and $V_{RT} - V_{RB}$ must be within the specified range.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C < T_C < +125°C$ unless otherwise specified		Group A subgroups	Limits Min	Limits Max	Unit
Positive supply current, static	I_{CC}	V_{EE} = -4.9 V, V_{CC} = 5.5 V		1,2,3		40	mA
Negative supply current, static	I_{EE}	V_{EE} = -5.5 V		1,2,3		-320	mA
Reference current	I_{REF}	V_{EE} = -4.9 V, V_{RT} = 0 V, V_{RB} = -2.0 V		1,2,3	5.0	50	mA
Total reference resistance 2/	R_{REF}	V_{RT} = 0 V, V_{RB} = -2.0 V		1,2,3	40	400	Ω
Input equivalent resistance 2/	R_{IN}	V_{RT} = 0 V, V_{RB} = -2.0 V		1,2,3	10	4000	kΩ
Input capacitance 2/	C_{IN}	V_{RT} = 0 V, V_{RB} = -2.0 V		4,5,6		100	pF
Input constant bias current	I_{CB}	V_{EE} = -5.5 V, V_{CC} = 5.5 V		1,2,3		550	µA
Input low current	I_{IL}	V_{EE} = -4.9 V, V_{CC} = 5.5 V, V_I = 0.4 V	CONV	1,2,3		-400	µA
			NLINV, NMINV	1,2,3		-600	µA
Input high current	I_{IH}	V_{CC} = 5.5 V, V_{EE} = -4.9 V, V_I = 2.4 V		1,2,3		50	µA
Input current at maximum input voltage	I_I	V_{CC} = 5.5 V, V_{EE} = -4.9 V, V_I = 5.5 V		1,2,3		1.0	mA
Output short-circuit current 3/	I_{OS}	V_{EE} = -4.9 V, V_{CC} = 5.5 V		1,2,3		-30	mA
Output low voltage	V_{OL}	V_{EE} = -5.5 V, V_{CC} = 4.5 V, I_{OL} = 4.0 mA		1,2,3		0.5	V
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -400 µA		1,2,3	2.4		V

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Limits Min	Limits Max	Unit
Digital input capacitance 2/	C_I	f = 1.0 MHz	4		15	pF
Maximum conversion rate	F_S	V_{EE} = -4.9 V, V_{CC} = 4.5 V, F_S = 20 MHz minimum per figure 4	4,5,6	20		MSPS 4/
Functional tests		V_{EE} = -4.9 V, V_{CC} = 4.5 V, f = 1.0 MHz, see 4.3.1b	7,8			
Sampling time offset 2/	t_{STO}	See figure 4	9,10,11	0	15	ns
Digital output delay	t_D	V_{EE} = -4.9 V, V_{CC} = 5.5 V, see figure 4	9,10,11	5.0	35	ns
Digital output hold time 2/	t_{HO}	See figure 4	9,10,11	5.0		ns
Linearity error integral, independent	E_{LI}	V_{RT} = 0 V, V_{RB} = -2.0 V, F_S = 100 kHz	4,5,6		0.2	%
Linearity error, differential	E_{LD}	V_{RT} = 0 V, V_{RB} = -2.0 V, F_S = 100 kHz	4,5,6		0.2	%
Nominal size code	Q	F_S = 100 kHz	---	25	175	%
Offset error, top 2/	E_{OT}	V_{IN} = midpoint of code 0	1,2,3		+50	mV
Missing codes	Q_{MISS}	F_S = 100 kHz	---		0	codes
Offset error, bottom 2/	E_{OB}	V_{IN} = midpoint of code 255	1,2,3		-30	mV
Temperature coefficient of offset error 2/	$\frac{\Delta E_O}{\Delta T}$		1,2,3		±50	µV/°C
Bandwidth, full power input 2/	BW		4,5,6	5.0		MHz

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C < T_C < +125°C$ unless otherwise specified		Group A subgroups	Limits Min	Limits Max	Unit
Signal-to-noise ratio (20 MSPS conversion rate, 10 MHz bandwidth) 2/	SNR	Peak signal/ RMS noise	1.248 MHz input	4,5,6	53		dB
			2.438 MHz input	4,5,6	52		dB
		RMS signal/ RMS noise	1.248 MHz input	4,5,6	44		dB
			2.438 MHz input	4,5,6	43		dB
Differential phase error 2/ 5/	DP	F_S = 4 X NTSC		4,5,6		1.0	degree
Differential gain error 2/ 5/	DG	F_S = 4 X NTSC		4,5,6		2.0	%

1/ Unless otherwise specified, characteristics apply over the recommended operating conditions specified in 1.4 herein.

2/ Guaranteed if not tested.

3/ Output high, one pin to ground, one second duration maximum.

4/ Mega samples per second.

5/ In excess of quantization.

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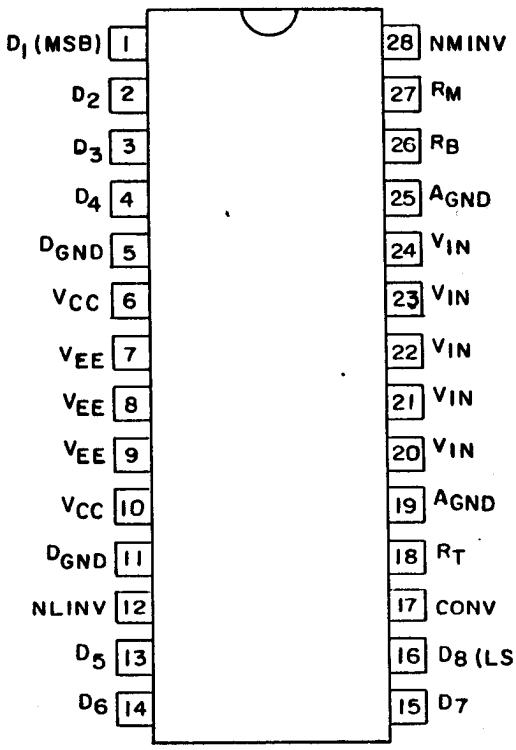
Case X

Device type 01



Case 3

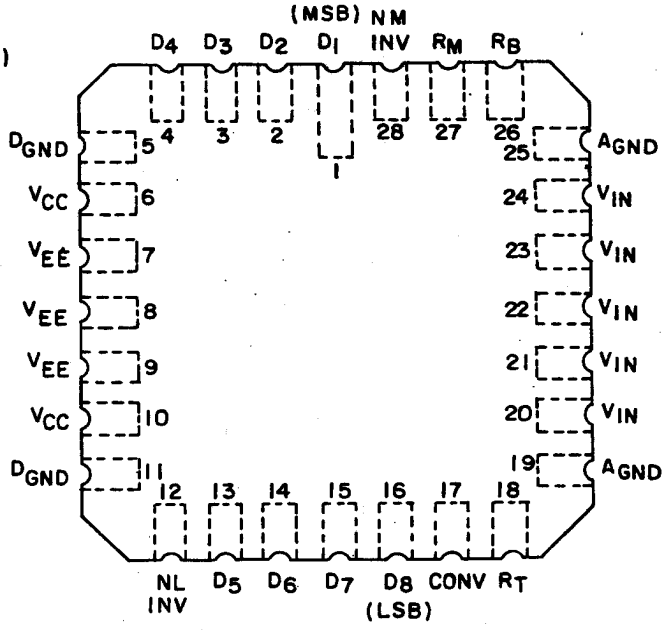


FIGURE 1. Terminal connections (top view).

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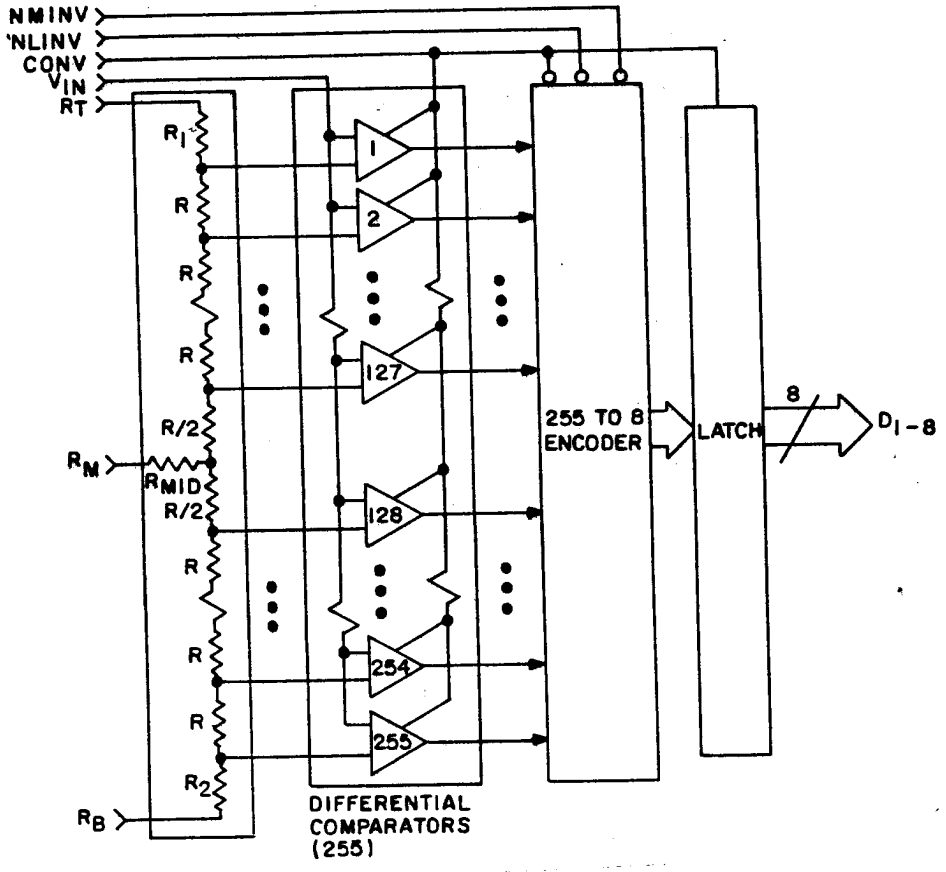

FIGURE 2. Block diagram.

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Step	Range		Binary		Offset two's complement	
			True	Inverted	True	Inverted
	-2.0000 V F_S	-2.0480 V F_S	NMINV = 1	0	0	0
	7.8431 mV Step	8.000 mV step	NLINV = 1	0	1	1
000	0.0000 V	0.0000 V	00000000	11111111	10000000	0111111
001	-0.0078 V	-0.0080 V	00000001	11111110	10000001	0111110
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
127	-0.9961 V	-1.0160 V	01111111	10000000	11111111	00000000
128	-1.0039 V	-1.0240 V	10000000	01111111	00000000	11111111
129	-1.0118 V	-1.0320 V	10000001	01111110	00000001	11111110
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
254	-1.9921 V	-2.0320 V	11111110	00000001	01111110	10000001
255	-2.0000 V	-2.0400 V	11111111	00000000	01111111	10000000

NOTES:
1. NMINV and NLINV are to be considered dc controls. They may be tied to +5.0 V for a logical "1" and tied to ground for a logical "0".
2. Voltages are code midpoints when calibrated by adjusting V_{RT} and V_{RB} to set the 1st and 255th thresholds to the desired voltages. Note that R_1 is greater than R (refer to block diagram on figure 2 herein), ensuring calibration with a positive voltage on RT. Assuming a 0 V to -2.0 V desired range, continuously strobe the converter with -0.0039 V (1/2 LSB from 0 V) on the analog input, and adjust V_{RT} for output toggling between codes 00 and 01. Then apply -1.996 V (1/2 LSB from -2.0 V) and adjust V_{RB} for toggling between codes 254 and 255.

The degree of required adjustment is indicated by the offset error, E_{OT} and E_{OB}. Offset errors are generated by the inherent parasitic resistance between the package pin and the actual resistor chain on the integrated circuit. These parasitic resistors are shown as R_1 and R_2 in the block diagram shown on figure 2. Calibration will cancel all offset voltages, eliminating offset and gain errors.

This method of calibration requires that both ends of the resistor chain, RT and RB are driven by buffered operational amplifiers. Instead of adjusting V_{RT}, RT can be connected to analog ground and the 0 V end of the range calibrated with a buffer offset control. The offset error at the bottom of the resistor chain results in a slight gain error, which can be compensated for by varying the voltage applied to RB. The bottom reference is a convenient point for gain adjust that is not in the analog signal path.

FIGURE 3. Truth table.

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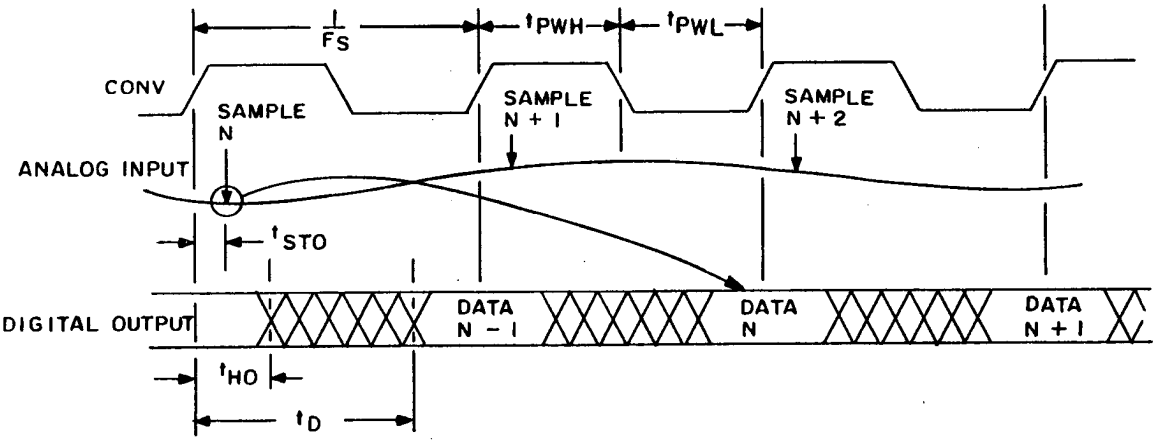

FIGURE 4. Timing diagram.

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3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 7 and 8 tests sufficient to verify the truth table.

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TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1,4,7,9
Final electrical test parameters (method 5004)	1*,2,3,4,5,6, 7*,8,9,10,11
Group A test requirements (method 5005)	1,2,3,4,5,6, 7,8,9,10,11
Groups C and D end-point electrical parameters (method 5005)	1,4,7,9

*PDA applies to subgroups 1 and 7.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test (method 1005 of MIL-STD-883) conditions:

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

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6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8760001XX	59621	TDC1048J6V
5962-87600013X	59621	TDC1048C3V

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
59621	TRW/LSI Products Division 4243 Campus Point Court San Diego, CA 92126

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