HB56HW465DB-5/5L/6/6L

32MB EDO DRAM S.O.DIMM
4-Mword × 64-bit, 4k refresh, 1 Bank Module
(4 pcs of 4M × 16 components)

HITACHI

ADE-203-861A (Z)
Rev. 1.0
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Description

The HB56HW465DB is a 4 M × 64 Dynamic RAM Small Outline Dual In-line Memory Module (S. O. DIMM), mounted 4 pieces of 64-Mbit DRAM (HM5165165) sealed in TSOP package and 1 piece of serial EEPROM for Presence Detect (PD). The HB56HW465DB offers Extended Data Out (EDO) Page Mode as a high speed access mode. An outline of the HB56HW465DB is 144-pin Zig Zag Dual tabs socket type compact and thin package. Therefore, the HB56HW465DB makes high density mounting possible without surface mount technology. The HB56HW465DB provides common data inputs and outputs. Decoupling capacitors are mounted beside each TSOP on the module board.

Features

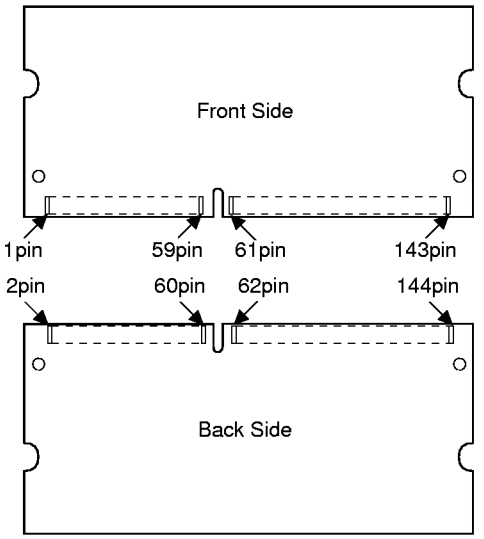
- 144-pin Zig Zag Dual tabs socket type
  - — Outline: 67.60 mm (Length) × 25.40 mm (Height) × 3.80 mm (Thickness)
  - — Lead pitch : 0.80 mm
- Single 3.3 V supply: 3.3 V ± 0.3 V
- High speed
  - — Access time: t_{RAC} = 50 ns/60 ns (max)
  - — Access time: t_{CAC} = 13 ns/15 ns (max)
- Low power dissipation
  - — Active mode: 2.02 W/1.73 W (max)
  - — Standby mode (TTL): 28.8 mW (max)
  - — Standby mode (CMOS): 7.2 mW (max)
    2.2 mW (max) (L-version)
- JEDEC standard outline S. O. DIMM
- EDO page mode capability

- 4096 refresh cycles : 64 ms
  : 128 ms (L-version)
- 4 variations of refresh
  — $\overline{\text{RAS}}$-only refresh
  — $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  — Hidden refresh
  — Self refresh (L-version)

Ordering Information

Type No.	Access time	Package	Contact pad
HB56HW465DB-5	50 ns	144-pin small outline DIMM	Gold
HB56HW465DB-6	60 ns		
HB56HW465DB-5L	50 ns		
HB56HW465DB-6L	60 ns		

Pin Arrangement



Front side				Back side			
Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name
1	V_{SS}	73	$\overline{\text{OE}}$	2	V_{SS}	74	NC
3	DQ0	75	V_{SS}	4	DQ32	76	V_{SS}
5	DQ1	77	NC	6	DQ33	78	NC
7	DQ2	79	NC	8	DQ34	80	NC

Front side				Back side			
Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name
9	DQ3	81	V_{CC}	10	DQ35	82	V_{CC}
11	V_{CC}	83	DQ16	12	V_{CC}	84	DQ48
13	DQ4	85	DQ17	14	DQ36	86	DQ49
15	DQ5	87	DQ18	16	DQ37	88	DQ50
17	DQ6	89	DQ19	18	DQ38	90	DQ51
19	DQ7	91	V_{SS}	20	DQ39	92	V_{SS}
21	V_{SS}	93	DQ20	22	V_{SS}	94	DQ52
23	$\overline{CE0}$	95	DQ21	24	$\overline{CE4}$	96	DQ53
25	$\overline{CE1}$	97	DQ22	26	$\overline{CE5}$	98	DQ54
27	V_{CC}	99	DQ23	28	V_{CC}	100	DQ55
29	A0	101	V_{CC}	30	A3	102	V_{CC}
31	A1	103	A6	32	A4	104	A7
33	A2	105	A8	34	A5	106	A11
35	V_{SS}	107	V_{SS}	36	V_{SS}	108	V_{SS}
37	DQ8	109	A9	38	DQ40	110	NC
39	DQ9	111	A10	40	DQ41	112	NC
41	DQ10	113	V_{CC}	42	DQ42	114	V_{CC}
43	DQ11	115	$\overline{CE2}$	44	DQ43	116	$\overline{CE6}$
45	V_{CC}	117	$\overline{CE3}$	46	V_{CC}	118	$\overline{CE7}$
47	DQ12	119	V_{SS}	48	DQ44	120	V_{SS}
49	DQ13	121	DQ24	50	DQ45	122	DQ56
51	DQ14	123	DQ25	52	DQ46	124	DQ57
53	DQ15	125	DQ26	54	DQ47	126	DQ58
55	V_{SS}	127	DQ27	56	V_{SS}	128	DQ59
57	NC	129	V_{CC}	58	NC	130	V_{CC}
59	NC	131	DQ28	60	NC	132	DQ60
61	NC	133	DQ29	62	NC	134	DQ61
63	V_{CC}	135	DQ30	64	V_{CC}	136	DQ62
65	NC	137	DQ31	66	NC	138	DQ63
67	$\overline{WE}$	139	V_{SS}	68	NC	140	V_{SS}
69	$\overline{RE0}$	141	SDA	70	NC	142	SCL
71	NC	143	V_{CC}	72	NC	144	V_{CC}

Pin Description

Pin name	Function
A0 to A11	Address input Row address A0 to A11 Column address A0 to A9 Refresh address A0 to A11
DQ0 to DQ63	Data input/output
$\overline{RE}0$	Row address strobe ($\overline{RAS}$)
$\overline{CE}0$ to $\overline{CE}7$	Column address strobe ($\overline{CAS}$)
$\overline{WE}$	Read/Write enable
$\overline{OE}$	Output enable
SDA	Serial data for PD
SCL	Serial clock for PD
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

Serial PD Matrix*[1]

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
0	Number of bytes used by module manufacturer	1	0	0	0	0	0	0	0	80	128
1	Total SPD memory size	0	0	0	0	1	0	0	0	08	256 byte
2	Memory type	0	0	0	0	0	0	1	0	02	EDO
3	Number of row addresses bits	0	0	0	0	1	1	0	0	0C	12
4	Number of column addresses bits	0	0	0	0	1	0	1	0	0A	10
5	Number of banks	0	0	0	0	0	0	0	1	01	1
6	Module data width	0	1	0	0	0	0	0	0	40	64 bits
7	Module data width (continued)	0	0	0	0	0	0	0	0	00	0 (+)
8	Module interface signal levels	0	0	0	0	0	0	0	1	01	LVTTL
9	$\overline{RAS}$ access time -5/5L	0	0	1	1	0	0	1	0	32	t_{RAC} = 50 ns
	$\overline{RAS}$ access time -6/6L	0	0	1	1	1	1	0	0	3C	t_{RAC} = 60 ns
10	$\overline{CAS}$ access time -5/5L	0	0	0	0	1	1	0	1	0D	t_{CAC} = 13 ns
	$\overline{CAS}$ access time -6/6L	0	0	0	0	1	1	1	1	0F	t_{CAC} = 15 ns
11	Module configuration type	0	0	0	0	0	0	0	0	00	Non parity
12	Refresh rate/type -5/6	0	0	0	0	0	0	0	0	00	Normal (15.625 µs)
	Refresh rate/type -5L/6L (L-version)	1	0	0	0	0	0	1	1	83	Self refresh (31.3 µs)
13	DRAM width	0	0	0	1	0	0	0	0	10	4M × 16
14	Error checking DRAM data width	0	0	0	0	0	0	0	0	00	
15 to 31	Reserved for future offerings	0	0	0	0	0	0	0	0	00	
32 to 61	Superset information	0	0	0	0	0	0	0	0	00	Future offerings
62	SPD revision	0	0	0	0	0	0	0	1	01	Rev. 1
63	Checksum for bytes 0 to 62 -5	0	0	1	1	0	0	1	0	32	
	Checksum for bytes 0 to 62 -6	0	0	1	1	1	1	1	0	3E	
	Checksum for bytes 0 to 62 -5L	1	0	1	1	0	1	0	1	B5	
	Checksum for bytes 0 to 62 -6L	1	1	0	0	0	0	0	1	C1	

Serial PD Matrix*[1] (cont)

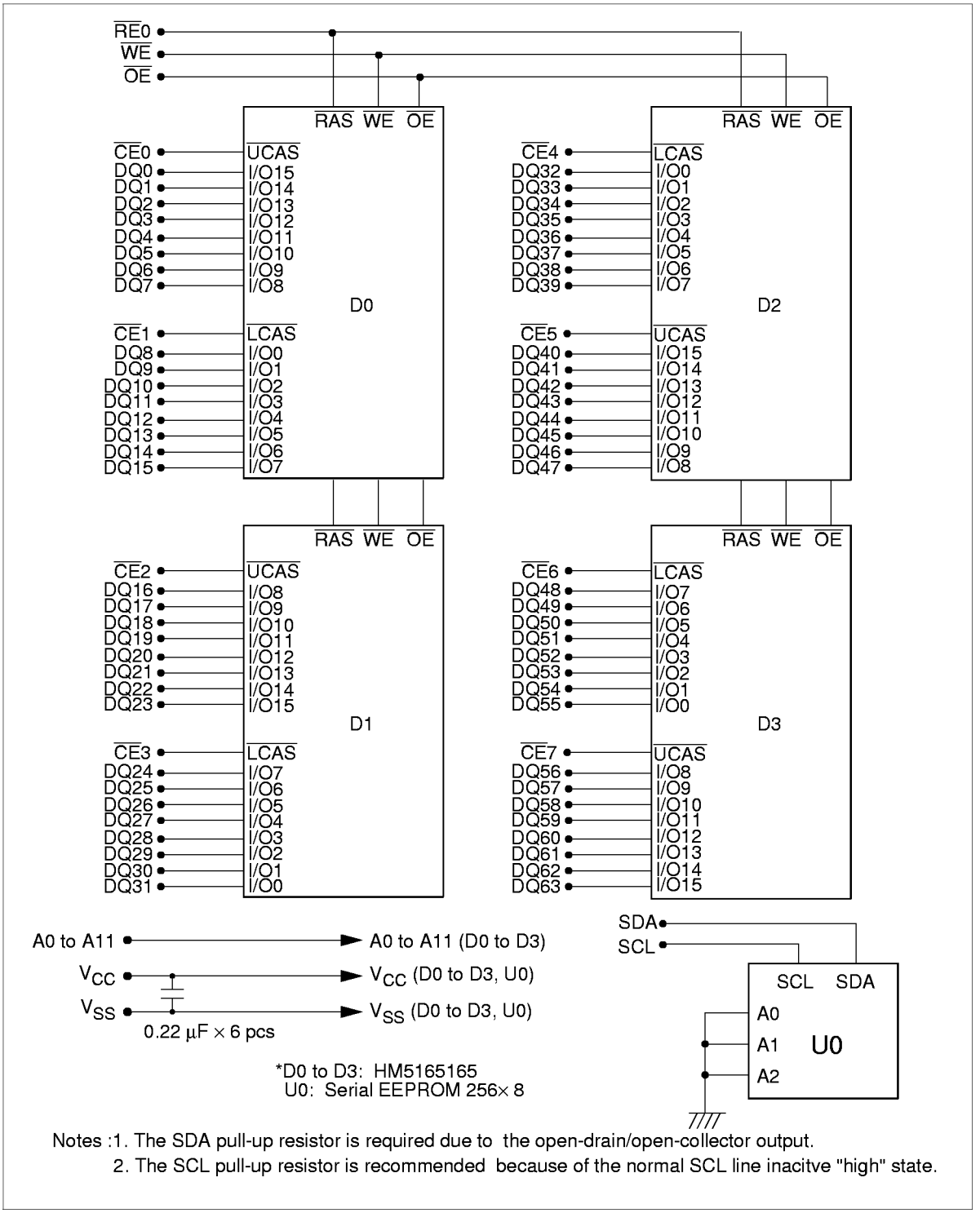
Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
64	Manufacturer's JEDEC ID code	0	0	0	0	0	1	1	1	07	Hitachi
65 to 71	Manufacturer's JEDEC ID code	0	0	0	0	0	0	0	0	00	
72	Manufacturing location	×	×	×	×	×	×	×	×	××	*[2] (ASCII-8bit code)
73	Manufacturer's part number	0	1	0	0	1	0	0	0	48	H
74	Manufacturer's part number	0	1	0	0	0	0	1	0	42	B
75	Manufacturer's part number	0	0	1	1	0	1	0	1	35	5
76	Manufacturer's part number	0	0	1	1	0	1	1	0	36	6
77	Manufacturer's part number	0	1	0	0	1	0	0	0	48	H
78	Manufacturer's part number	0	1	0	1	0	1	1	1	57	W
79	Manufacturer's part number	0	0	1	1	0	1	0	0	34	4
80	Manufacturer's part number	0	0	1	1	0	1	1	0	36	6
81	Manufacturer's part number	0	0	1	1	0	1	0	1	35	5
82	Manufacturer's part number	0	1	0	0	0	1	0	0	44	D
83	Manufacturer's part number	0	1	0	0	0	0	1	0	42	B
84	Manufacturer's part number	0	0	1	0	1	1	0	1	2D	—
85	Manufacturer's part number -5/-5L	0	0	1	1	0	1	0	1	35	5
	Manufacturer's part number -6/6L	0	0	1	1	0	1	1	0	36	6
86	Manufacturer's part number -5/6	0	0	1	0	0	0	0	0	20	(Space)
	Manufacturer's part number -5L/6L (L-version)	0	1	0	0	1	1	0	0	4C	L
87 to 90	Manufacturer's part number	0	0	1	0	0	0	0	0	20	(Space)
91	Revision code	0	0	1	1	0	0	0	0	30	Initial
92	Revision code	0	0	1	0	0	0	0	0	20	(Space)
93	Manufacturing date (year code)	×	×	×	×	×	×	×	×	××	Year code*[3] (binary)
94	Manufacturing date (week code)	×	×	×	×	×	×	×	×	××	Week code*[4] (binary)

Serial PD Matrix*[1] (cont)

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
95 to 98	Assembly serial number	*5									
99 to 125	Manufacturer specific data	*6									
126	Reserved	0	0	0	0	0	0	0	0	00	
127	Reserved	0	0	0	0	0	0	0	0	00	

Notes: 1. All serial PD data are not protected. 0: Serial data, “driven Low”, 1: Serial data, “driven High”
2. Byte 72 is manufacturing location code. (ex: in case of Japan, byte 72 is 4Ah. 4Ah shows “J” on ASCII code.)
3. Byte 93 (Manufacturing date-year code) ex: 61h shows year ‘97. 62h shows year ‘98.
4. Byte 94 (Manufacturing date-week code) ex: 0Bh shows week 11. 24h shows week 36.
5. Byte 95 through 98 are assembly serial number.
6. All bits of byte 99 through 125 are not defined (“1” or “0”).

Block Diagram



Notes :1. The SDA pull-up resistor is required due to the open-drain/open-collector output.
2. The SCL pull-up resistor is recommended because of the normal SCL line inacitve "high" state.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Terminal voltage on any pin relative to V_{SS}	V_T	–0.5 to +4.6	V
Power supply voltage relative to V_{SS}	V_{CC}	–0.5 to +4.6	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	4.0	W
Storage temperature range	Tstg	–55 to +125	°C

DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{CC}	3.0	3.3	3.6	V	1, 2
	V_{SS}	0	0	0	V	2
Input high voltage	V_{IH}	2.0	—	V_{CC} + 0.3	V	1
Input low voltage	V_{IL}	–0.3	—	0.8	V	1
Ambient temperature range	Ta	0	—	70	°C	

Notes: 1. All voltage referred to V_{SS}.
2. The supply voltage with all V_{CC} pins must be on the same level. The supply voltage with all V_{SS} pins must be on the same level.

DC Characteristics

		HB56HW465DB					
		50 ns		60 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**
Operating current*1, *2	I_{CC1}	—	560	—	480	mA	t_{RC} = min
Standby current	I_{CC2}	—	8	—	8	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z
		—	2	—	2	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z
Standby current (L-version)	I_{CC2}	—	0.6	—	0.6	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z
$\overline{RAS}$-only refresh current*2	I_{CC3}	—	560	—	480	mA	t_{RC} = min
Standby current*1	I_{CC5}	—	20	—	20	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} Dout = enable
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	560	—	480	mA	t_{RC} = min
EDO page mode current*1, *3	I_{CC7}	—	480	—	440	mA	$\overline{RAS}$ = V_{IL} , $\overline{CAS}$ cycle, t_{HPC} = t_{HPC} min
Battery backup current*4 (Standby with CBR refresh) (L-version)	I_{CC10}	—	2.0	—	2.0	mA	CMOS interface Dout = High-Z CBR refresh: t_{RC} = 31.3 µs t_{RAS} ≤ 0.3 µs
Self refresh mode current (L-version)	I_{CC11}	—	1.6	—	1.6	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≤ 0.2 V Dout = High-Z
Input leakage current	I_{LI}	–5	5	–5	5	µA	0 V ≤ Vin ≤ V_{CC} + 0.3 V
Output leakage current	I_{LO}	–5	5	–5	5	µA	0 V ≤ Vout ≤ V_{CC} Dout = disable
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –2 mA
Output low voltage	V_{OL}	0	0.4	0	0.4	V	Low Iout = 2 mA

Notes : 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.

2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Measured with one sequential address change per EDO cycle, t_{HPC}.
4. V_{IH} ≥ V_{CC} – 0.2 V, 0 V ≤ V_{IL} ≤ 0.2 V.

Capacitance (Ta = 25°C, V_{CC} = 3.3 V ± 0.3 V)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	40	pF	1
Input capacitance ($\overline{RAS}$, $\overline{WE}$, $\overline{OE}$)	C_{I2}	—	48	pF	1
Input capacitance ($\overline{CAS}$)	C_{I3}	—	22	pF	1
I/O capacitance (DQ)	$C_{I/O}$	—	17	pF	1, 2

Notes : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V) *1, *2, *19

Test Conditions

- Input rise and fall time: 2 ns
- Input levels: V_{IL} = 0 V, V_{IH} = 3 V
- Input timing reference levels: 0.8 V, 2.0 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

		50 ns		60 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Random read or write cycle time	t_{RC}	84	—	104	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	30	—	40	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	8	—	10	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10000	60	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10000	10	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	ns	
Row address hold time	t_{RAH}	8	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	ns	
Column address hold time	t_{CAH}	8	—	10	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	12	37	14	45	ns	3
$\overline{RAS}$ to column address delay time	t_{RAD}	10	25	12	30	ns	4
$\overline{RAS}$ hold time	t_{RSH}	13	—	15	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	35	—	40	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	—	5	—	ns	
$\overline{OE}$ to Din delay time	t_{OED}	13	—	15	—	ns	5
$\overline{OE}$ delay time from Din	t_{DZO}	0	—	0	—	ns	6
$\overline{CAS}$ delay time from Din	t_{DZC}	0	—	0	—	ns	6
Transition time (rise and fall)	t_T	2	50	2	50	ns	7

Read Cycle

		50 ns		60 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Access time from $\overline{RAS}$	t_{RAC}	—	50	—	60	ns	8, 9
Access time from $\overline{CAS}$	t_{CAC}	—	13	—	15	ns	9, 10, 17
Access time from address	t_{AA}	—	25	—	30	ns	9, 11, 17
Access time from $\overline{OE}$	t_{OEA}	—	13	—	15	ns	9
Read command setup time	t_{RCS}	0	—	0	—	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	0	—	ns	12
Read command hold time from $\overline{RAS}$	t_{RCHR}	50	—	60	—	ns	
Read command hold time to $\overline{RAS}$	t_{RRH}	0	—	0	—	ns	12
Column address to $\overline{RAS}$ lead time	t_{RAL}	25	—	30	—	ns	
Column address to $\overline{CAS}$ lead time	t_{CAL}	15	—	18	—	ns	
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0	—	0	—	ns	
Output data hold time	t_{OH}	3	—	3	—	ns	21
Output data hold time from $\overline{OE}$	t_{OHO}	3	—	3	—	ns	
Output buffer turn-off time	t_{OFF}	—	13	—	15	ns	13, 21
Output buffer turn-off to $\overline{OE}$	t_{OEZ}	—	13	—	15	ns	13
$\overline{CAS}$ to Din delay time	t_{CDD}	13	—	15	—	ns	5
Output data hold time from $\overline{RAS}$	t_{OHR}	3	—	3	—	ns	21
Output buffer turn-off to $\overline{RAS}$	t_{OFR}	—	13	—	15	ns	13, 21
Output buffer turn-off to $\overline{WE}$	t_{WEZ}	—	13	—	15	ns	13
$\overline{WE}$ to Din delay time	t_{WED}	13	—	15	—	ns	
$\overline{RAS}$ to Din delay time	t_{RDD}	13	—	15	—	ns	

Write Cycle

		50 ns		60 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Write command setup time	t_{WCS}	0	—	0	—	ns	14
Write command hold time	t_{WCH}	8	—	10	—	ns	
Write command pulse width	t_{WP}	8	—	10	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	13	—	15	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	8	—	10	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	ns	15
Data-in hold time	t_{DH}	8	—	10	—	ns	15

Read-Modify-Write Cycle

		50 ns		60 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read-modify-write cycle time	t_{RWC}	116	—	140	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	67	—	79	—	ns	14
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	30	—	34	—	ns	14
Column address to $\overline{WE}$ delay time	t_{AWD}	42	—	49	—	ns	14
$\overline{OE}$ hold time from $\overline{WE}$	t_{OEH}	13	—	15	—	ns	

Refresh Cycle

		50 ns		60 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
$\overline{CAS}$ setup time (CBR refresh cycle)	t_{CSR}	5	—	5	—	ns	
$\overline{CAS}$ hold time (CBR refresh cycle)	t_{CHR}	8	—	10	—	ns	
$\overline{WE}$ setup time (CBR refresh cycle)	t_{WRP}	0	—	0	—	ns	
$\overline{WE}$ hold time (CBR refresh cycle)	t_{WRH}	8	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	5	—	5	—	ns	

EDO Page Mode Cycle

		50 ns		60 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
EDO page mode cycle time	t_{HPC}	20	—	25	—	ns	20
EDO page mode $\overline{RAS}$ pulse width	t_{RASP}	—	100000	—	100000	ns	16
Access time from $\overline{CAS}$ precharge	t_{CPA}	—	28	—	35	ns	9, 17
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{CPRH}	28	—	35	—	ns	
Output data hold time from $\overline{CAS}$ low	t_{DOH}	3	—	3	—	ns	9, 22
$\overline{CAS}$ hold time referred $\overline{OE}$	t_{COL}	8	—	10	—	ns	
$\overline{CAS}$ to $\overline{OE}$ setup time	t_{COP}	5	—	5	—	ns	
Read command hold time from $\overline{CAS}$ precharge	t_{RCHC}	28	—	35	—	ns	
Write pulse width during $\overline{CAS}$ precharge	t_{WPE}	8	—	10	—	ns	
$\overline{OE}$ precharge time	t_{OEP}	8	—	10	—	ns	

EDO Page Mode Read-Modify-Write Cycle

		50 ns		60 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
EDO page mode read- modify-write cycle time	t_{HPRWC}	57	—	68	—	ns	
$\overline{WE}$ delay time from $\overline{CAS}$ precharge	t_{CPW}	45	—	54	—	ns	14

Refresh

Parameter	**Symbol**	**Max**	**Unit**	**Notes**
Refresh period	t_{REF}	64	ms	4096 cycles
Refresh period (L-version)	t_{REF}	128	ms	4096 cycles

Self Refresh Mode (L-version)

		50 ns		60 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
$\overline{RAS}$ pulse width (self refresh)	t_{RASS}	100	—	100	—	µs	26
$\overline{RAS}$ precharge time (self refresh)	t_{RPS}	90	—	110	—	ns	26
$\overline{CAS}$ hold time (self refresh)	t_{CHS}	–50	—	–50	—	ns	

Notes: 1. AC measurements assume t_T = 2 ns.

2. An initial pause of 200 µs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$-only refresh or $\overline{CAS}$-before-$\overline{RAS}$ refresh).
3. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, than the access time is controlled exclusively by t_{CAC}.
4. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
5. Either t_{OED} or t_{CDD} must be satisfied.
6. Either t_{DZO} or t_{DZC} must be satisfied.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
9. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
10. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\geq t_{RAD} + t_{AA}$ (max).
11. Assumes that $t_{RAD} \geq t_{RAD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\leq t_{RAD} + t_{AA}$ (max).
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
13. t_{OFF} (max), t_{OEZ} (max), t_{WEZ} (max) and t_{OFR} (max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

14. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), or $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. t_{DS} and t_{DH} are referred to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{RASP} defines $\overline{RAS}$ pulse width in EDO page mode cycles.
17. Access time is determined by the longest among t_{AA}, t_{CAC} and t_{CPA}.
18. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
19. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large V_{CC}/V_{SS} line noise, which causes to degrade V_{IH} min/V_{IL} max level.
20. t_{HPC} (min) can be achieved during a series of EDO page mode write cycles or EDO page mode read cycles. If both write and read operation are mixed in a EDO page mode $\overline{RAS}$ cycle (EDO page mode mix cycle (1), (2)), minimum value of $\overline{CAS}$ cycle ($t_{CAS} + t_{CP} + 2\ t_T$) becomes greater than the specified t_{HPC} (min) value. The value of $\overline{CAS}$ cycle time of mixed EDO page mode is shown in EDO page mode mix cycle (1) and (2).
21. Data output turns off and becomes high impedance from later rising edge of $\overline{RAS}$ and $\overline{CAS}$. Hold time and turn off time are specified by the timing specifications of later rising edge of $\overline{RAS}$ and $\overline{CAS}$ between t_{OHR} and t_{OH} and between t_{OFR} and t_{OFF}.
22. t_{DOH} defines the time at which the output level go cross. V_{OL} = 0.8 V, V_{OH} = 2.0 V of output timing reference level.
23. Before and after self refresh mode, execute CBR refresh to all refresh addresses in or within 64 ms period on the condition a and b below.
    a. Enter self refresh mode within 15.6 μs after either burst refresh or distributed refresh at equal interval to all refresh addresses are completed.
    b. Start burst refresh or distributed refresh at equal interval to all refresh addresses within 15.6μs after exiting from self refresh mode.
24. In case of entering from $\overline{RAS}$-only-refresh, it is necessary to execute CBR refresh before and after self refresh mode according as note 23.
25. For L-version, it is available to apply each 128 ms and 31.2 μs instead of 64 ms and 15.6 μs at note 23.
26 At t_{RASS} > 100 μs, self refresh mode is activated, and not activated at t_{RASS} < 10 μs. It is undefined within the range of 10 μs ≤ t_{RASS} ≤ 100 μs. For $t_{RASS} \geq$ 10 μs, it is necessary to satisfy t_{RPS}.
27. XXX: H or L (H: V_{IH} (min) ≤ $V_{IN} \leq V_{IH}$ (max), L: V_{IL} (min) ≤ $V_{IN} \leq V_{IL}$ (max))

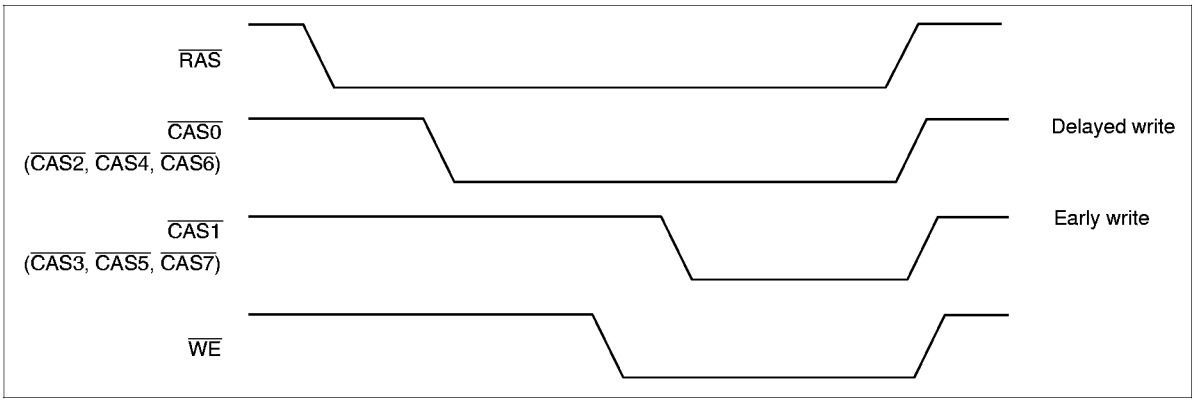
    ///////: Invalid Dout

    When the address, clock and input pins are not described on timing waveforms, their pins must be applied V_{IH} or V_{IL}.

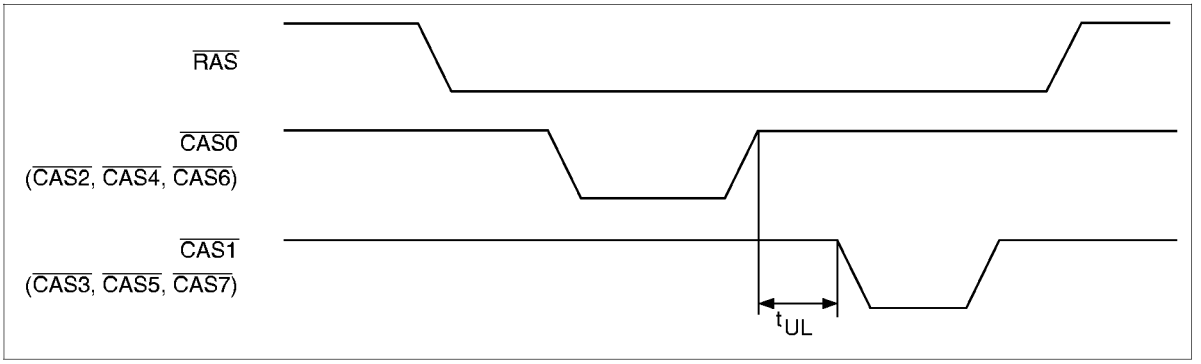
Notes concerning 2$\overline{CAS}$ control

Please do not separate the 2$\overline{CAS}$s ($\overline{CAS}$0 and $\overline{CAS}$1 (or $\overline{CAS}$2, $\overline{CAS}$4, $\overline{CAS}$6 and $\overline{CAS}$3, $\overline{CAS}$5, $\overline{CAS}$7)) operation timing intentionally. However skew between 2$\overline{CAS}$s are allowed under the following conditions.

1. Each of the 2CASs should satisfy the timing specifications individually.
2. Different operation mode for upper/lower byte is not allowed: such as following.



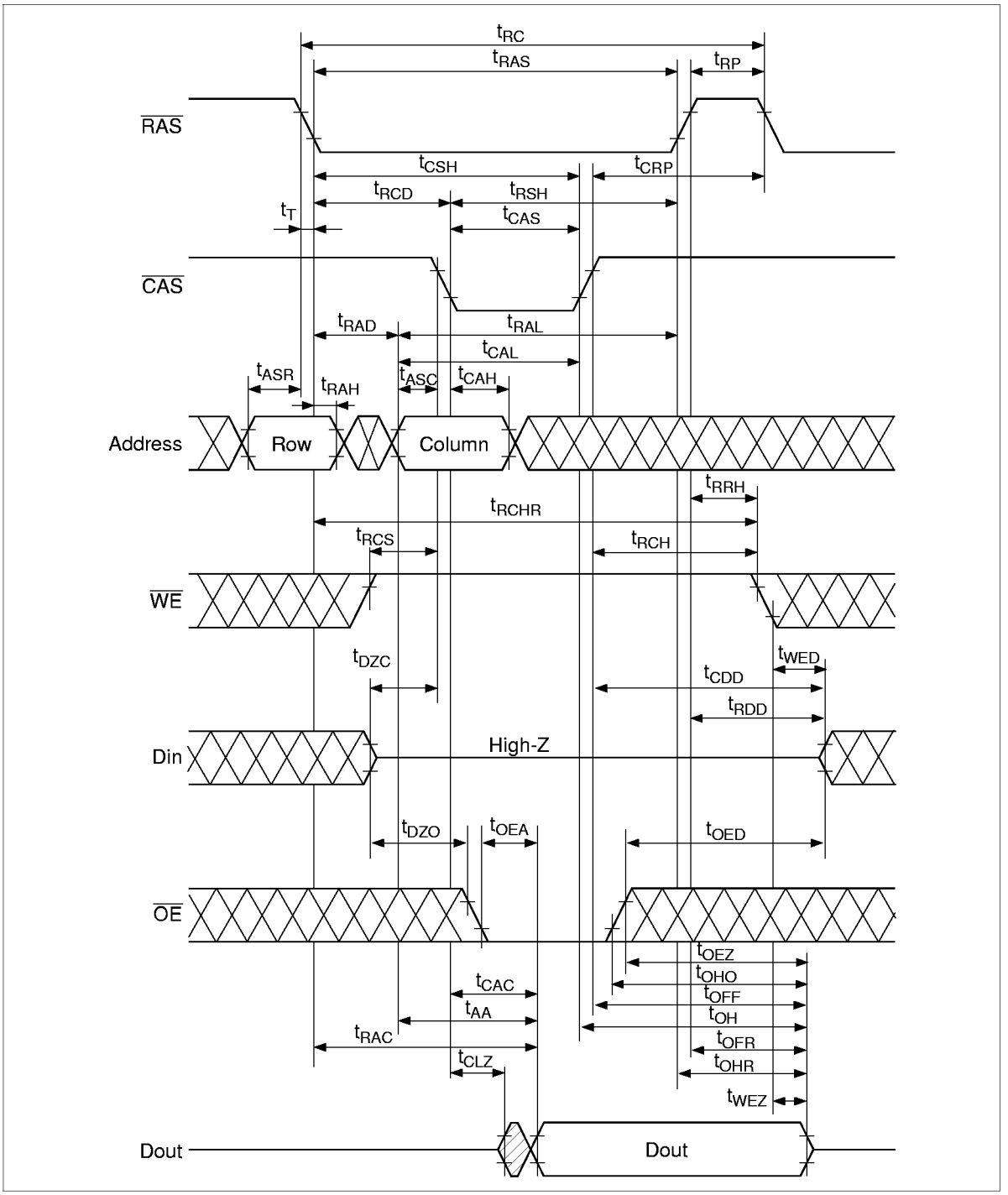
3. Closely separated upper/lower byte control is not allowed. However when the condition ($t_{CP} \leq t_{UL}$) is satisfied, EDO page mode can be performed.



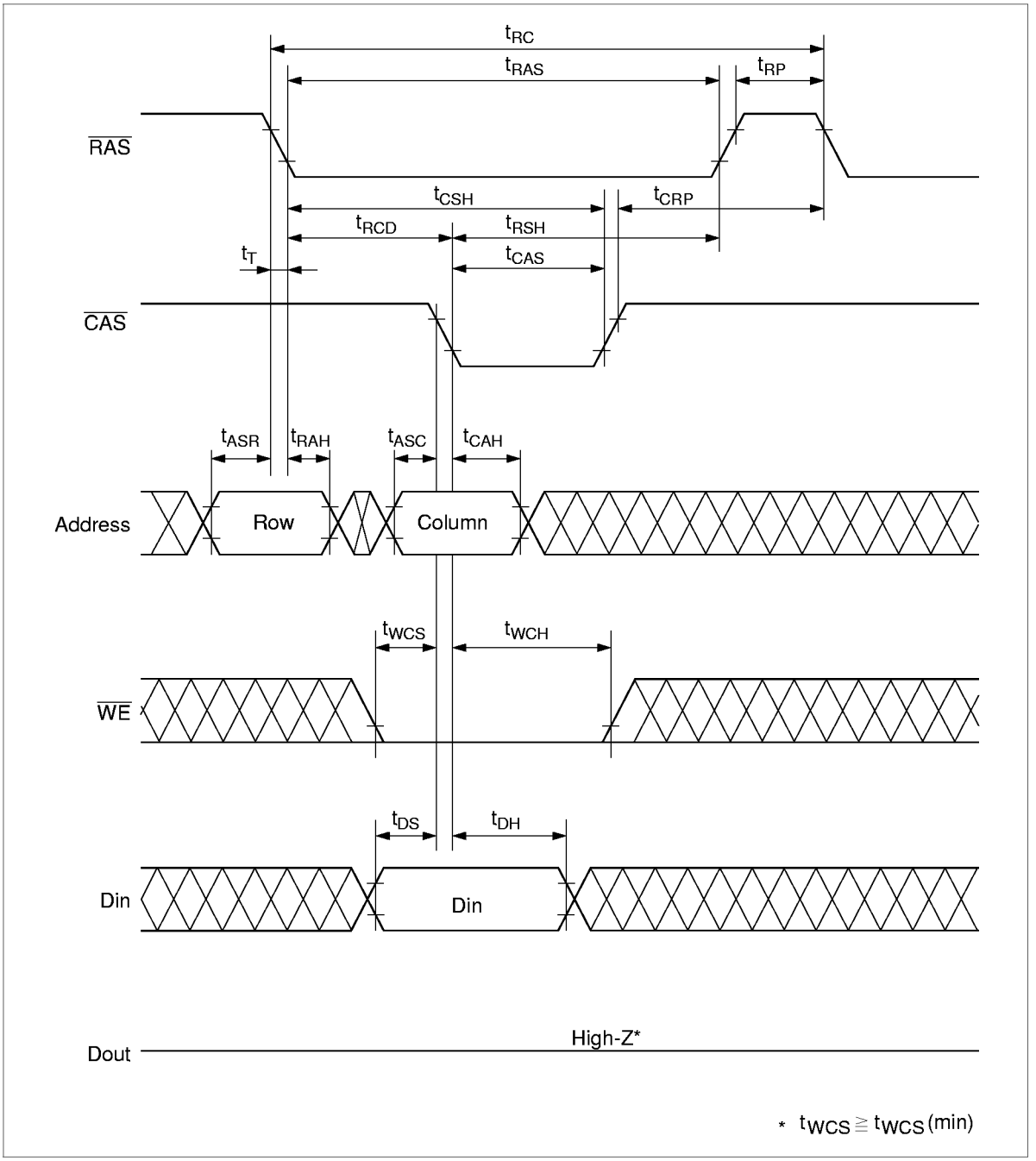
4. Byte control operation by remaining $\overline{CAS}$0 ($\overline{CAS}$2, $\overline{CAS}$4, $\overline{CAS}$6) or $\overline{CAS}$1 ($\overline{CAS}$3, $\overline{CAS}$5, $\overline{CAS}$7) high is guaranteed.

Timing Waveforms*[27]

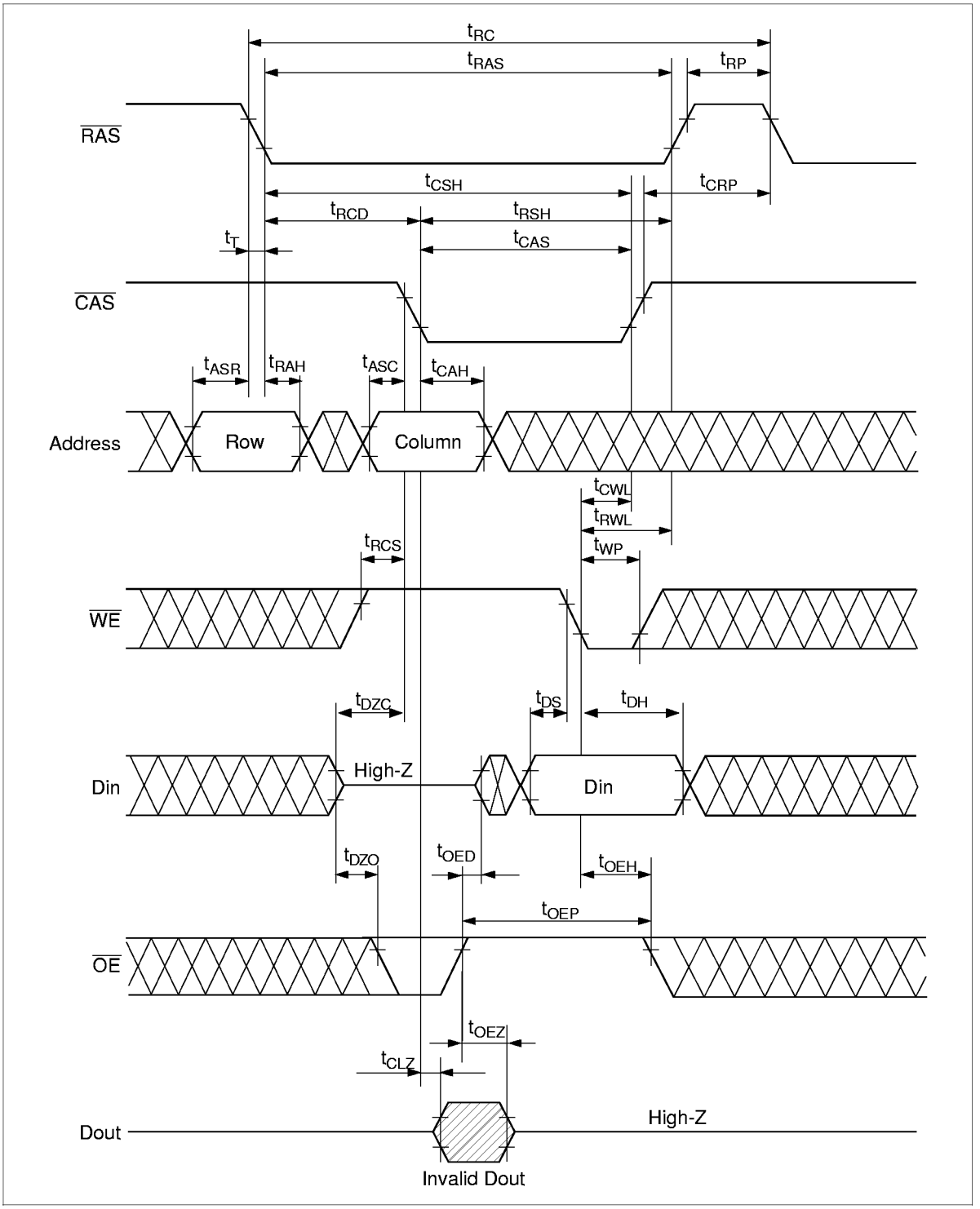
Read Cycle



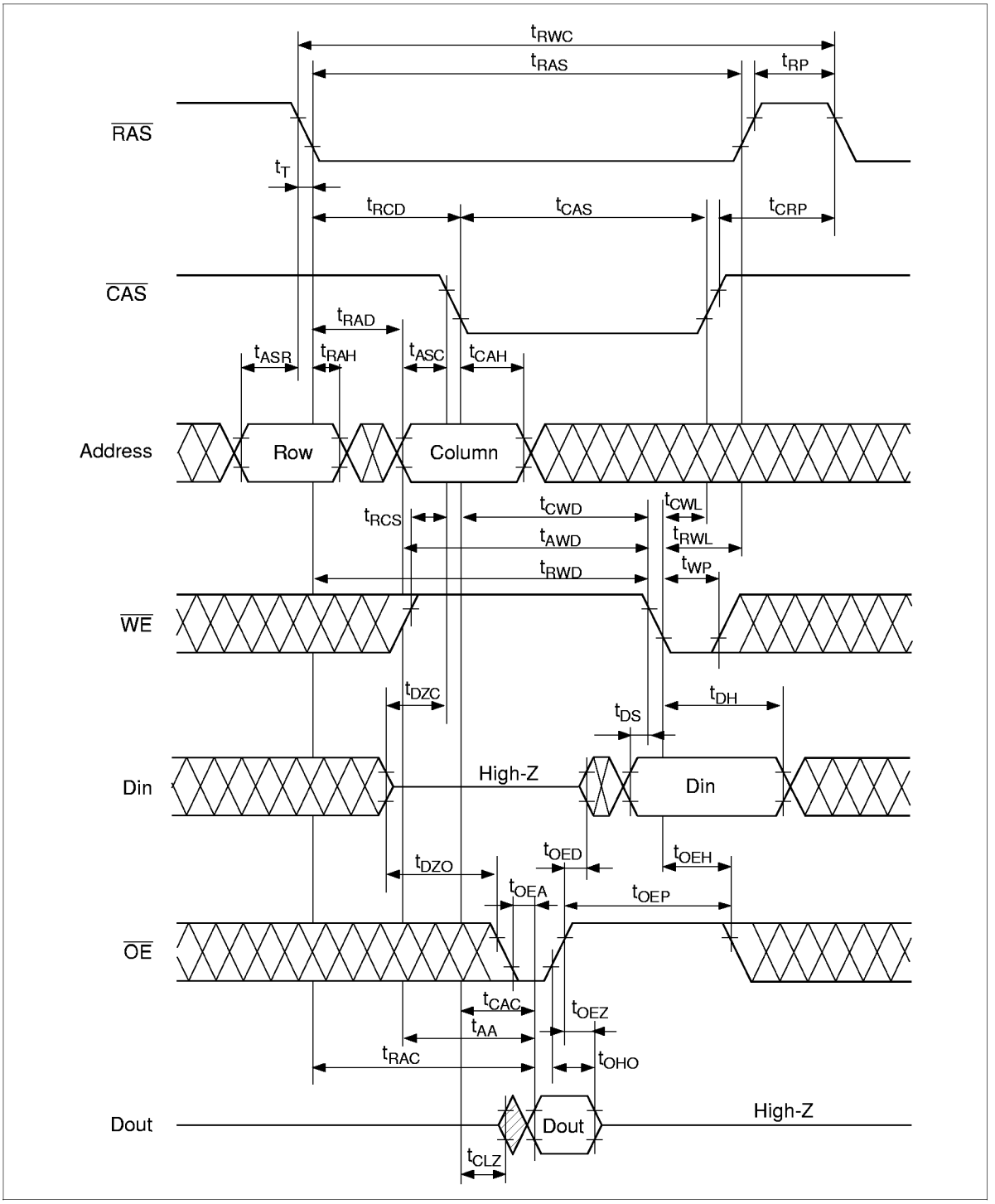
Early Write Cycle



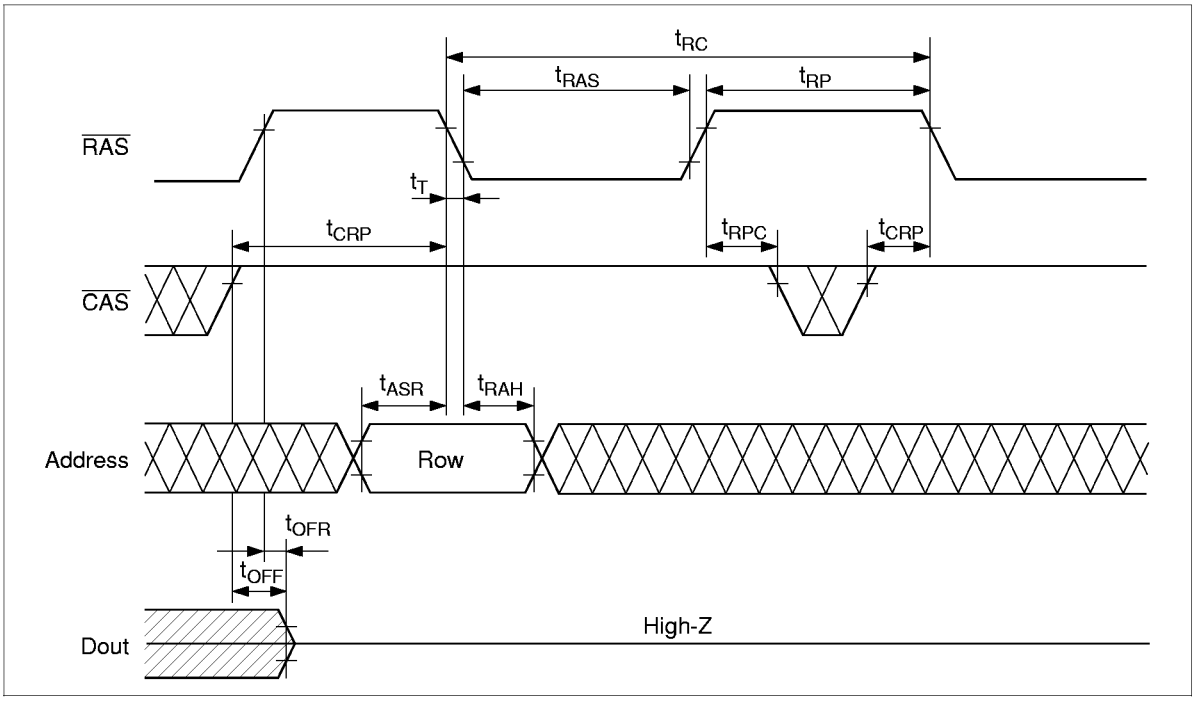
Delayed Write Cycle*[18]



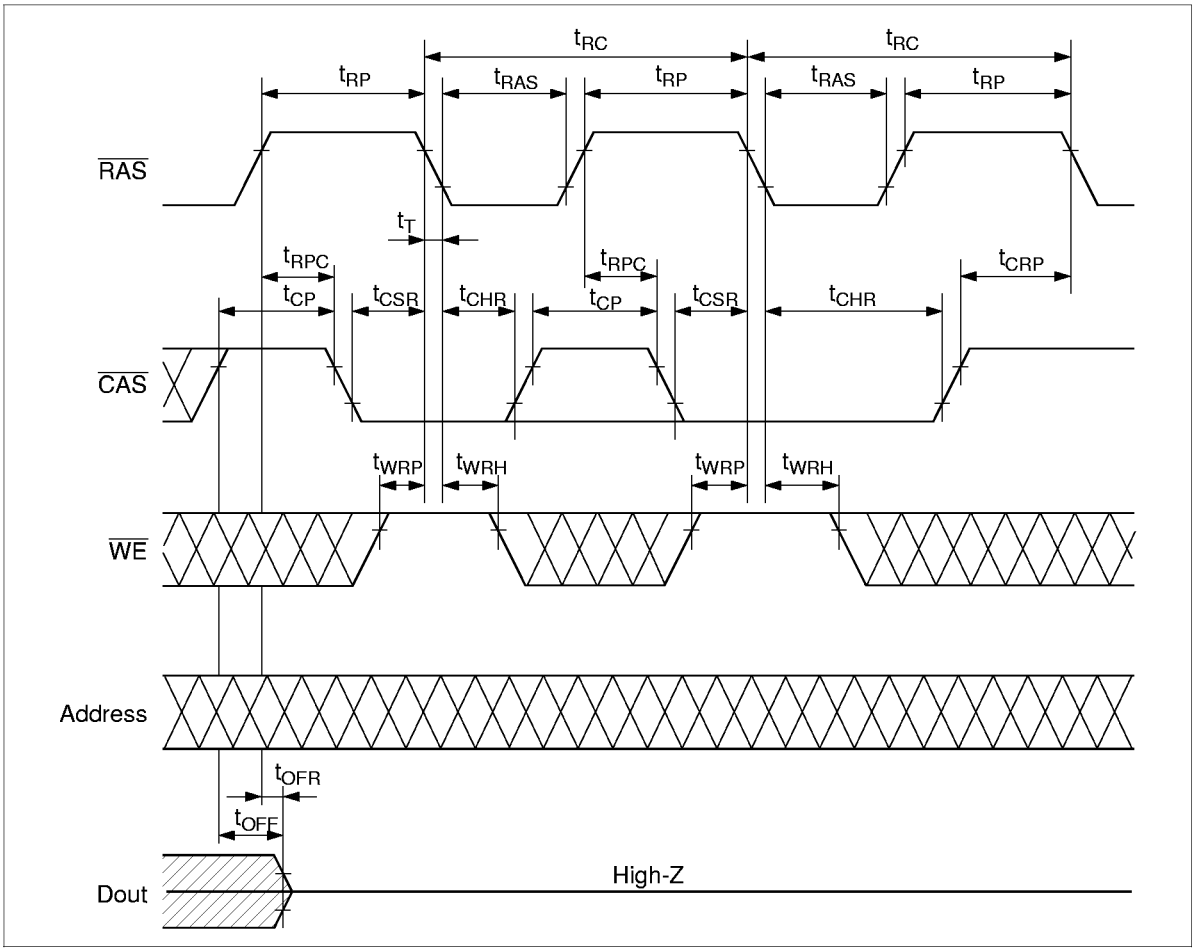
Read-Modify-Write Cycle[*18]



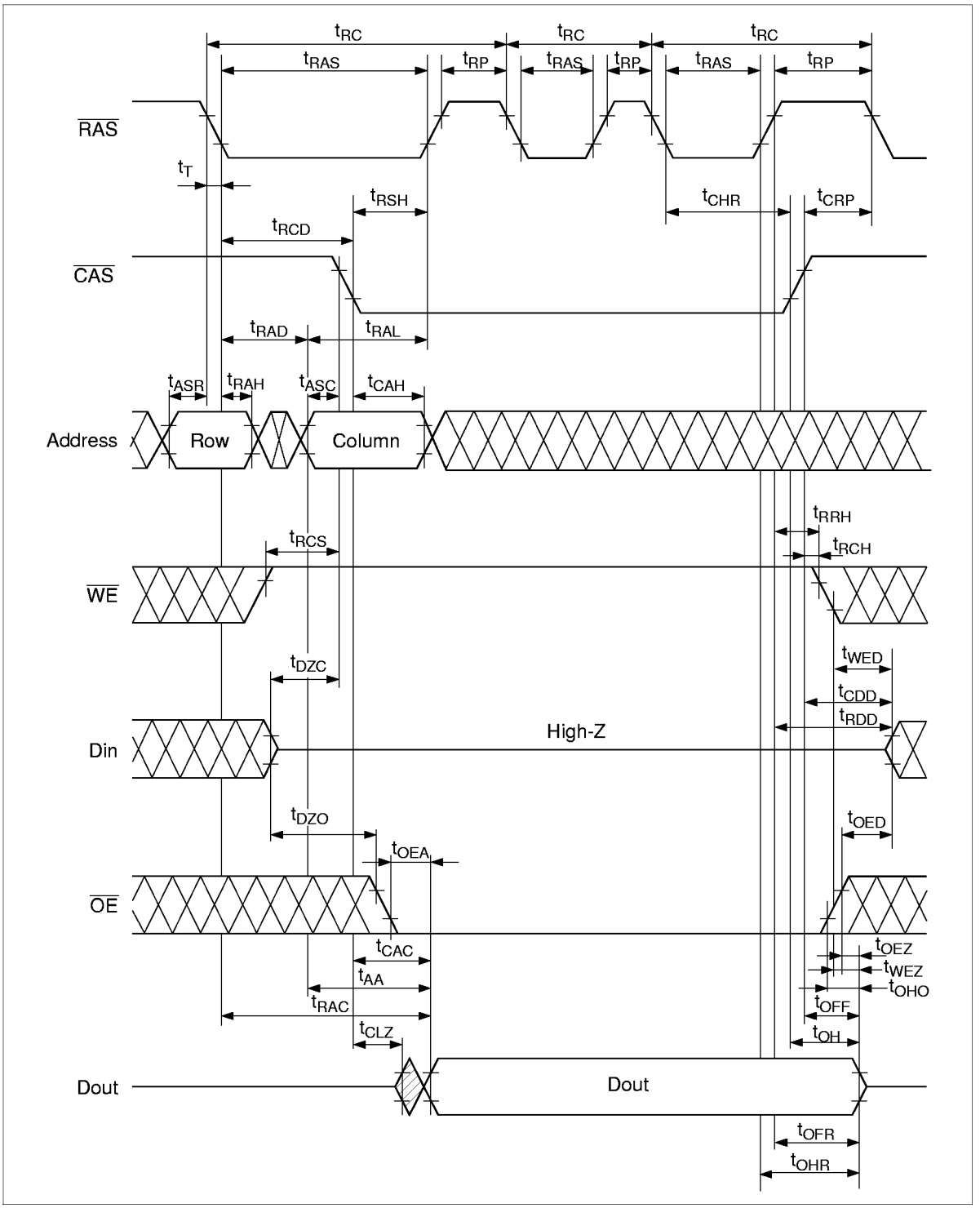
$\overline{\text{RAS}}$-Only Refresh Cycle



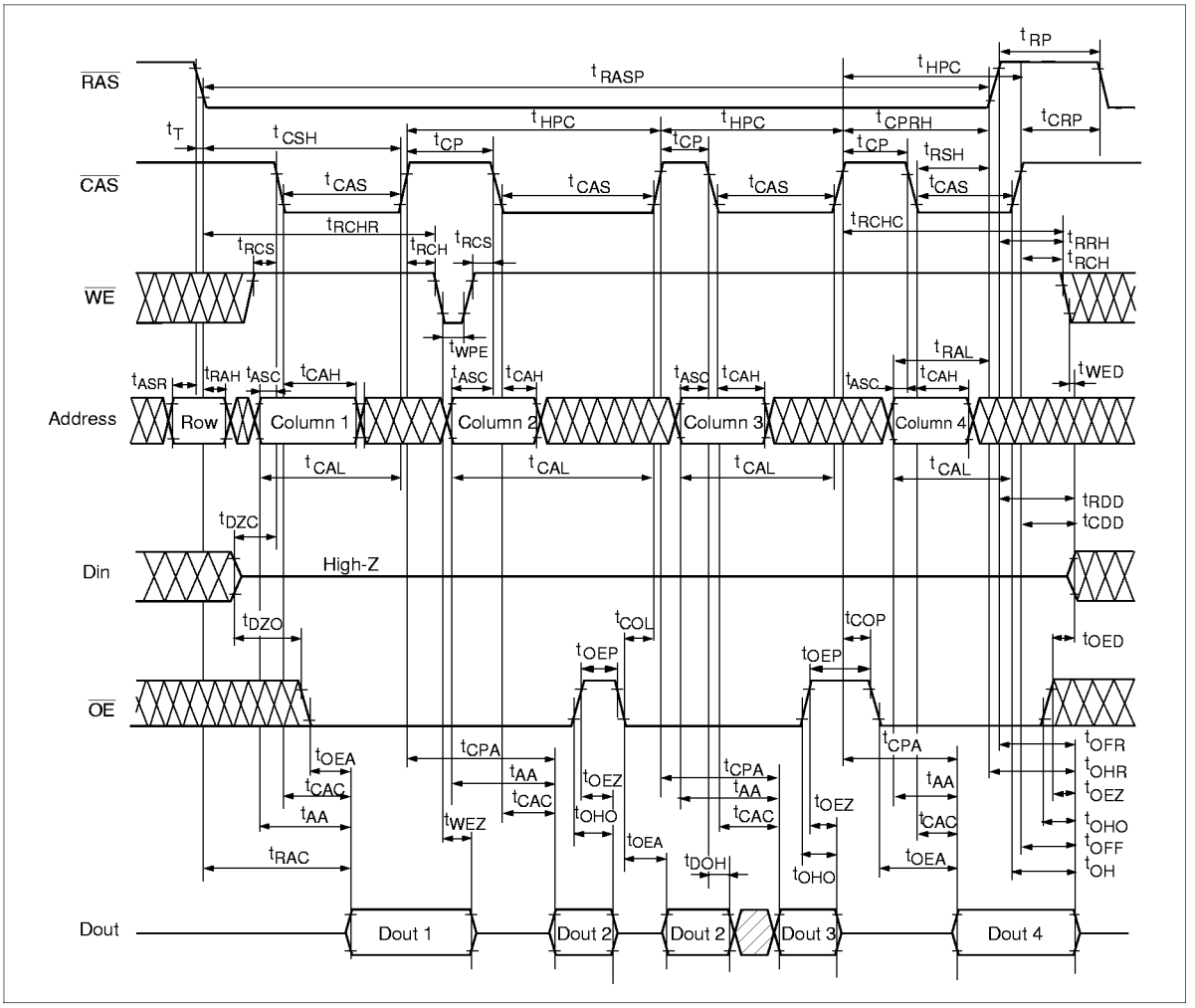
$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle



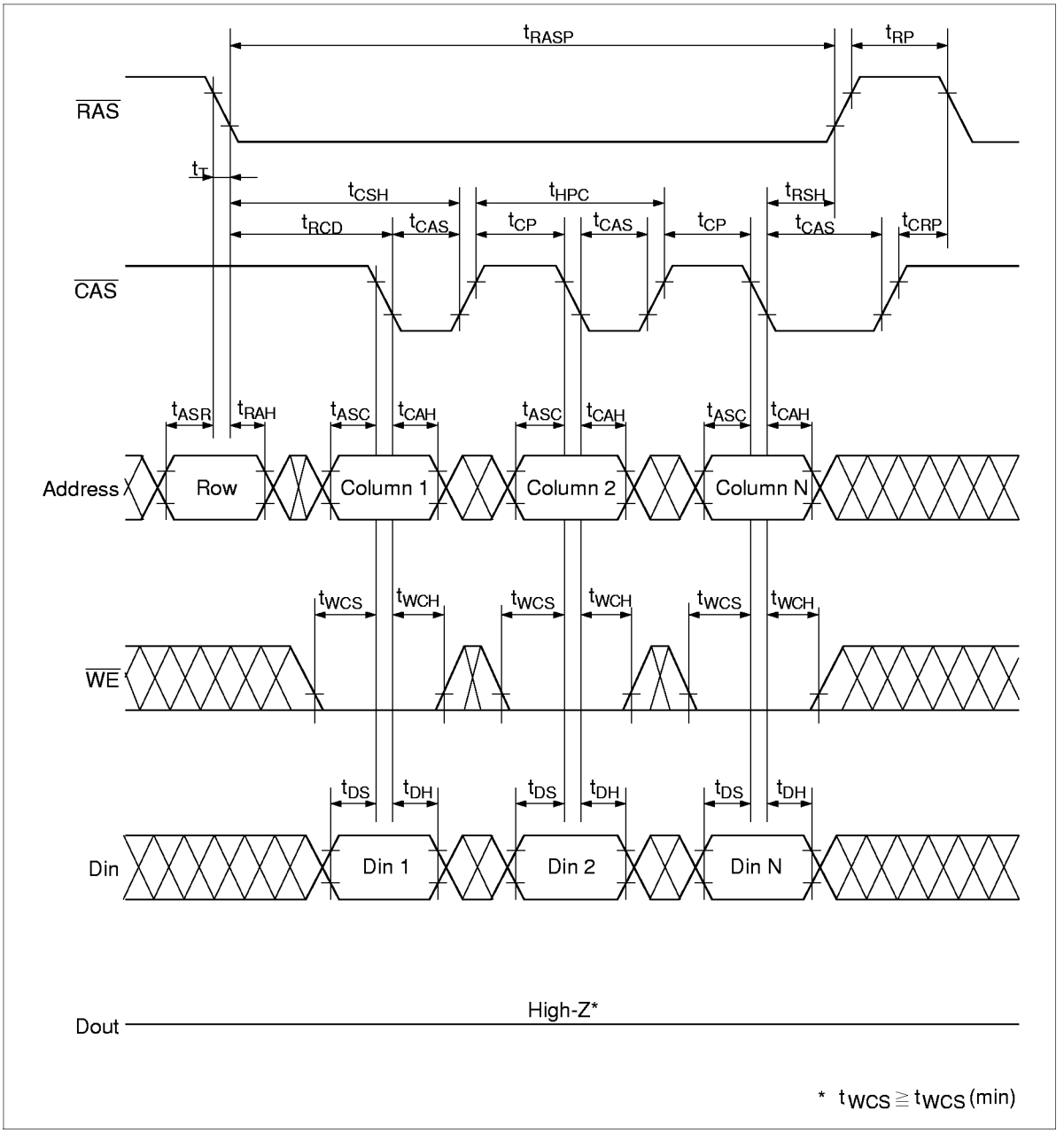
Hidden Refresh



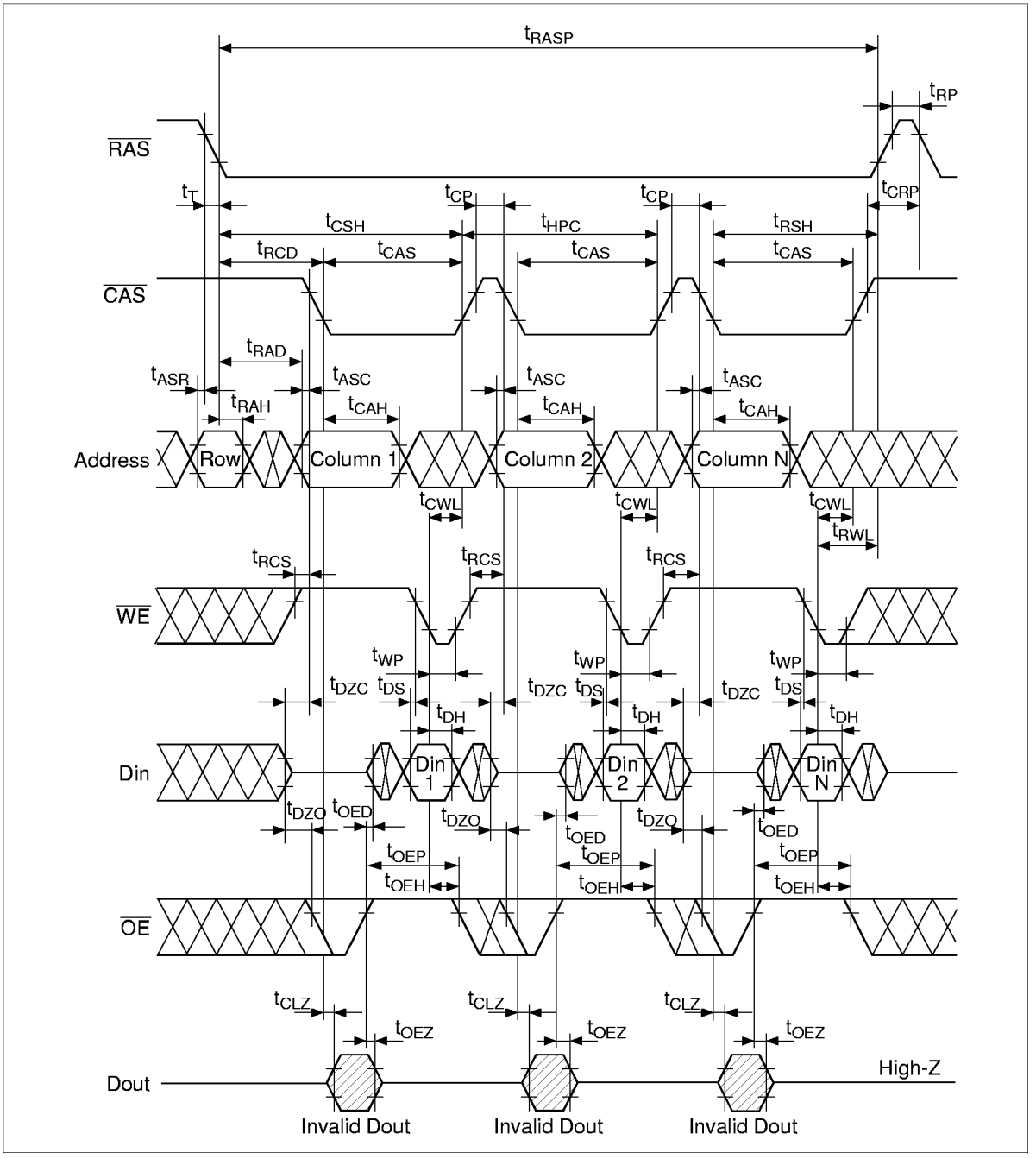
EDO Page Mode Read Cycle



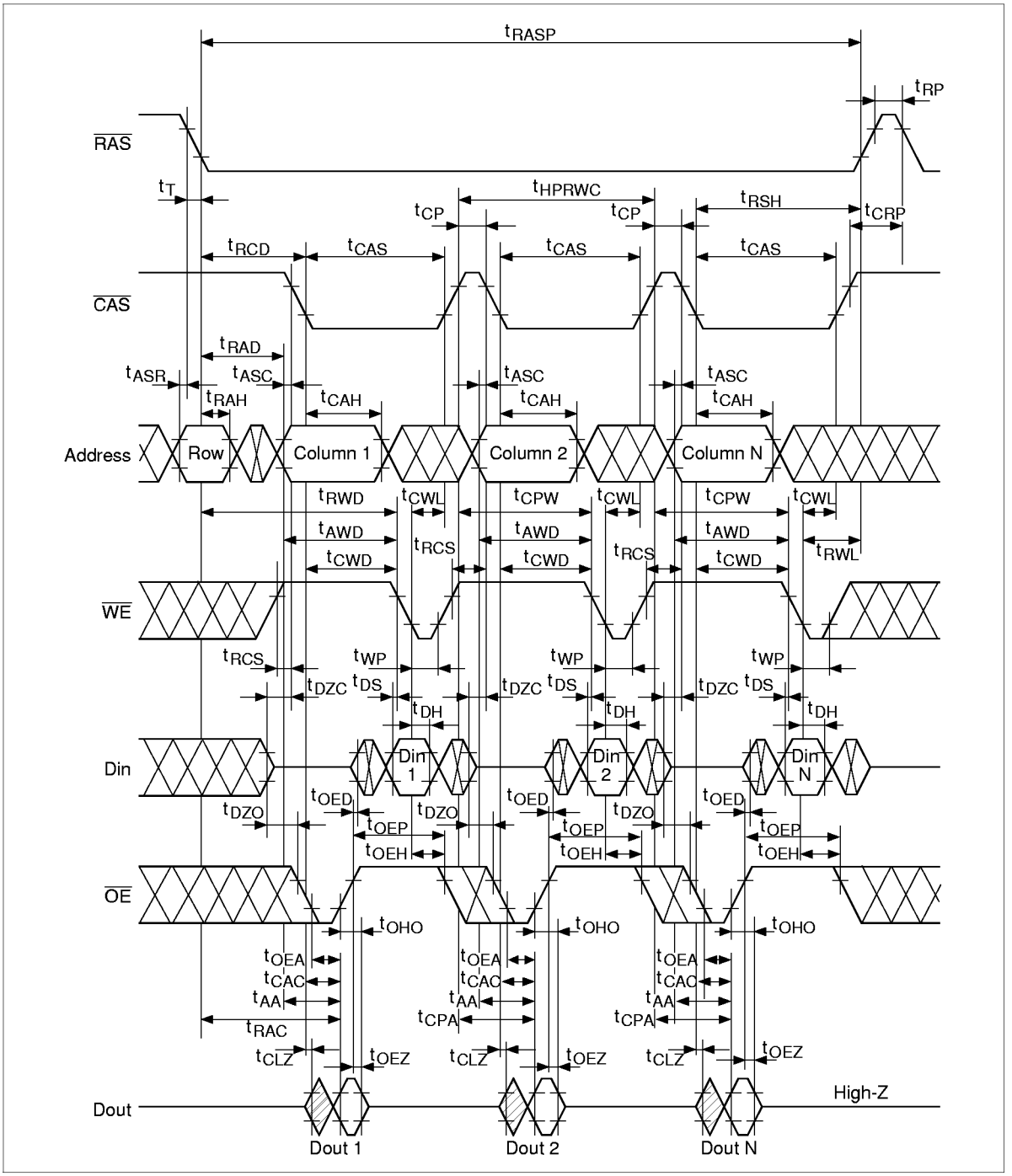
EDO Page Mode Early Write Cycle



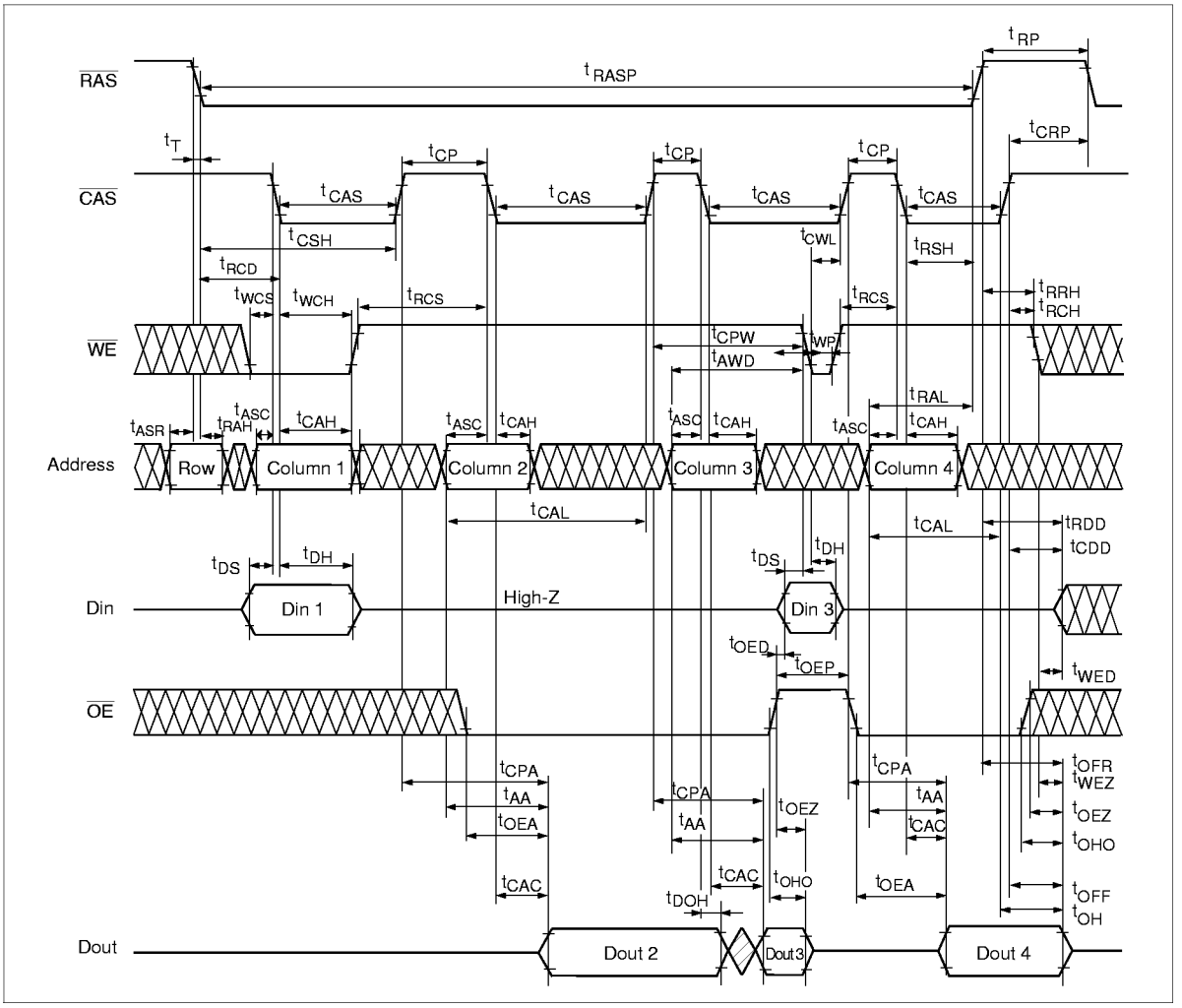
EDO Page Mode Delayed Write Cycle[*18]



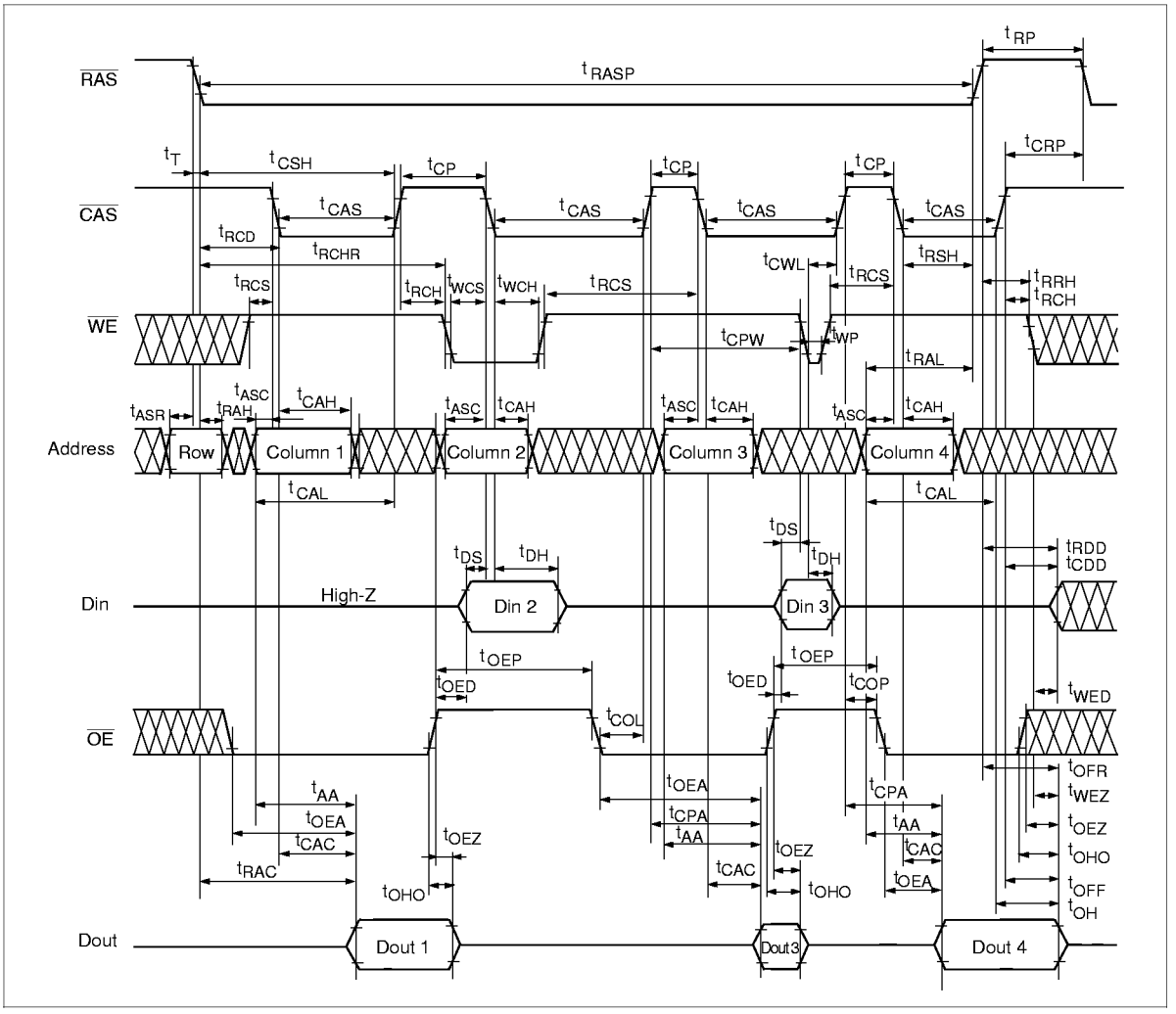
EDO Page Mode Read-Modify-Write Cycle[*18]



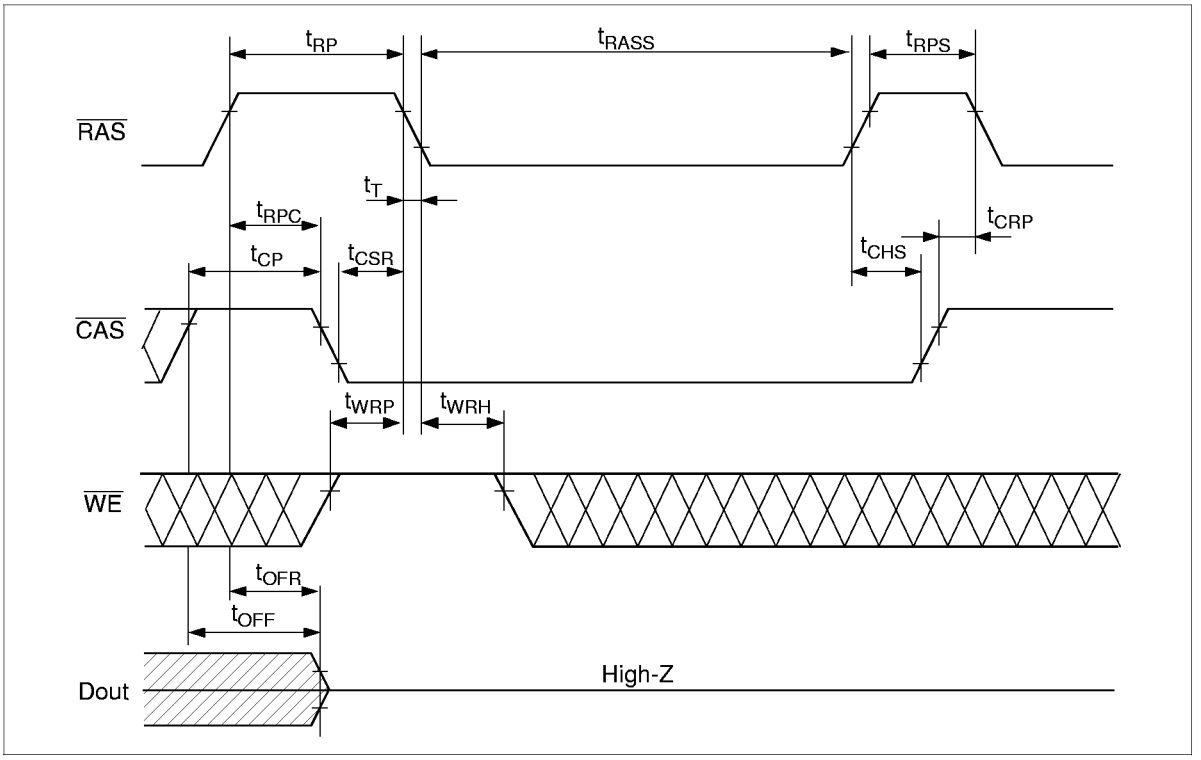
EDO Page Mode Mix Cycle (1)*[20]



EDO Page Mode Mix Cycle (2) *20

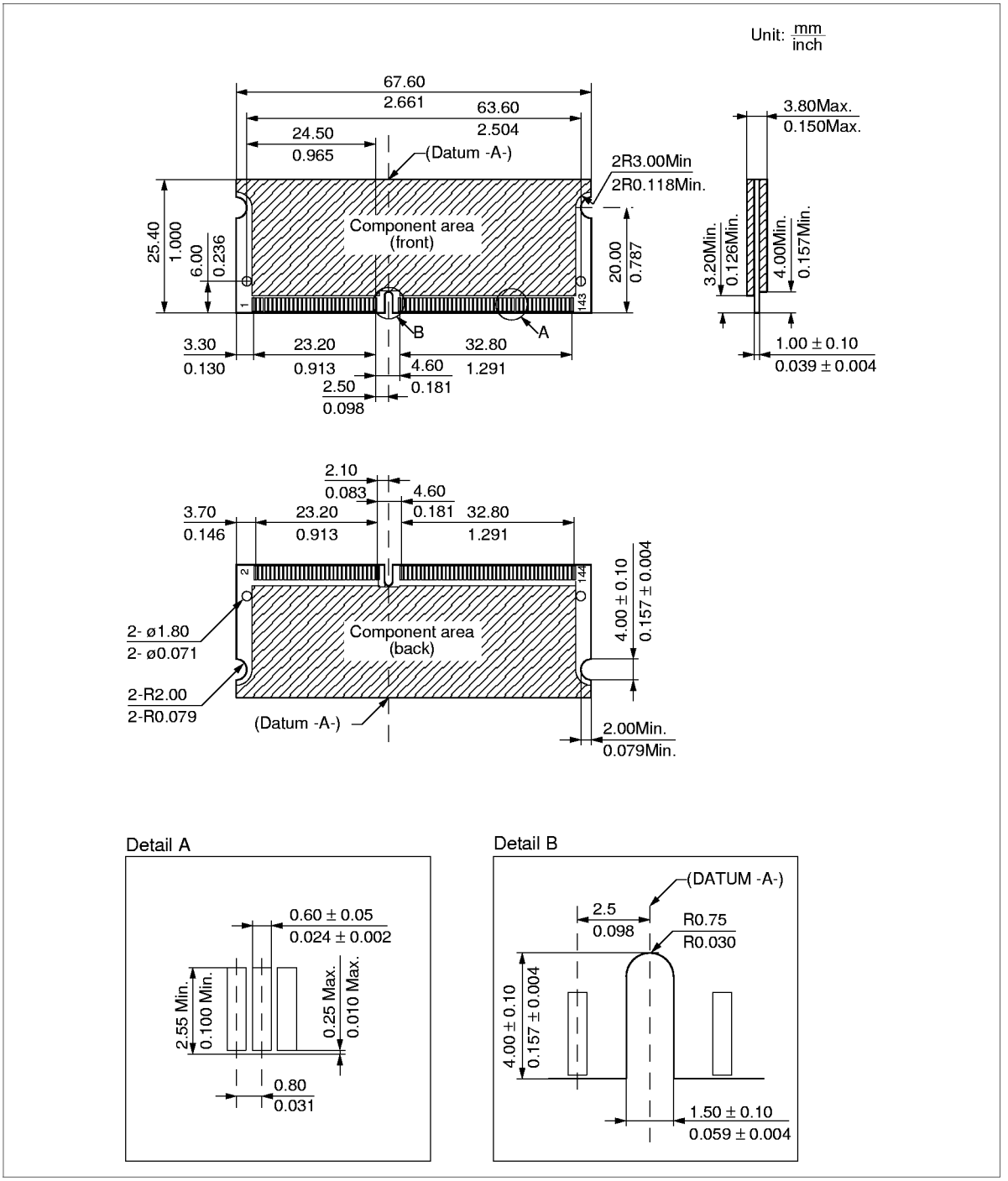


Self Refresh Mode Cycle(L-version)* [23, 24, 25, 26]



Physical Outline

HB56HW465DB Series



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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Nov. 10, 1997	Initial issue (referred to HM5164165/HM5165165 Series Rev. 0.1)	Y.Saitou	K.Tsuneda
1.0	May. 15, 1998	Deletion of Preliminary (referred to HM5164165/HM5165165 Series Rev. 0.1) Block Diagram correct errors Refresh Cycle t_{WRH} min: 10/10 ns to 8/10 ns Serial PD correct errors: No.85		