DATA SHEET

TEA1065
Versatile telephone transmission circuit with dialler interface

Product specification
File under Integrated Circuits, IC03A

March 1994

Philips
Semiconductors

PHILIPS

FEATURES

- Current and voltage regulator mode with adjustable static resistances
- Provides supply for external circuitry
- Symmetrical high-impedance inputs for piezoelectric microphone
- Asymmetrical high-impedance input for electret microphone
- DTMF signal input with confidence tone
- Mute input for pulse or DTMF dialling
- Power-down input for pulse dial or register recall
- Digital pulse input to drive an external switch transistor
- Receiving amplifier for magnetic, dynamic or piezoelectric earpieces
- Large gain setting range on microphone and earpiece amplifiers
- Line loss compensation facility, line current dependent (on microphone and earpiece amplifiers)
- Adjustable gain control
- DC line voltage adjustment facility

GENERAL DESCRIPTION

The TEA1065 is a bipolar integrated circuit which performs all speech and line interface functions that are required in fully electronic telephone sets with adjustable DC mask. The circuit performs electronic switching between dialling and speech internally.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA1065	24	DIL	plastic	SOT101L
TEA1065T	24	SO24	plastic	SOT137A

Notes

1. SOT101-1; 1998 Jun 18.
2. SOT137-1; 1998 Jun 18.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{LN}	line voltage	I_{line} = 15 mA	4.25	4.45	4.65	V
I_{line}	normal operation line current range		10	–	150	mA
I_{CC}	internal supply consumption					
	power-down input LOW		–	1.14	1.5	mA
	power-down input HIGH		–	73	105	μA
V_{CC}	supply voltage for peripherals	I_{line} = 15 mA; MUTE input HIGH				
		I_P = 1.2 mA	2.7	–	–	V
		I_P = 1.55 mA	2.5	–	–	V
G_V	voltage gain range					
	microphone amplifier		30	–	46	dB
	earpiece amplifier		20	–	45	dB
ΔG_V	line loss compensation					
	gain control range		–5.5	–5.9	–6.3	dB
T_{amb}	operating ambient temperature range		–25	–	+75	°C

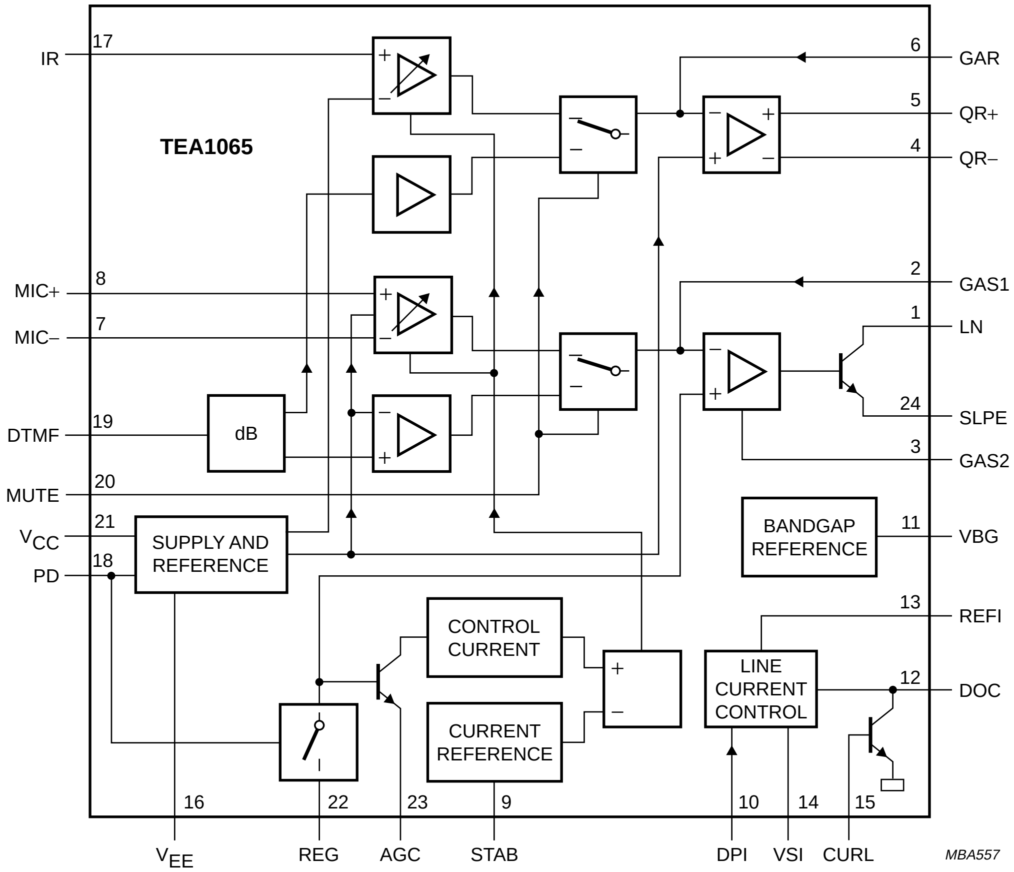


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
LN	1	positive line terminal
GAS1	2	gain adjustment; sending amplifier
GAS2	3	gain adjustment; sending amplifier
QR–	4	inverting output; receiving amplifier
QR+	5	non-inverting output; receiving amplifier
GAR	6	gain adjustment; receiving amplifier
MIC–	7	inverting microphone input
MIC+	8	non-inverting microphone input
STAB	9	current stabilizer
DPI	10	digital pulse input
VBG	11	bandgap output reference
DOC	12	drive current output
REFI	13	reference voltage input
VSI	14	voltage sense input
CURL	15	current limitation input
V_{EE}	16	negative line terminal
IR	17	receiving amplifier input
PD	18	power-down input
DTMF	19	dual-tone multifrequency input
MUTE	20	MUTE input
V_{CC}	21	positive supply decoupling
REG	22	voltage regulator decoupling
AGC	23	automatic gain control input
SLPE	24	slope (DC resistance) adjustment

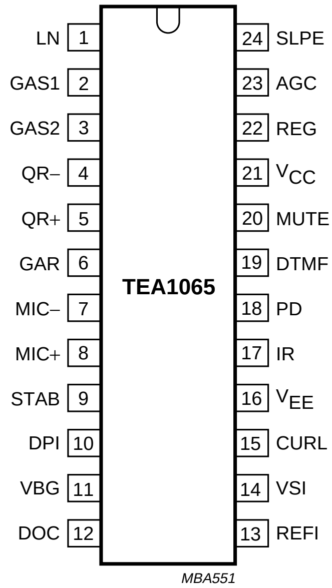


Fig.2 Pinning diagram.

FUNCTIONAL DESCRIPTION

Supply: V_{CC}, LN, SLPE, REG and STAB

The circuit and its peripherals are usually supplied from the telephone line. The circuit develops its own supply voltage at V_{CC} (pin 21) and regulates its voltage drop between LN and SLPE (pins 1 and 24). The internal supply requires a decoupling capacitor between V_{CC} and V_{EE} (pin 16); the internal voltage regulator has to be decoupled by a capacitor from REG (pin 22) to V_{EE}. The internal current stabilizer is set by a 3.6 kΩ resistor connected between STAB (pin 9) and V_{EE}.
The TEA1065 can be set either in a DC voltage regulator mode or in a DC current regulator mode. The DC mask can be selected by connecting the appropriate external components to the dedicated pins (VSI, REFI, DOC, VBG).
When the DC current regulator mode is not required it can be cancelled by connecting pin VSI to V_{EE}; pins REFI, VBG and DOC are left open-circuit.

Voltage regulator mode

The voltage regulator mode is achieved when the line current is less than the current I_{knee} as illustrated in Fig.3. With R13 = R14 = 30 kΩ, the current I_{knee} = 30 mA (I_p = 0 mA).

This line current value will be reached when the voltage on pin VSI (almost equal to the voltage on pin SLPE) exceeds the voltage on pin REFI (equal to the voltage on pin VBG divided by the resistor tap R13, R14). For other values of R13 and R14, the I_{knee} current is given by the following formula:

$$I_{knee} = I_{CC} + I_P + (VBG/R9) \times \{R14/(R14 + R13)\} - (R15/R9) \times I_O(VSI)$$

I_{CC} is the current required by the circuit itself (typ. 1.14 mA). I_P is the current required by the peripheral circuits connected between V_{CC} and V_{EE}. $I_{O(VSI)}$ is the output current from pin VSI (typ. 2.5 µA).

The DC slope of the V_{line}/I_{line} curve is, in this mode, determined by R9 (R9 = R9a + R9b) in series with the r_{ds} of the external line current control transistor (see Fig.4; $r_{ds} = \partial V_{GS}/\partial I_D$ at $V_{GS} = V_{DS}$).

Current regulator mode

The current regulator mode is achieved when the line current is greater than I_{knee}. In this mode, the slope of the V_{line}/I_{line} curve is approximately 1300 Ω with R9 = 20 Ω, R16 = 1 MΩ, R13 = R14 = 30 kΩ. For other values of these resistances, the slope value can be approximated by the following formula:

$$R9 \times \{1 + R16 \times (1/R13 + 1/R14)\}$$

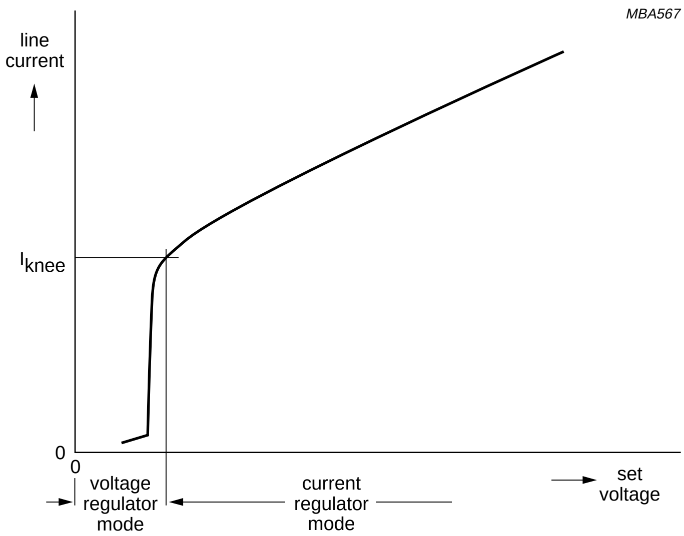


Fig.3 Voltage and current regulator mode.

The DC current flowing into the set is determined by the exchange supply voltage (V_{exch}), the DC resistance of the subscriber line (R_{line}) and the DC voltage on the subscriber set (see Fig.4).
If the line current exceeds I_{CC} + 0.3 mA, required by the circuit itself ($I_{CC} \approx 1.14$ mA), plus the current I_p required by the peripheral circuits connected to V_{CC} then the voltage regulator will divert the excess current via LN.

$$V_{LN} = V_{ref} + I_{SLPE} \times R9 = V_{ref} + (I_{line} - I_{CC} - 0.3 \times 10^{-3} - I_p) \times R9$$

where: V_{ref} is an internally generated temperature compensated reference voltage of 4.18 V and R9 is an external resistor connected between SLPE and V_{EE}.

The preferred value of R9 is 20 Ω. Changing R9 will influence the microphone gain, gain control characteristics, sidetone and the maximum output swing on LN. In this instance, the voltage on the line (excluding the diode rectifier bridge; see Fig.4) is:

$$V_{line} = V_{LN} + V_{GS} + R16 \times I_{DOC}$$

where: V_{GS} is the voltage drop between the gate and source terminal of the external line current control transistor and I_{DOC} is the current sunk by pin DOC (I_{DOC} = 0 in the voltage regulator mode and increases with I_{line} in the current regulator mode).
Under normal conditions $I_{SLPE} >> I_{CC} + 0.3\text{ mA} + I_p$ and for the voltage regulator mode ($I_{line} < I_{knee}$), the static behaviour of the circuit is equal to a 4.18 V voltage regulator diode with an internal resistance of R9 in series with the V_{GSon} of the external line current control transistor. For the current regulator mode ($I_{line} > I_{knee}$), the static behaviour of the circuit is equal to a 4.18 V voltage regulator diode with an internal resistance of R9 in series with the V_{GSon} of the external line current control transistor and also in series with a DC voltage source R16 × I_{DOC} (the preferred value of R16 is 1 MΩ at this value the current I_{DOC} is negligible compared to I_{line}).

In the audio frequency range the dynamic impedance between LN and V_{EE} is equal to R1 (see Fig.8). The internal reference voltage V_{ref} can be adjusted by means of an external resistor R_{VA}. This resistor, connected between LN and REG, will decrease the internal reference voltage. When R_{VA} is connected between REG and SLPE the internal reference voltage will increase.
The maximum allowed line current is given in Figs 5 and 6, where the current is shown as a function of the required reference voltage, ambient temperature and applied package.

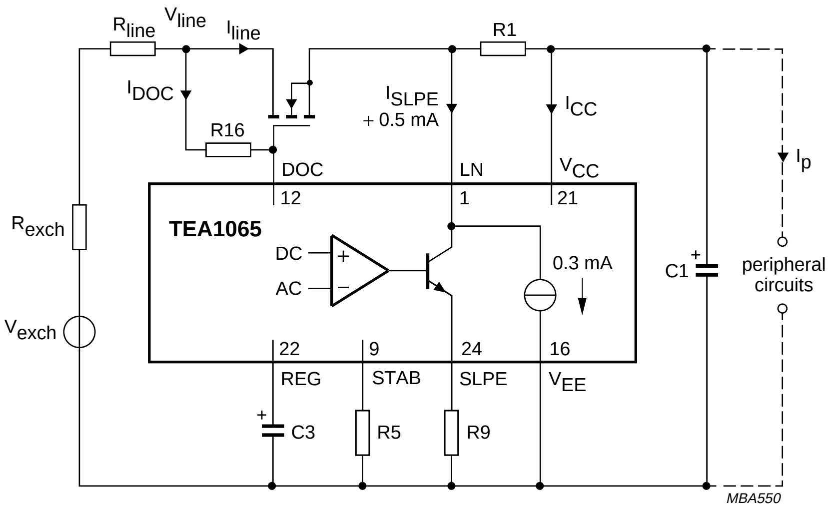
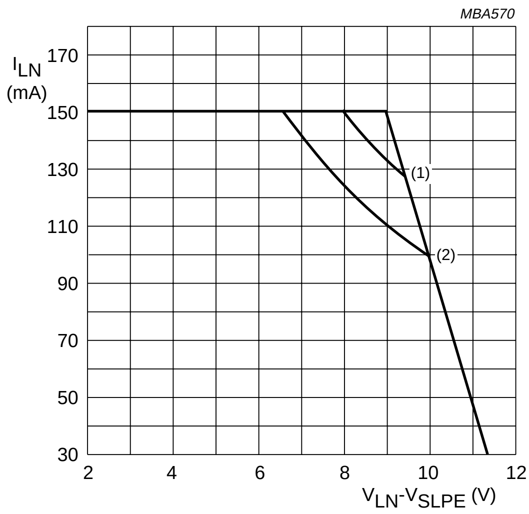


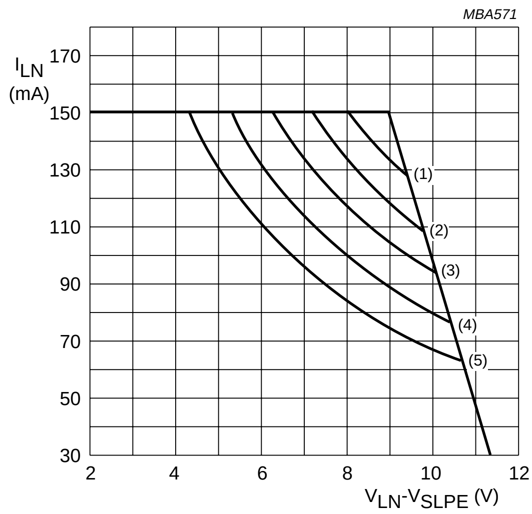
Fig.4 Supply arrangement.

The current I_p, available from V_{CC} for supplying peripheral circuits, depends on the external components and on the line current. Fig.7 shows this current for $V_{CC} > 2.2$ V and for $V_{CC} > 3$ V, where 3 V is the minimum supply voltage for most CMOS circuits including a diode voltage drop for a back-up diode. If MUTE is LOW the available current is further reduced when the receiving amplifier is driven (earpiece amplifier supplied from V_{CC}).



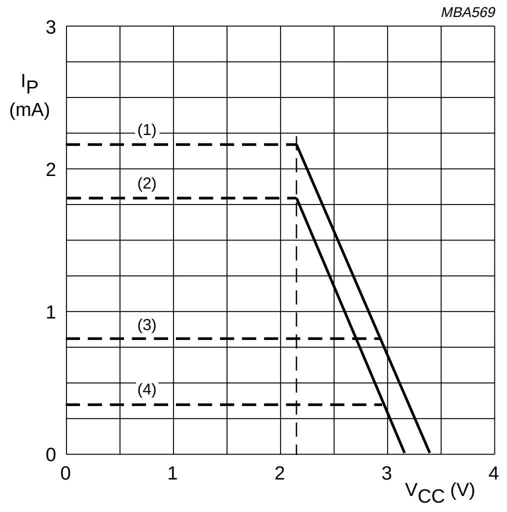
T_{amb}		P_{tot}
(1)	65 °C	1.2 W
(2)	75 °C	1.0 W

Fig.5 TEA1065 safe operating area.



T_{amb}		P_{tot}	
(1)	35 °C	1.2	W
(2)	45 °C	1.07	W
(3)	55 °C	0.93	W
(4)	65 °C	0.8	W
(5)	75 °C	0.67	W

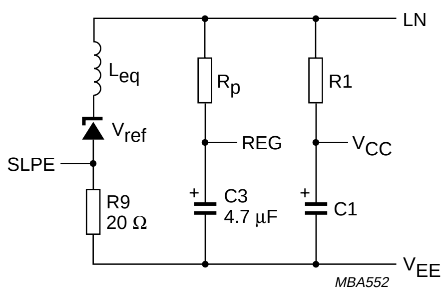
Fig.6 TEA1065T safe operating area.



I_{line} = 15 mA at V_{LN} = 4.45 V
R1 = 620 Ω
R9 = 20 Ω

Curve (1) and (3) are valid when the receiving amplifier is not driven or when MUTE = HIGH, curves (2) and (4) are valid when MUTE = LOW and the receiving amplifier is driven, $V_{o(rms)}$ = 150 mV, R_L = 150 Ω (asymmetrical).
(1) = 2.2 mA; (2) = 1.77 mA; (3) = 0.78 mA and (4) = 0.36 mA.

Fig.7 Maximum current I_p available from V_{CC} for external (peripheral) circuitry with V_{CC} > 2.2 V and V_{CC} > 3 V.



$L_{eq} = C3 \times R9 \times R_p$
R_p = 17.5 kΩ

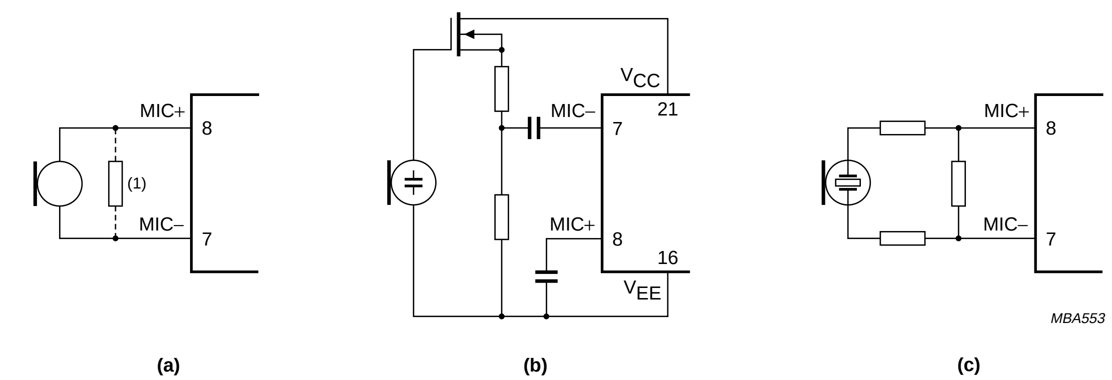
Fig.8 Equivalent circuit impedance between LN and V_{EE}.

Microphone inputs MIC+ and MIC− and gain adjustment connections GAS1 and GAS2

The TEA1065 has symmetrical microphone inputs, its input impedance is 40.8 kΩ (2 × 20.4 kΩ) and its voltage gain is typ. 38 dB with R7 = 68 kΩ. Either dynamic, magnetic or piezoelectric microphones can be used, or an electret microphone with a built-in FET buffer. Arrangements for the microphones types are illustrated in Fig.9.

The gain of the microphone amplifier is proportional to external resistor R7, connected between GAS1 and GAS2, which can be adjusted between 30 dB and 46 dB to suit the sensitivity of the transducer.

An external 100 pF capacitor (C6) is required between GAS1 and SLPE to ensure stability. A larger value of C6 may be chosen to obtain a first-order low-pass filter. The “cut-off” frequency corresponds with the time constant R7 × C6.



(a) magnetic or dynamic microphone, the resistor (1) may be connected to reduce the terminating impedance, or for sensitive types a resistive attenuator can be used to prevent overloading the microphone inputs;

(b) electret microphone;

(c) piezoelectric microphone.

Fig.9 Microphone arrangements.

MUTE input

When MUTE = HIGH the DTMF input is enabled and the microphone and receiving amplifier inputs are inhibited. When MUTE = LOW or open-circuit the DTMF input is inhibited and the microphone and receiving amplifier inputs are enabled. Switching the MUTE input will cause negligible clicks at the earpiece outputs and on the line. An electrostatic discharge protection diode is connected between pin MUTE and pin V_{CC} (pins 20 and 21).

Dual-tone multifrequency input DTMF

When the DTMF input is enabled, dialling tones may be sent onto the line. The voltage gain from DTMF to LN is typ. 12.5 dB less than the gain of the microphone amplifier and varies with R7 in the same way as the gain of the microphone amplifier. This means that the tone level at the DTMF input has to be adjusted after setting the gain of the microphone amplifier. When R7 = 68 kΩ the gain is typically 25.5 dB. The signalling tones can be heard in the earpiece at a low level (confidence tone).

Receiving amplifiers: IR, QR+, QR– and GAR

The receiving amplifier has one input IR and two complementary outputs, QR+ (non-inverting) and QR– (inverting). These outputs may be used for single-ended or differential drive, depending on the type and sensitivity of the earpiece used (see Fig.10). Gain from IR to QR+ is typically 31 dB with R4 = 100 kΩ, which is sufficient for low-impedance magnetic or dynamic earpieces which are suitable for single-ended drive. By using both outputs (differential drive) the gain is increased by 6 dB. Differential drive can be used when earpiece impedance exceeds 450 Ω as with high impedance dynamic, magnetic or piezoelectric earpieces.

The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions where the ratio of peak and RMS value is higher.

The gain of the receiving amplifier can be adjusted over a range of –11 dB to +8 dB to suit the sensitivity of the transducer that is used. The gain is proportional to external resistor R4 connected between GAR and QR+.

Two external capacitors, C4 = 100 pF and C7 = 1 nF, are necessary to ensure stability. A larger value of C4 may be chosen to obtain a first-order low-pass filter. The “cut-off” frequency corresponds with the time constant R4 × C4.

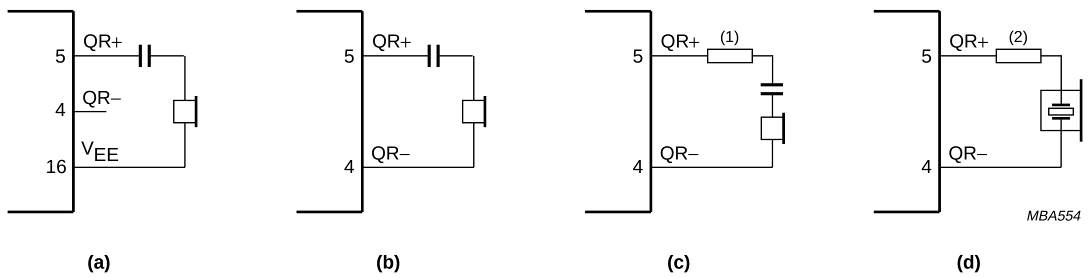


Fig.10 Alternative receiver arrangements:
(a) dynamic earpiece with an impedance less than 450 Ω;
(b) dynamic earpiece with an impedance more than 450 Ω;
(c) magnetic earpiece with an impedance more than 450 Ω, resistor (1) may be connected to prevent distortion (inductive load);
(d) piezoelectric earpiece, resistor (2) is required to increase the phase margin (stability with capacitive load).

Automatic gain control

Automatic compensation of line loss is obtained by connecting a resistor (R6) between AGC and V_{EE}. The automatic gain control varies the gain of the microphone amplifier and receiving amplifier in accordance with the DC line current (see Fig.12). The control range is 5.9 dB; this corresponds to a line length of 3.5 km of twisted pair cable (see Fig.11). The DTMF gain is not affected by this feature.

If automatic line loss compensation is not required the AGC pin can be left open-circuit, the amplifiers then give their maximum gain.

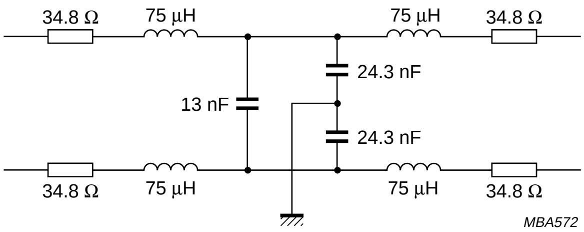


Fig.11 Typical 0.5 km line cell model used for automatic gain control optimization.

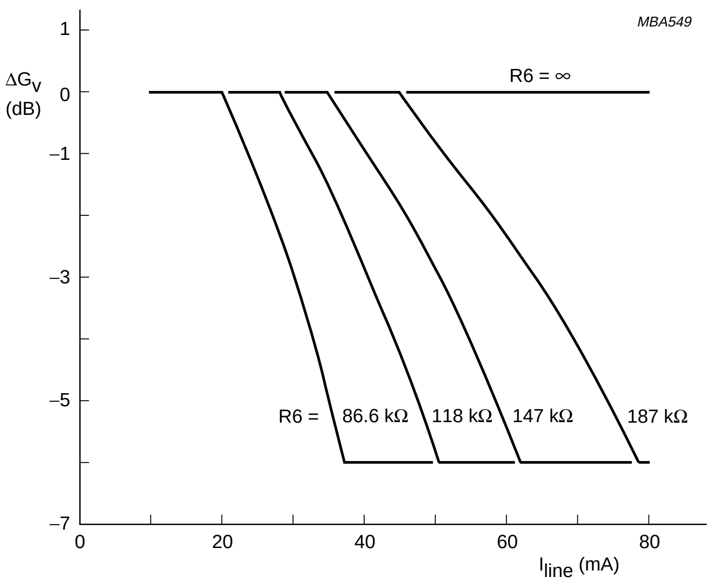


Fig.12 Variation of gain as a function of line current with R6 as a parameter; R9 = 20 Ω.

Power-down input PD

During pulse dialling or register recall (timed-loop-break) the telephone line is interrupted, consequently it provides no supply for the transmission circuit and the peripherals connected to V_{CC}. These gaps have to be bridged by the charge in the smoothing capacitor C1. The requirement on this capacitor is relaxed by applying a HIGH level to the PD input during the loop-break. This reduces the internal supply current from typ. 1.14 mA to 73 µA.

A HIGH level at PD also disconnects the capacitor at REG which results in the voltage stabilizer having no switch-on delay after line interruptions. This results in no contribution of the IC to the current waveform during pulse dialling or register recall. When this facility is not required PD may be left open-circuit or connected to V_{EE}. An electrostatic discharge protection diode is connected between pin PD and V_{CC}.

Digital pulse input DPI

A HIGH level at DPI creates a current which flows from pin DOC to V_{EE} in order to interrupt the line current by the external line current control transistor (see Fig.18; MOSFET BUK554). A LOW level (or pin left open-circuit) disables this current to provide the normal DC regulation (voltage or current). A simple application without regulation of current in pulse dialling mode is given in Fig.18.

When DPI is activated (HIGH level), the external line current control transistor is switched off resulting in no current in the TEA1065. The voltage on pin SLPE becomes zero and capacitor C15 discharges cancelling the current regulation when DPI becomes inactive (LOW level).

To provide a constant regulation (in speech mode and pulse mode), an external transistor is required to keep C15 charged during DPI active (see Fig.19 in which the Field Effect Transistor BSJ177 is directly driven by the DPI signal).
An electrostatic discharge protection diode is connected between pin DPI and pin V_{CC}.

Voltage sense input and reference voltage input VSI and REFI

The voltage on pin VSI represents the DC voltage of pin SLPE. The RC filter (R15 × C15) is also intended to disable the DC regulation when C15 is shunted or not yet charged (especially directly after hook-off). The time constant R15 × C15 determines approximately the time when no regulation (except CURL pin limitation) is activated.
The voltage applied on pin REFI represents a fraction of the bandgap reference voltage given by pin VBG (resistor tap R13 and R14) in order to determine I_{knee}.

Drive current output DOC

Pin DOC drives the external line current control transistor in order to achieve line interruption during pulse dialling (or register recall) and also the DC slope when $I_{line} > I_{knee}$.
The current sunk by pin DOC is determined by the voltage on pin VSI in comparison with the voltage on pin VBG divided by the resistor tap R13 and R14.
When pin DPI is activated, pin DOC changes to a low voltage (by trying to sink typ. 900 µA to V_{EE}) to switch off the external line current control transistor.

Bandgap reference output VBG

This output provides a voltage reference to set the knee line current with the following formula:

$$I_{knee} = I_{CC} + I_P + (VBG/R9) \times \{R14/(R14 + R13)\} - (R15/R9) \times 2.5 \times 10^{-6}$$

In order to improve stability, a capacitive load is not allowed on this output.

Current limit input CURL

This input is applied to the base of an internal NPN transistor which has its collector connected to pin DOC and its emitter to V_{EE} (see Fig.13). The transistor limits the line current just after hook-off or during line transients to a value given by the following formula:

$$I_{hook\text{-}off} = I(R1) + V_{BE}/R9b$$

V_{BE} is the base-emitter voltage of the transistor (typ. 700 mV at 25 °C). I(R1) is the current flowing through R1 to charge C1 just after hook-off.

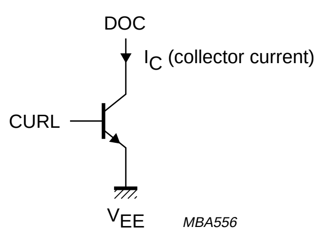


Fig.13 Internal current limiting transistor.

The maximum hook-off current then becomes:

$I_{hook\text{-}off} = V_Z/R1 + V_{BE} \times (R9a + R9b + R1)/(R1 \times R9b)$

where V_Z is the Zener voltage of diode D5 (see Fig.18).

Side-tone suppression

Suppression of the transmitted signal in the earpiece is obtained by the anti-sidetone network comprising R1//Z_{line}, R2, R3, R9 and Z_{bal} (see Fig.18). Maximum compensation is obtained when the following conditions are fulfilled:

a) $R9 \times R2 = R1 \times (R3 + R8)$
b) $k = R3 \times (R8 + R9)/(R2 \times R9)$
c) $Z_{bal} = k \times Z_{line}$

The scale factor k is chosen to meet the compatibility with a standard capacitor from the E6 or E12 range for $Z_{bal.}$

In practice Z_{line} varies considerably with the line length and line type. Therefore, the value chosen for Z_{bal} should be for an average line length giving satisfactory sidetone suppression with long and short times. The suppression also depends on the accuracy of the match between Z_{bal} and the impedance of the average line.

Example

With k = 1, R1 = 619 Ω, R9 = 20 Ω and an average line impedance represented by 270 Ω + (120 nF // 1100 Ω), the calculation results in:

- R2 = 130 kΩ
- R3 = 3650 Ω
- R8 = 715 Ω

The anti-sidetone network for the TEA1060 family, shown in Fig.15, attenuates the signal received from the line by 32 dB before it enters the receiving amplifier. The attenuation is almost constant over the whole audio-frequency range.

Note

More information on the balancing of the anti-sidetone bridges can be obtained in our publication *“Versatile speech transmission ICs for electronic telephone sets”*, order number 9398 341 10011.

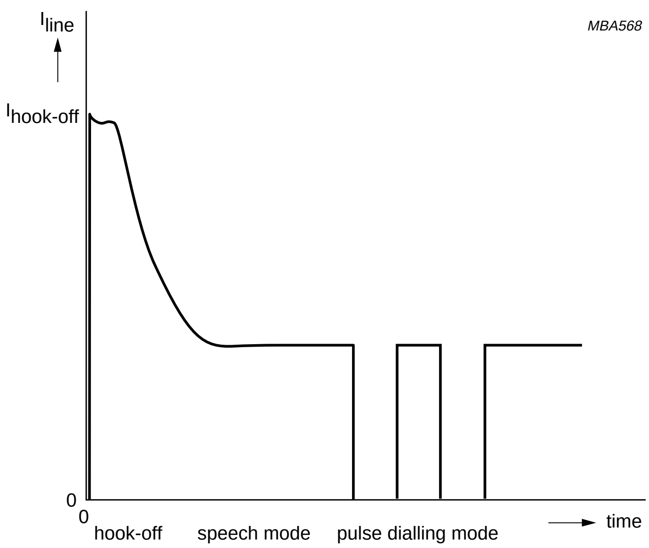


Fig.14 Example of line current shape in pulse dialling mode (see also Fig.18).

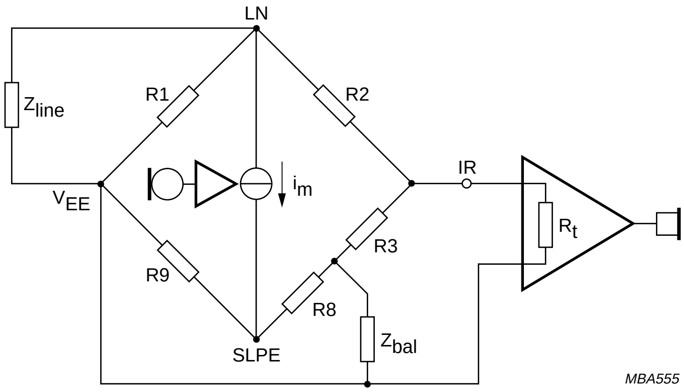


Fig.15 Equivalent circuit of TEA1060 family anti-sidetone bridge.

LIMITING VALUES

In accordance with the absolute maximum system (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{LN}	positive line voltage continuous		–	12	V
V_{DOC}	positive DOC voltage continuous		–	12	V
V_{LN}	repetitive line voltage during switch-on or line interruption		–	13.2	V
I_{LN}	line current (see also Fig.5 and 6)		–	150	mA
V_I	input voltage on pins other than LN, DOC, VSI, REFI and CURL		$V_{EE} - 0.7$	$V_{CC} + 0.7$	V
P_{tot}	total power dissipation	see Figs 5 and 6			
T_{stg}	storage temperature range		–40	+ 125	°C
T_{amb}	operating ambient temperature range		–25	+75	°C
T_j	junction temperature		–	+125	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air; TEA1065	–	50	K/W
$R_{th\ j\text{-}a}$	from junction to ambient in free air; TEA1065T (1)	–	75	K/W

Note

1. TEA1065T is mounted on glassy epoxy board 28.5 × 19.1 × 1.5 mm

HANDLING

Every pin withstands the ESD test in accordance with MIL-STD-883C class 2, method 3015 (HBM 1500 Ω, 100 pF, 3 positive pulses and 3 negative pulses on each pin as a function of pin V_{EE}.

CHARACTERISTICS

I_{LN} = 10 to 150 mA; V_{EE} = 0 V; f = 800 Hz; T_{amb} = 25 °C; R9 = 20 Ω; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply LN and V_{CC} (pins 1 and 21)						
V_{LN}	voltage drop over circuit	I_{line} = 5 mA	3.95	4.25	4.55	V
		I_{line} = 15 mA	4.25	4.45	4.65	V
		I_{line} = 100 mA	5.4	6.1	6.7	V
		I_{line} = 140 mA	–	–	7.5	V
$\Delta V_{LN}/\Delta T$	variation with temperature	I_{line} = 15 mA	–3	–1	+1	mV/K
V_{LN}	voltage drop over circuit	I_{line} = 15 mA				
		$R_{VA} = R_{1-22}$ = 68 kΩ	3.6	3.9	4.15	V
		$R_{VA} = R_{22-24}$ = 39 kΩ	4.7	5.0	5.3	V
I_{CC}	supply current	PD = LOW; V_{CC} = 2.8 V	–	1.14	1.5	mA
		PD = HIGH; V_{CC} = 2.8 V	–	73	105	μA
Microphone inputs MIC+ and MIC– (pins 8 and 7)						
$\lvert Z_i \rvert$	input impedance		18.5	20.4	24.3	kΩ
G_v	voltage gain	I_{line} = 15 mA; R7 = 68 kΩ	37	38	39	dB
$\Delta G_v f$	variation with frequency referred to 800 Hz	I_{line} = 15 mA; f = 300 to 3400 Hz	–0.5	±0.2	+0.5	dB
$\Delta G_v T$	variation with temperature referred to 25 °C	I_{line} = 50 mA; T_{amb} = –25 to 75 °C; without R6	–	±0.5	–	dB
Dual-tone multi-frequency input DTMF (pin 19)						
$\lvert Z_i \rvert$	input impedance		16.8	20.7	24.6	kΩ
G_v	voltage gain	I_{line} = 15 mA; R7 = 68 kΩ	24.5	25.5	26.5	dB
$\Delta G_v f$	variation with frequency referred to 800 Hz	I_{line} = 15 mA f = 300 to 3400 Hz	–0.5	±0.2	+0.5	dB
$\Delta G_v T$	variation with temperature referred to 25 °C	I_{line} = 50 mA; T_{amb} = –25 to +75 °C	–	±0.5	–	dB
Gain adjustment GAS1 and GAS2 (pin 2 and 3)						
ΔG_v	gain variation with R7 connected between pins 2 and 3; transmitting amplifier		–8	–	+8	dB

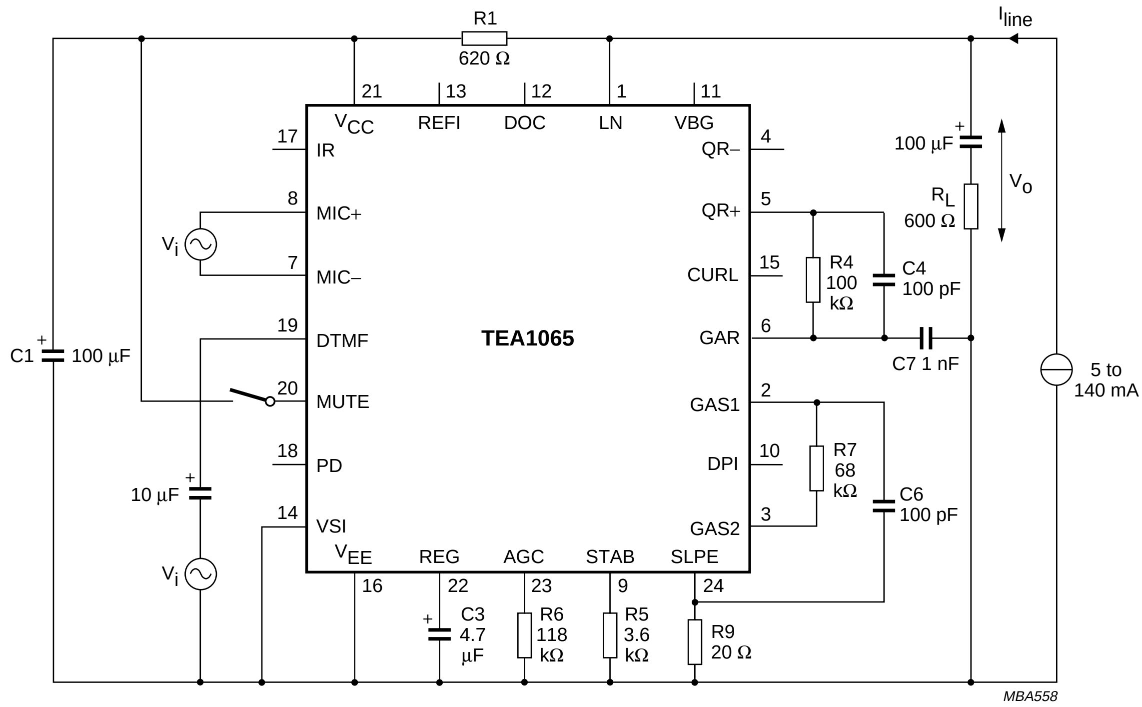
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Transmitting amplifier output LN (pin 1)						
$V_{LN(rms)}$	output voltage (RMS value)	I_{line} = 15 mA				
		d_{tot} = 2%	1.9	2.3	–	V
		d_{tot} = 10%	–	2.6	–	V
$V_{no(rms)}$	noise output voltage (RMS value)	I_{line} = 15 mA; R7 = 68 kΩ; pin 7 and 8 open-circuit psophometrically weighted (P53 curve); control transistor included (MOS BUK554 type see Fig.18)	–	–68	–	dBmp
Receiving amplifier input IR (pin 17)						
Z_I	input impedance		17	21	25	kΩ
Receiving amplifier outputs QR+ and QR– (pin 5 and 4)						
Z_O	output impedance		–	4	–	Ω
G_v	voltage gain	I_{line} = 15 mA; R4 = 100 kΩ				
		single-ended; RT = 300 Ω	30	31	32	dB
		differential; RT = 600 Ω	36	37	38	dB
ΔG_vf	variation with frequency referred to 800 Hz	f = 300 to 3400 Hz	–0.5	±0.2	+0.5	dB
ΔG_vT	variation with temperature referred to 25 °C	without R6; I_{line} = 50 mA; T_{amb} = –25 to +75 °C	–	±0.2	–	dB
$V_{O(rms)}$	output voltage (RMS value)	I_{line} = 15 mA; THD = 2%; sinewave drive; R4 = 100 kΩ				
		single-ended; RT = 150 Ω	0.3	0.38	–	V
		differential; RT = 450 Ω	0.56	0.72	–	V
		differential; CT = 60 nF; (1500 Ω series resistor); f = 3400 Hz	0.87	1.07	–	V
		I_{line} = 30 mA; differential; CT = 60 nF; (1500 Ω series resistor); f = 3400 Hz	1.02	1.22	–	V
$V_{O(rms)}$	noise output voltage (RMS value)	I_{line} = 15 mA; R4 = 100 kΩ				
		single-ended; RT = 300 Ω	–	50	–	µV
		differential; RT = 600 Ω	–	100	–	µV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Gain adjustment GAR (pin 6)						
ΔG_v	receiving amplifier, gain adjustment range		–11	–	+8	dB
Mute input MUTE (pin 20)						
V_{IH}	input voltage HIGH		1.5	–	V_{CC}	V
V_{IL}	input voltage LOW		–	–	0.3	V
I_{MUTE}	input current		–	8	15	μA
ΔG_v	change of microphone amplifier gain	MUTE = HIGH	–	–70	–	dB
G_v	voltage gain from DTMF input to QR+ or QR–	MUTE = HIGH; R4 = 100 kΩ single-ended; RT = 300 Ω	–19	–17	–15	dB
Power-down input PD (pin 18)						
V_{IH}	input voltage HIGH		1.5	-	V_{CC}	V
V_{IL}	input voltage LOW		-	-	0.3	V
I_{PD}	input current		-	2.5	5.0	μA
Automatic gain control input AGC (pin 23)						
ΔG_v	controlling the gain from IR to QR+, QR– and the gain from MIC+, MIC– to LN; gain control range with respect to I_{line} = 15 mA	R6 = 118 kΩ	–5.5	–5.9	–6.3	dB
I_{line}	highest line current for maximum gain		–	28	–	mA
I_{line}	lowest line current for minimum gain		–	50	–	mA
ΔG_v	change of gain between I_{line} = 15 and 35.5 mA		–	-1.5	–	dB
Current limiting input CURL (pin 15)						
V_{BE}	base-emitter voltage drop of internal transistor	see Fig.13; I_C = 50 μA = I_{DOC}	–	0.7	–	V
H_{FE}	current gain of internal transistor	see Fig.13; I_C = 50 μA = I_{DOC}	60	120	–	
$I_{C(max)}$	maximum collector current of internal transistor	see Fig.13	–	–	2	mA
Bandgap reference voltage output VBG (pin 12)						
V_{BG}	reference voltage		–	1.22	–	V
I_{BG}	output drive capability	note 1	–100	-	+50	μA
Z_O	output impedance		–	12	–	Ω

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Voltage sense input VSI (pin 14)						
I_O	output current	pin VSI connected to V_{EE}	–	–2.5	–	µA
Reference input REFI (pin 13)						
I_O	output current		–	–	2.0	mA
Drive current output DOC (pin 11)						
I_O	output current	REFI connected to V_{EE}; VSI not connected; DPI = LOW	120	300	–	µA
		REFI not connected; VSI connected to V_{EE}; DPI = HIGH	200	900	–	µA
Digital pulse input DPI (pin 10)						
V_{IH}	input voltage HIGH		1.5	–	V_{CC}	V
V_{IL}	input voltage LOW		–	–	0.3	V
I_{DPI}	input current		–	2.5	5	µA

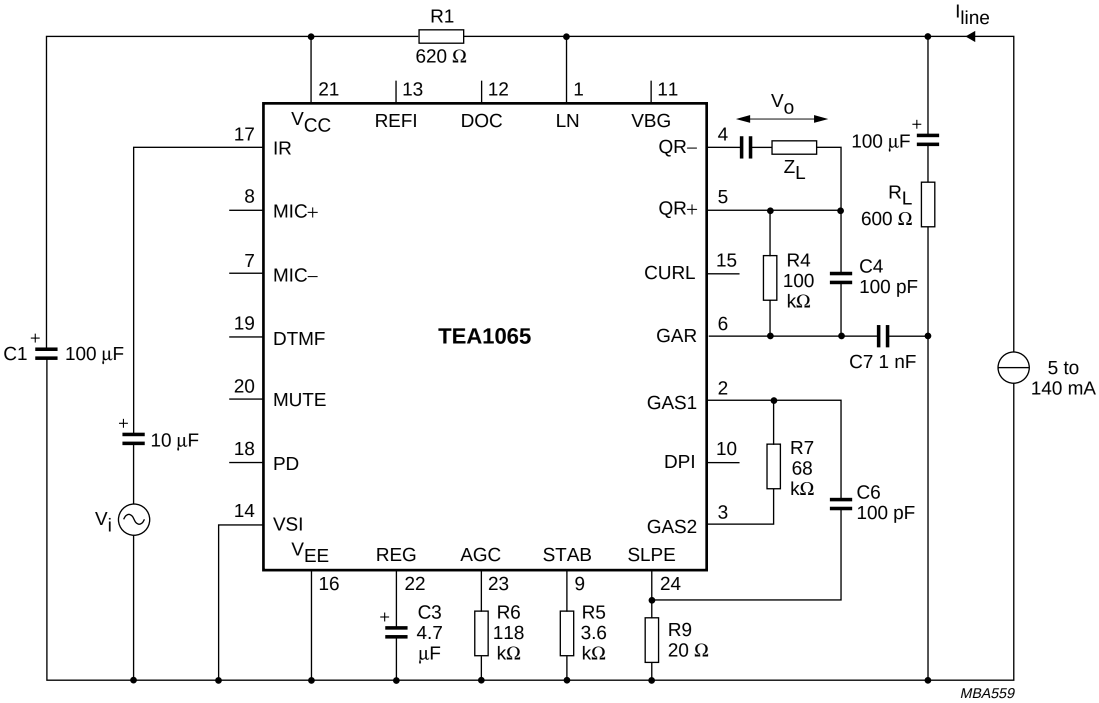
Note

1. No capacitive load on the V_{BG} output. Positive current is defined as conventional current flow into a device. Negative current is defined as conventional current flow out of a device.



Voltage gain is defined as $G_v = 20 \text{ Log } |V_o/V_i|$. For measuring the gain from MIC+ and MIC– the MUTE input should be LOW or open-circuit, for measuring the DTMF input MUTE should be HIGH. Inputs not under test should be open-circuit except VSI that should be connected to V_{EE}.

Fig.16 Test circuit for defining voltage gain of MIC+, MIC– and DTMF inputs.



Voltage gain is defined as $G_v = 20 \text{ Log } |V_o/V_i|$.

Fig.17 Test circuit for defining voltage gain of the receiving amplifier.

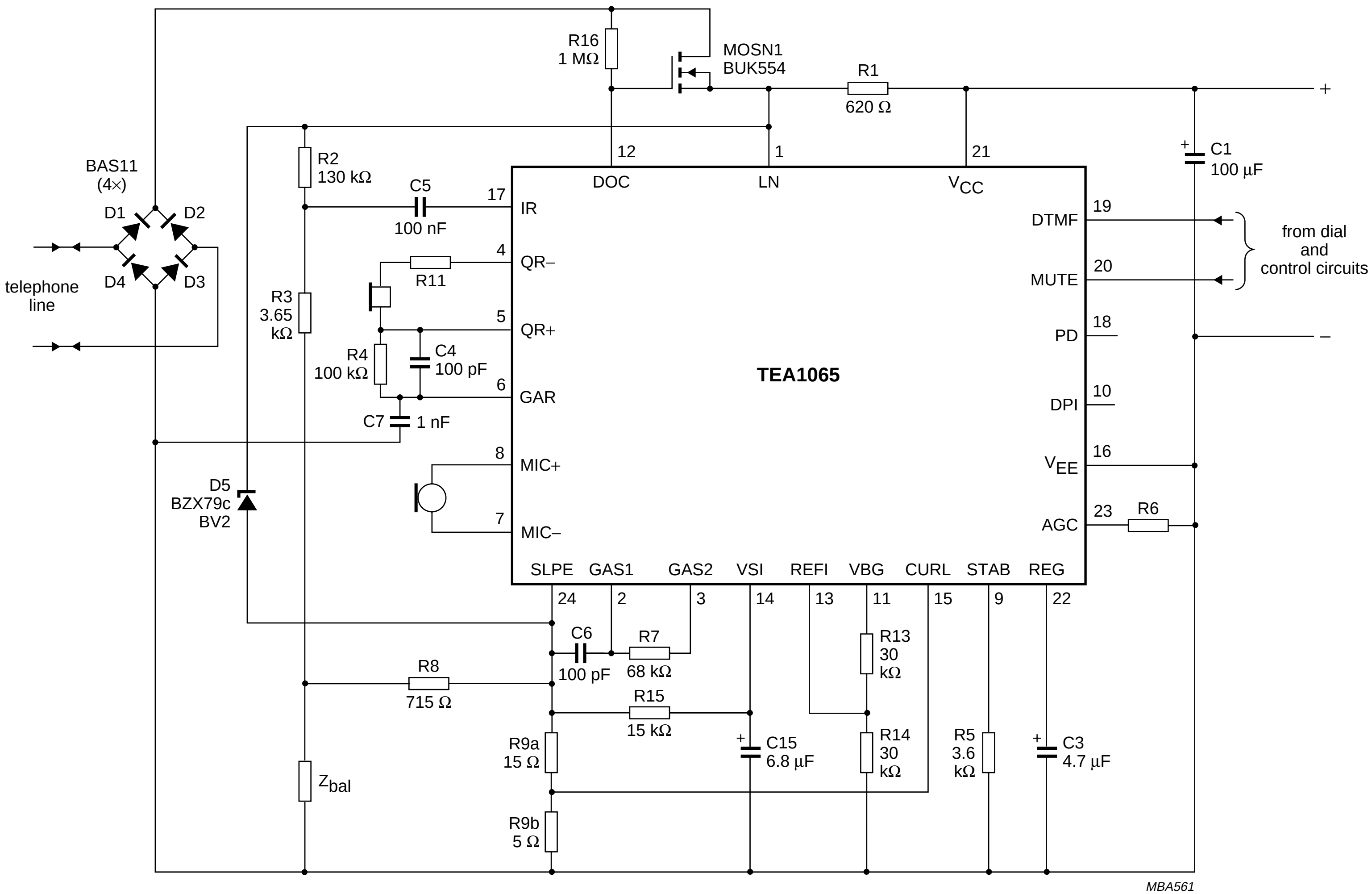
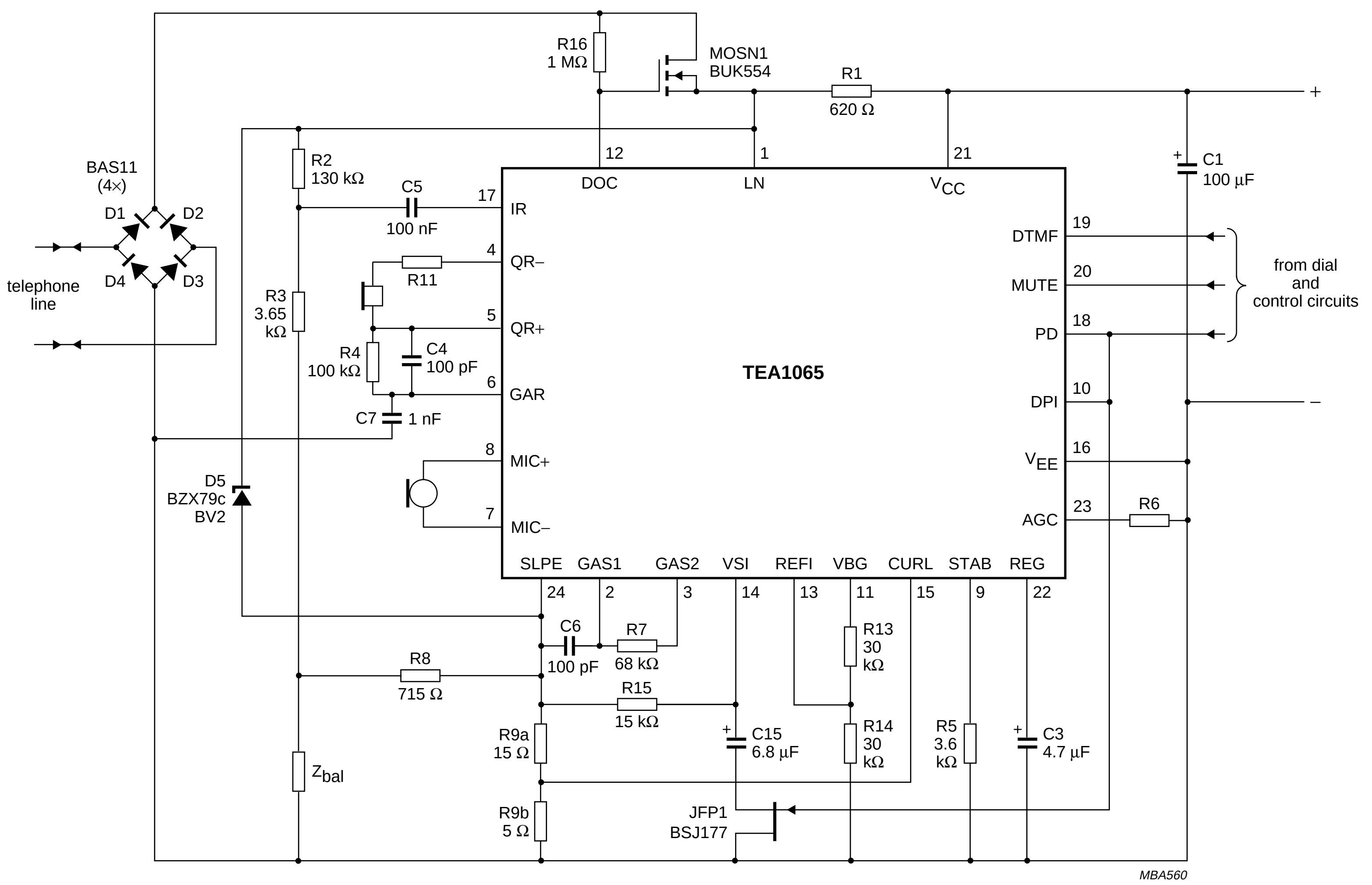


Fig.18 Typical application of the TEA1065, with a piezoelectric earpiece and DTMF dialling.

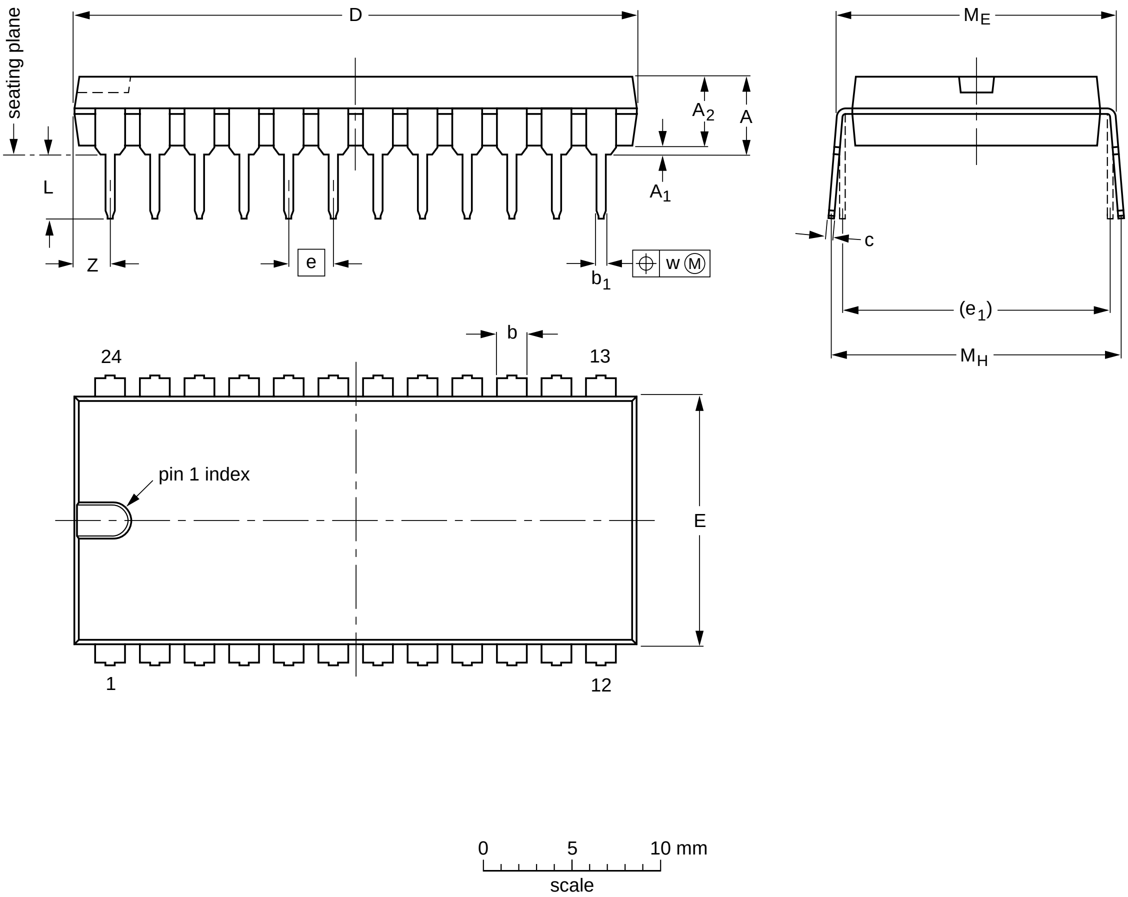


DTMF dialling requires a different protection arrangement.

Fig.19 Typical application of the TEA1065, with a piezoelectric earpiece and pulse dialling.

PACKAGE OUTLINES

DIP24: plastic dual in-line package; 24 leads (600 mil) — SOT101-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

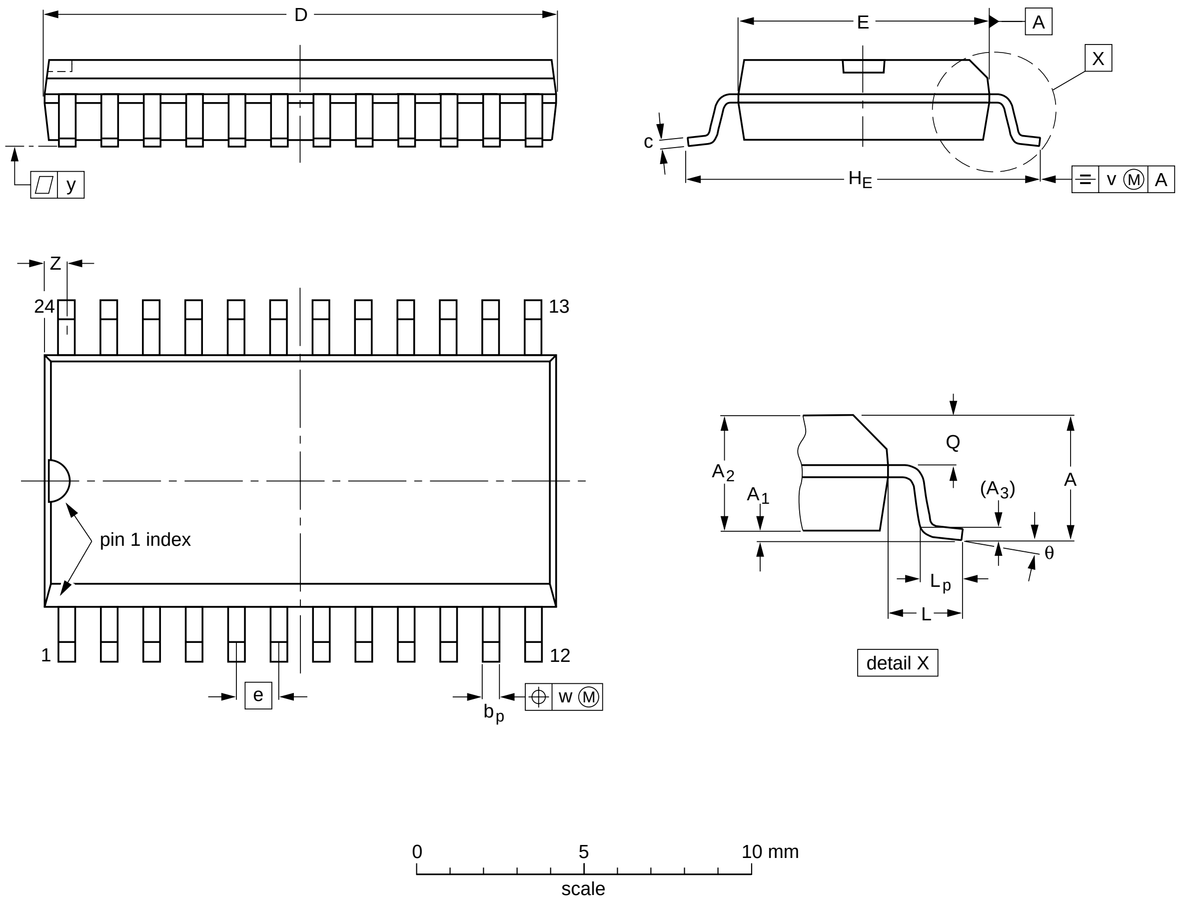
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	32.0 31.4	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	2.2
inches	0.20	0.020	0.16	0.066 0.051	0.021 0.015	0.013 0.009	1.26 1.24	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT101-1	051G02	MO-015AD				~~92-11-17~~ 95-01-23

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~95-01-24~~ 97-05-22

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *“Data Handbook IC26; Integrated Circuit Packages”* (order code 9398 652 90011).

DIP

SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO

REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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