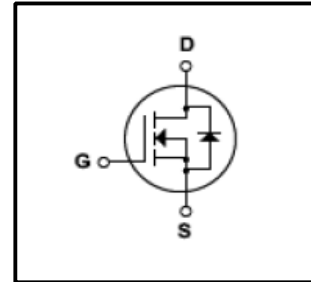


Silicon N-Channel MOSFET

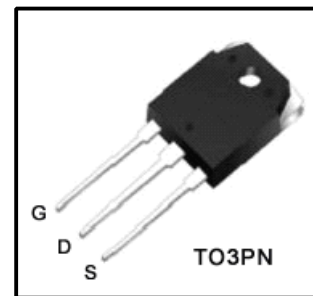
Features

- 18A,500V, $R_{DS(on)}$ (Max0.27 Ω)@ $V_{GS}=10V$
- Ultra-low Gate charge(Typical 42nC)
- Fast Switching Capability
- 100%Avalanche Tested
- Maximum Junction Temperature Range(150 $^{\circ}C$)



General Description

This Power MOSFET is produced using Winsemi's advanced planar stripe, VDMOS technology. This latest technology has been especially designed to minimize on-state resistance, have a high rugged avalanche characteristics. This device is specially well-suited for AC-DC switching power supplies, DC-DC power Converters high voltage H-bridge motor drive PWM



Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{DSS}	Drain Source Voltage	500	V
I_D	Continuous Drain Current(@ $T_c=25^{\circ}C$)	18	A
	Continuous Drain Current(@ $T_c=100^{\circ}C$)	12.7	A
I_{DM}	Drain Current Pulsed (Note1)	80	A
V_{GS}	Gate to Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note2)	330	mJ
E_{AR}	Repetitive Avalanche Energy (Note1)	27.7	mJ
dv/dt	Peak Diode Recovery dv /dt (Note3)	4.5	V/ ns
P_D	Total Power Dissipation(@ $T_c=25^{\circ}C$)	280	W
T_J, T_{stg}	Junction and Storage Temperature	-55~150	$^{\circ}C$
T_L	Channel Temperature	300	$^{\circ}C$

Thermal Characteristics

Symbol	Parameter	Value			Units
		Min	Typ	Max	
R_{QJC}	Thermal Resistance , Junction -to -Case	-	-	0.45	$^{\circ}C/W$
R_{QCS}	Thermal Resistance , Case-to-Sink	-	0.24	-	$^{\circ}C/W$
R_{QJA}	Thermal Resistance , Junction-to -Ambient	-	-	40	$^{\circ}C/W$

Electrical Characteristics(Tc=25°C)

Characteristics	Symbol	Test Condition	Min	Type	Max	Unit	
Gate leakage current	I _{GSS}	V _{GS} =±25V, V _{DS} =0V	-	-	±10	nA	
Gate-source breakdown voltage	V _{(BR)GSS}	I _G =±10 μA, V _{DS} =0V	±30	-	-	V	
Drain cut -off current	I _{DSS}	V _{DS} =500V, V _{GS} =0V	-	-	100	μA	
Drain -source breakdown voltage	V _{(BR)DSS}	I _D =10 mA, V _{GS} =0V	500	-	-	V	
Breakdown voltage Temperature coefficient	$\frac{\Delta BV_{DSS}}{\Delta T_J}$	I _D =250μA, Referenced to 25°C	-	0.5	-	V/°C	
Gate threshold voltage	V _{GS(th)}	V _{DS} =10V, I _D =1mA	3	-	5	V	
Drain -source ON resistance	R _{DS(ON)}	V _{GS} =10V, I _D =9A	-	0.23	0.27	Ω	
Forward Transconductance	g _{fs}	V _{DS} =40V, I _D =9A	-	16	-	S	
Input capacitance	C _{iss}	V _{DS} =25V,	-	2530	3290	pF	
Reverse transfer capacitance	C _{rss}	V _{GS} =0V,	-	11	14.3		
Output capacitance	C _{oss}	f=1MHz	-	300	390		
Switching time	Rise time	tr	V _{DD} =250V,	-	40	90	ns
	Turn-on time	ton	I _D =18A	-	150	310	
	Fall time	tf	R _G =25Ω	-	95	200	
	Turn-off time	toff	(Note4,5)	-	110	230	
Total gate charge(gate-source plus gate-drain)	Q _g	V _{DD} =400V, V _{GS} =10V,	-	42	55	nC	
Gate-source charge	Q _{gs}	I _D =18A	-	12	-		
Gate-drain("miller") Charge	Q _{gd}	(Note4,5)	-	14	-		

Source-Drain Ratings and Characteristics(Ta=25°C)

Characteristics	Symbol	Test Condition	Min	Type	Max	Unit
Continuous drain reverse current	I _{DR}	-	-	-	18	A
Pulse drain reverse current	I _{DRP}	-	-	-	72	A
Forward voltage(diode)	V _{DSF}	I _{DR} =18A, V _{GS} =0V	-	-	1.4	V
Reverse recovery time	trr	I _{DR} =18A, V _{GS} =0V,	-	500	-	ns
Reverse recovery charge	Q _{rr}	dI _{DR} / dt =100 A / μs	-	5.4	-	μC

Note 1.Repeativity rating :pulse width limited by junction temperature

2.L=5.2mH I_{AS}=18A, V_{DD}=50V, R_G=25Ω, Starting T_J=25°C

3. I_{SD}≤18A, di/dt≤200A/us, V_{DD}<BV_{DSS}, STARTING T_J=25°C

4. Pulse Test:Pulse Width≤300us, Duty Cycle≤2%

5. Essentially independent of operating temperature.

This transistor is an electrostatic sensitive device

Please handle with caution

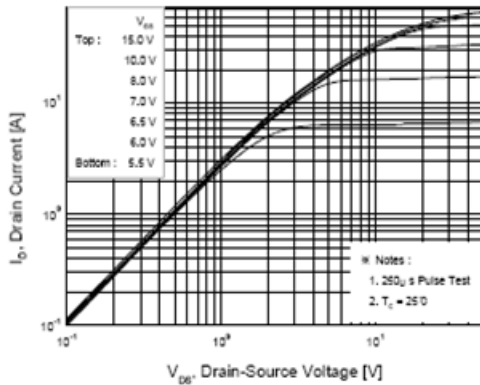


Fig.1 On State Characteristics

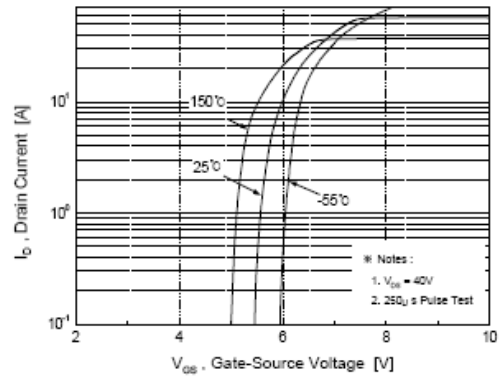


Fig.2 Transfer Current Characteristics

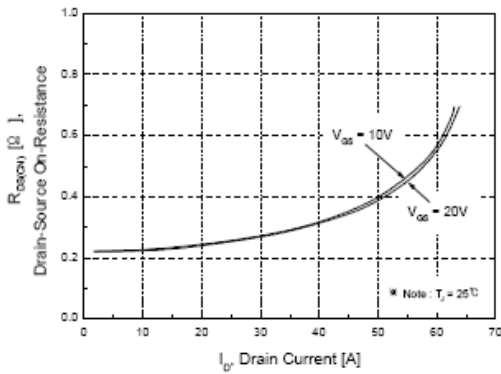


Fig.3 On-Resistance Variation vs Drain Current

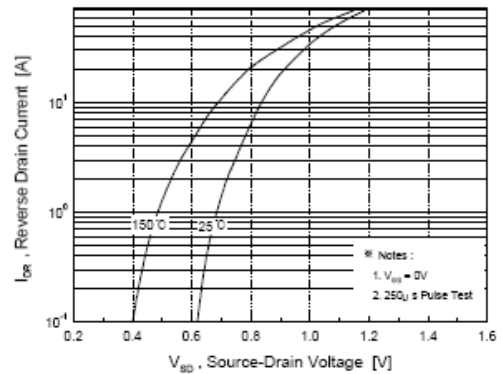


Fig.4 Body Diode Forward Voltage Variation with Source Current and Temperature

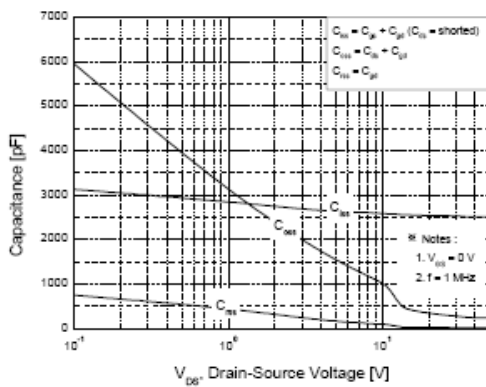


Fig.5 Capacitance Characteristics

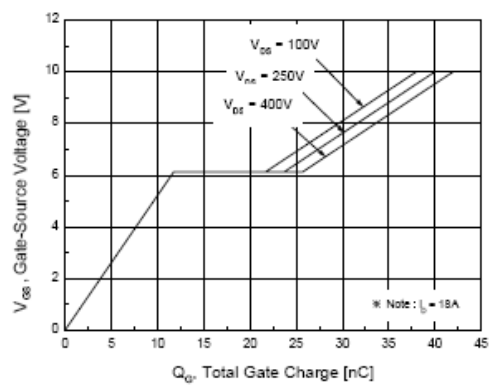


Fig.6 Gate Charge Characteristics

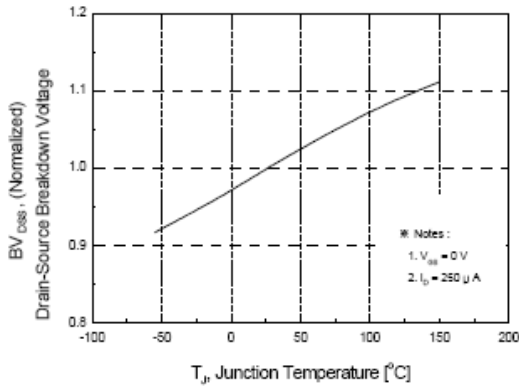


Fig.7 Breakdown Voltage Variation

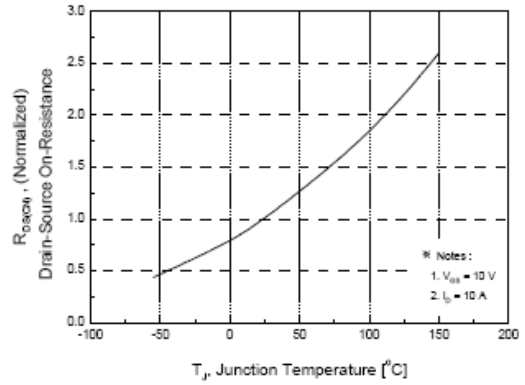


Fig.8 On-Resistance Variation vs. Temperature

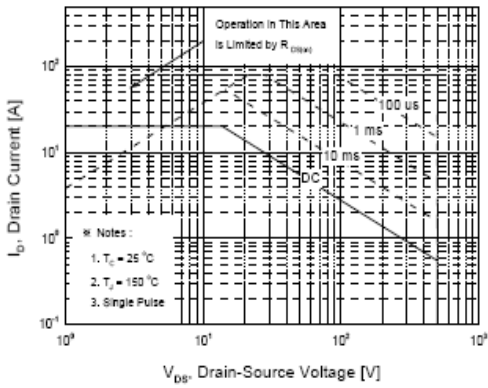


Fig.9 Maximum Safe Operation Area

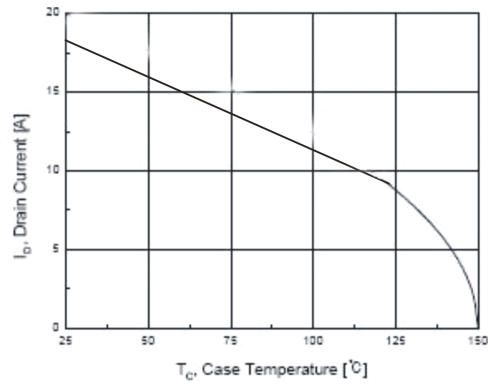


Fig.10 Maximum Drain Current vs Case Temperature

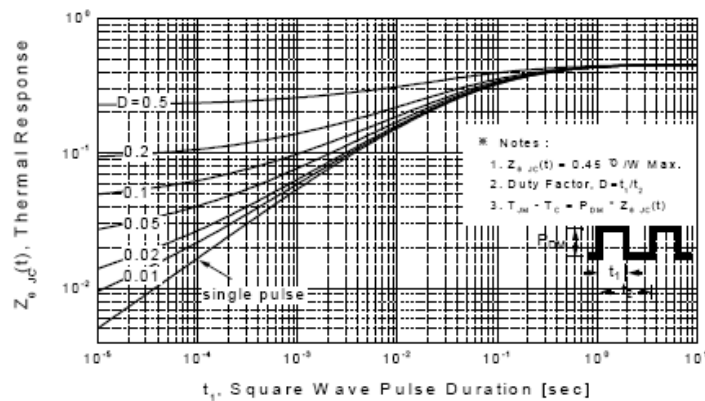


Fig.11 Transient Thermal Response Curve

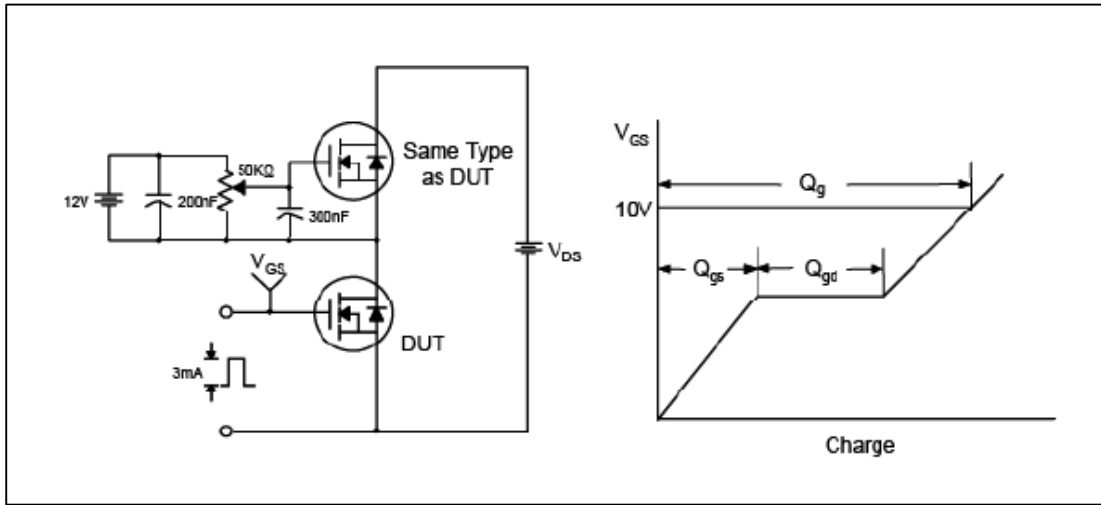


Fig.12 Gate Test Circuit & Waveform

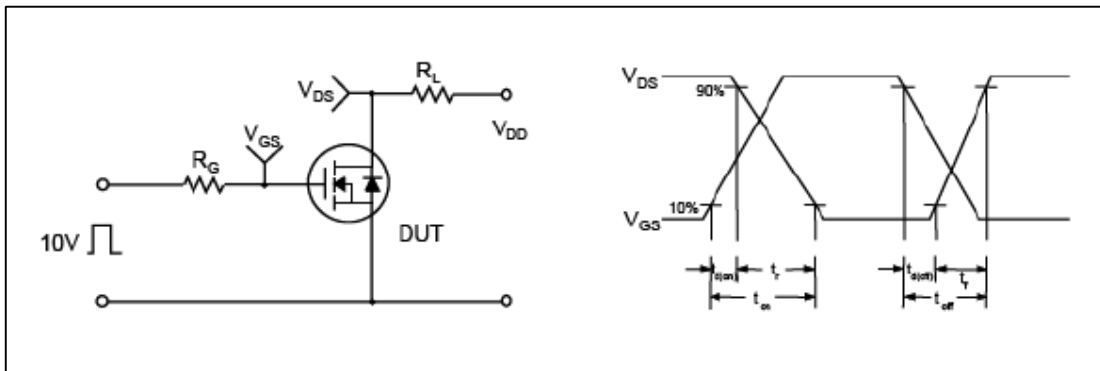


Fig.13 Resistive Switching Test Circuit & Waveform

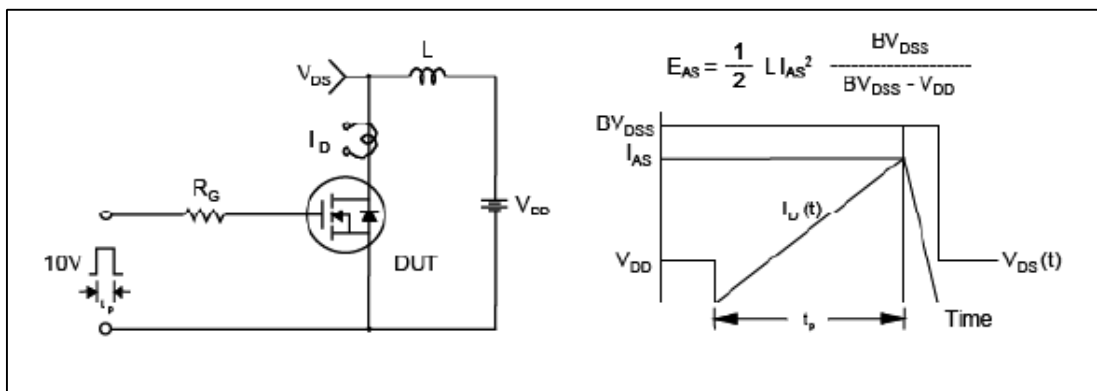


Fig.14 Unclamped Inductive Switching Test Circuit & Waveform

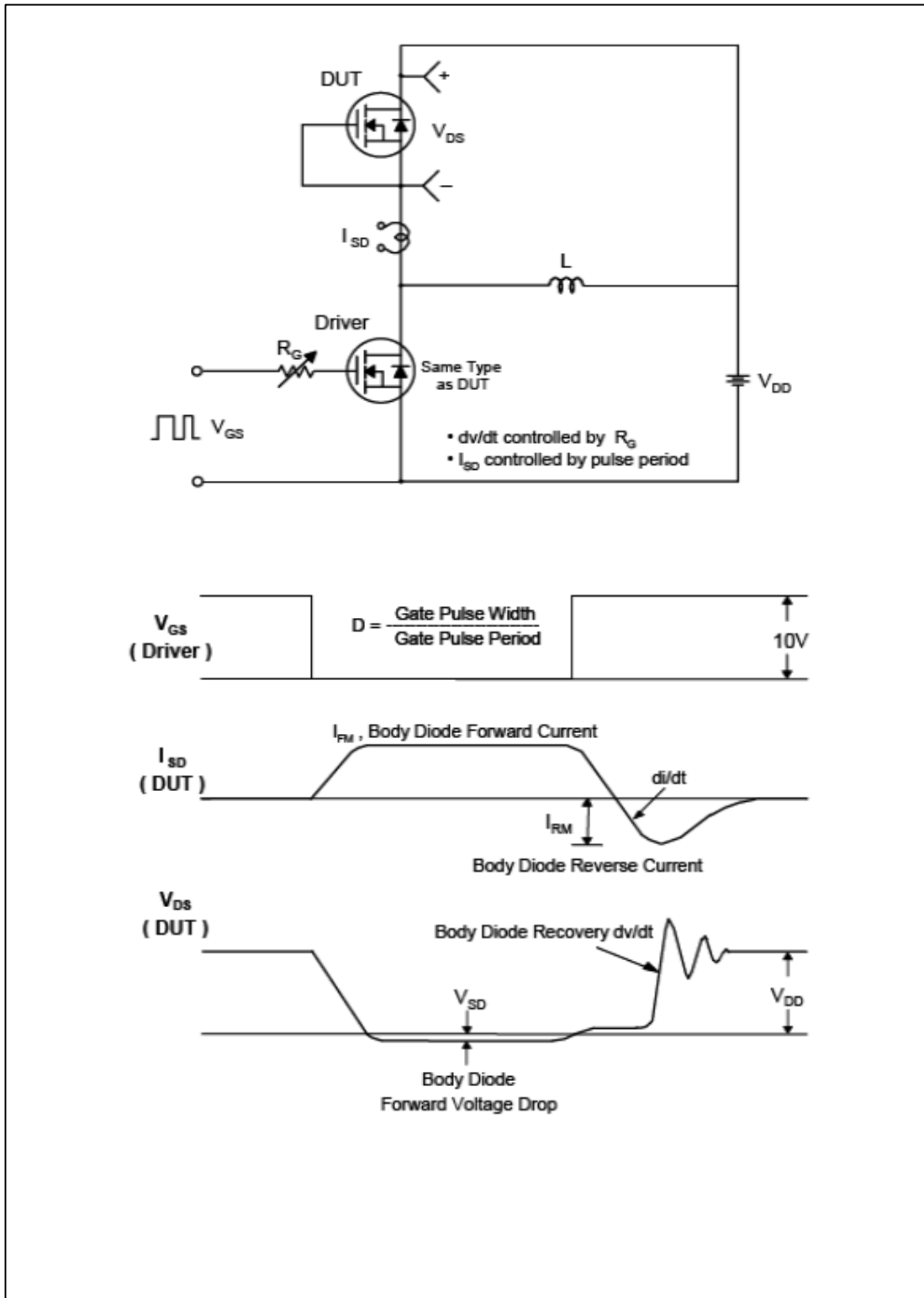


Fig.15 Peak Diode Recovery dv/dt Test Circuit & Waveform

TO-3PN Package Dimension

