

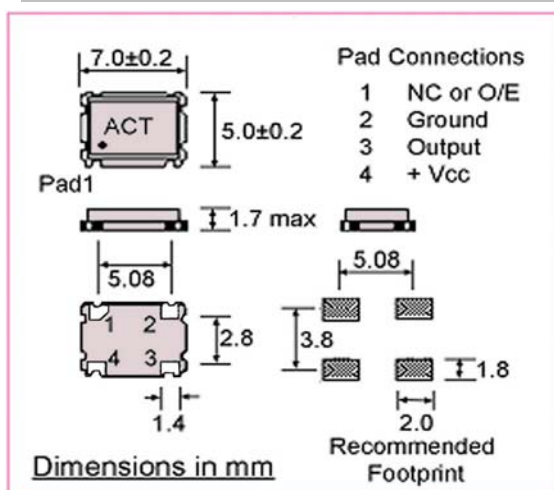
## ACT9200L

The ACT9200 family is a miniature, low profile SMD package, with a ceramic base utilising a seam welded metal lid for high reliability and better long-term stability. The metal lid is grounded through the package to assist with EMI emission reductions. This 7x5mm device is available as the ACT9200 in both 3V3 and 5V0 (see ACT9200 datasheet). A 32.768kHz version is available as the 9200WC (See 9200WC data sheet). Taped and reeled packaging (1k reels) and loose quantities are available for purchase, to suit high and low volume production.



## Specification

Parameter	Symb.	Specification		Condition
Supply Voltage	Vdd	2.5Vdc ± 10%	1.8Vdc ± 10%	Please specify
Frequency Range	fo	1.000 ~ 200.00 MHz		Please specify
Frequency Stability	Δf/fo	±15ppm ~ ±100ppm		Please specify
Temp Operating Range	Topr	0 ~ +70°C standard to -40 ~ +85°C		Please specify
Temp Storage Range	Tstg	-55 to +125°C		
Supply Current (max)	Iop	10mA (1.000 ~ 34.999 MHz)	8mA (1.000 ~ 34.999 MHz)	
		20mA (35.000 ~ 60.00 MHz)	15mA (35.000 ~ 60.00 MHz)	
		30mA (60.001 ~ 99.999 MHz)	25mA (60.001 ~ 99.999 MHz)	
		40mA (100.00 ~ 155.00 MHz)	35mA (100.00 ~ 155.00 MHz)	
		40mA (155.01 ~ 200.00 MHz)	35mA (155.01 ~ 200.00 MHz)	
Duty Cycle	Tw/t	40/60% (Std) & 45/55% available		Please specify
Output Level '0'	VOL	0.4Vdc max (TTL)	10% VDD max (HCMOS)	
Output Level '1'	VOH	2.4Vdc min (TTL)	90% VDD min (HCMOS)	
Rise & Fall Time (max)	TrTf	10nS (1.000 ~ 34.999 MHz)		
		5nS (35.00 ~ 99.999 MHz)		
		2.5nS (100.00 ~ 200.00 MHz)		
Output Load	N/CL	10TTL / 15pF (30pF available)		
Start-up Time	Tosc	10mS max		
Tri-state Input Voltage	No Connection	Enable output		
	VIH : ≥90% of VDD	Enable output		
	VIL : ≤10% of VDD	Disable output : High Impedance		
Ageing	Fa	±5ppm ±3ppm option	first year max @25°C	
Period Jitter (Absolute)	Tj	100pS max @ 1.0MHz	Other frequencies - see Note 2 below	
Period Jitter (one sigma)	Tj	25pS max @ 1.0MHz	Other frequencies - see Note 2 below	



Pad surface Material  
Au

### APPLICATIONS

- Microprocessor clock
- PDA / notebook
- Wireless applications
- Audio
- Gigabit ethernet
- Fibre channel
- Instrumentation

**NOTE1:** To reduce HF power supply noise, an external bypass capacitor of 0.01μF close to ground and Vdd is recommended.

**NOTE 2:** Typical (max) Jitter values in pS:

	RMS(1 sigma)	Absolute (PK-PK)
25MHz:	6.3 (10)	17.8 (28)
33MHz:	5.2 (10)	14.7 (28)
60MHz:	3.7 (5.0)	10.5 (14.0)
100MHz	1.0 (3.0)	2.8 (8.4)

Please note that all parameters can not necessarily be specified in the same device

Customer to Specify : Frequency, Frequency Stability, Operating Temperature Range, Output Type, Output enable, Voltage, Duty Cycle

In line with our ongoing policy of product evolution and improvement, the above specification is subject to change without notice

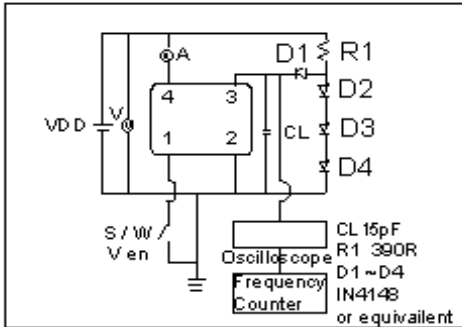
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<http://www.actcrystals.com>

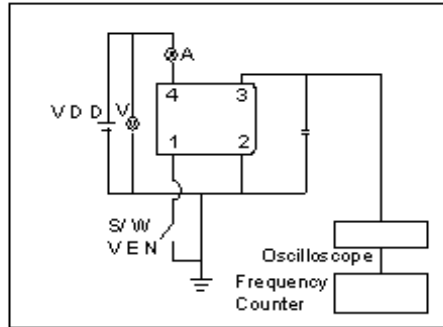
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## ACT9200L CIRCUIT DRAWINGS

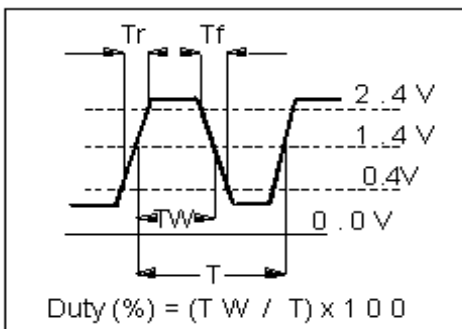
### TTL Test Circuit



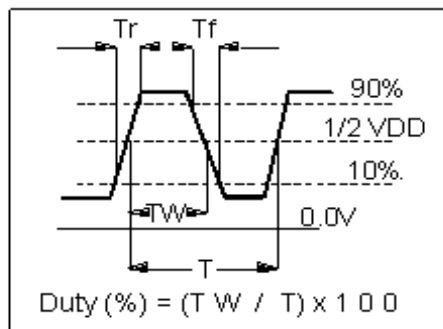
### CMOS Test Circuit



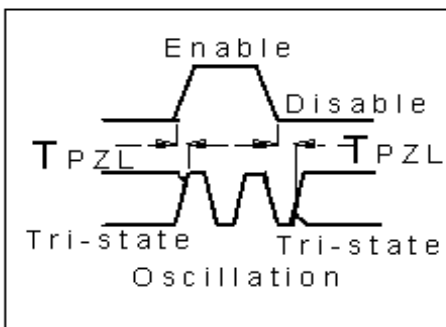
### TTL Waveform



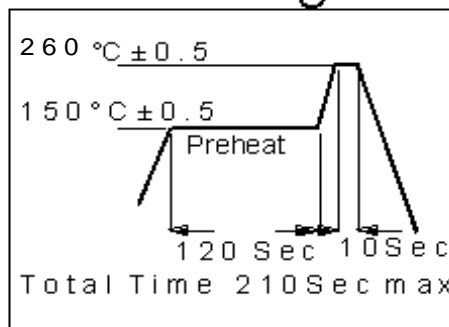
### CMOS Waveform



### Tristate Function



### Reflow Diagram



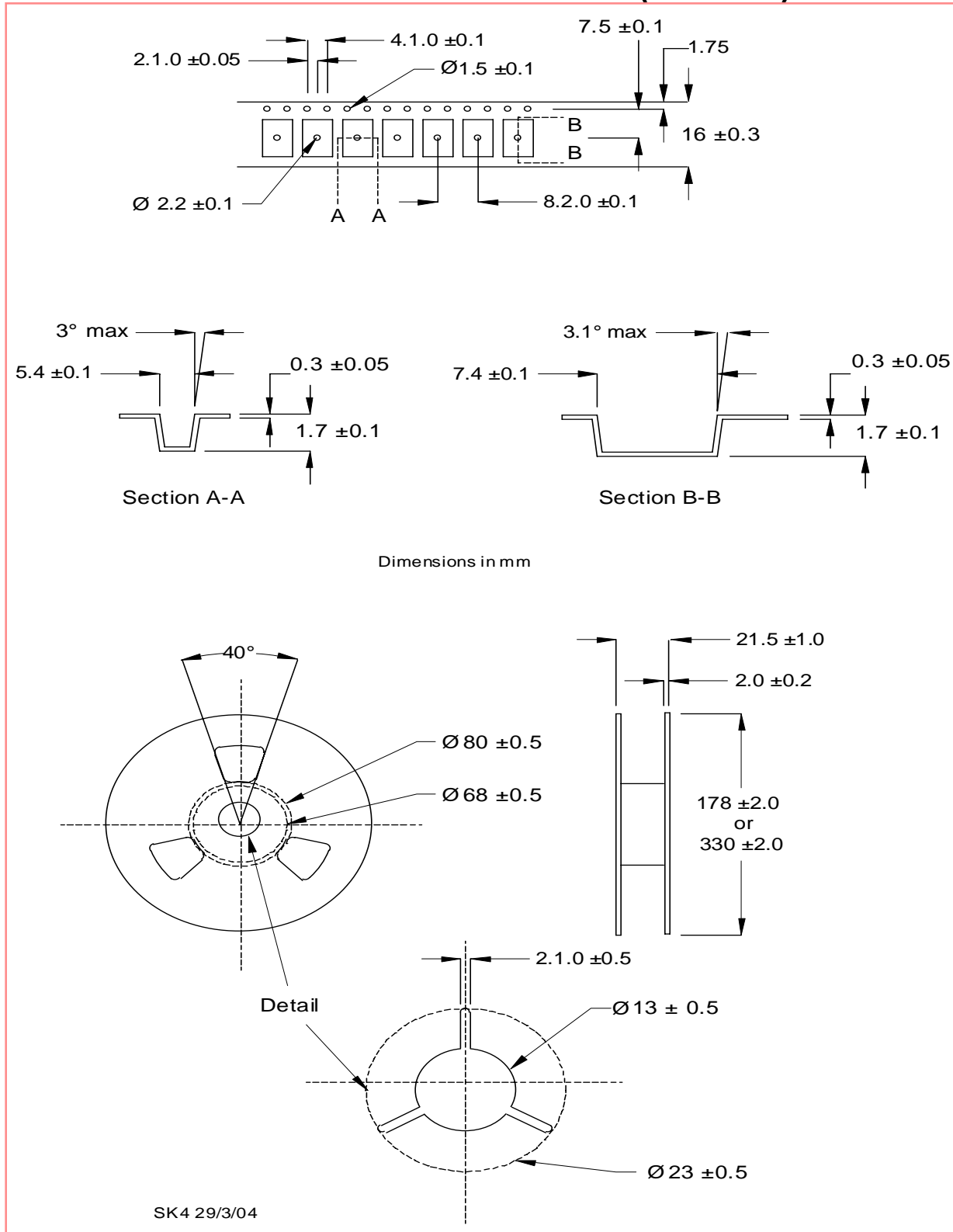
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## ACT9200L TAPE & REEL SPECIFICATIONS (1K Reels )



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