PRELIMINARY

Integrated Circuit Systems, Inc.

ICS8602

ZERO DELAY, DIFFERENTIAL-TO-LVCMOS/LVTTL CLOCK GENERATOR

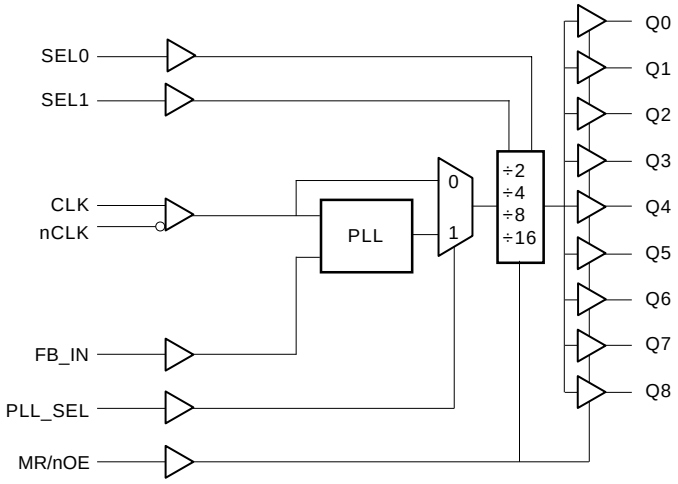
GENERAL DESCRIPTION

The ICS8602 is a high performance, low skew, 1-to-9 Differential-to-LVCMOS/LVTTL Zero Delay Buffer and a member of the HiPerClockS™ family of High Performance Clocks Solutions from ICS. The CLK, nCLK pair can accept most standard differential input levels. The VCO operates at a frequency range of 250MHz to 500MHz. The external feedback allows the device to achieve "zero delay" between the input clock and the output clocks. The device is designed only for 1:1 input/output frequency ratios. The output divider allows a wide input/output frequency range with the 250MHz to 500MHz VCO. The PLL_SEL pin can be used to bypass the PLL for system test and debug purposes. In bypass mode, the reference clock is routed around the PLL and into the internal output dividers.The low impedance LVCMOS/LVTTL outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be doubled by utilizing the ability of the outputs to drive two series terminated lines. The differential reference clock input will accept any differential signal levels.

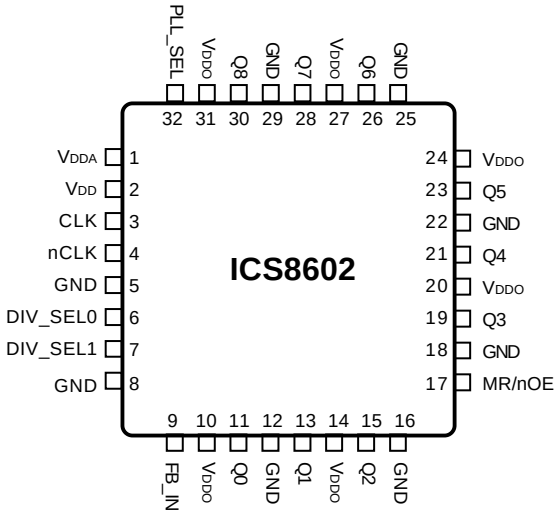
FEATURES

- Fully integrated PLL
- 9 LVCMOS/LVTTL outputs, 7Ω typical output impedance
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Output frequency range: 15.625MHz to 250MHz
- Input frequency range: 15.625MHz to 250MHz
- VCO range: 250MHz to 500MHz
- External feedback for "zero delay" clock regeneration with configurable frequencies
- Cycle-to-cycle jitter: 36ps (typical)
- Output skew: 125ps (maximum)
- Static Phase Offset: TBD±100ps (typical)
- 3.3V supply voltage
- 0°C to 70°C ambient operating temperature

BLOCK DIAGRAM



PIN ASSIGNMENT



32-Lead LQFP
7mm x 7mm x 1.4mm package body
Y Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	V_{DDA}	Power		Analog supply pin.
2	V_{DD}	Power		Core supply pin.
3	CLK	Input	Pulldown	Non-inverting differential clock input.
4	nCLK	Input	Pullup	Inverting differential clock input.
5, 8, 12 16, 18, 22, 25, 29	GND	Power		Power supply ground.
6, 7	DIV_SEL0, DIV_SEL1	Input	Pulldown	Determines output divider valued in Table 3. LVCMOS / LVTTL interface levels.
9	FB_IN	Input	Pulldown	Feedback input to phase detector for regenerating clocks with "zero delay". LVCMOS / LVTTL interface levels.
10, 14, 20, 24, 27, 31	V_{DDO}	Power		Output supply pins.
11, 13, 15, 19, 21, 23, 26, 28, 30	Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8	Output		Clock outputs. 7Ω typical output impedance. LVCMOS / LVTTL interface levels.
17	MR/nOE	Input	Pulldown	Active HIGH Master Reset. Active LOW output enable. When logic HIGH, the internal dividers are reset and the outputs are tri-stated (HiZ). When logic LOW, the internal dividers and the outputs are enabled. LVCMOS / LVTTL interface levels.
32	PLL_SEL	Input	Pullup	Selects between the PLL and the reference clock as the input to the dividers. When HIGH, selects PLL. When LOW, selects reference clock. LVCMOS / LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4	pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ
C_{PD}	Power Dissipation Capacitance (per output)	V_{DD}, V_{DDA}, V_{DDO} = 3.47V		TBD		pF
R_{OUT}	Output Impedance			7		Ω

TABLE 3A. CONTROL INPUT FUNCTION TABLE, PLL_SEL = 1

DIV_SEL1	DIV_SEL0	fOUT = fIN Frequency Range (MHz)	
		Minimum	Maximum
0	0	125	250
0	1	62.5	125
1	0	31.25	62.5
1	1	15.625	31.25

TABLE 3B. CONTROL INPUT FUNCTION TABLE, PLL_SEL = 0 PLL BYPASS MODE

DIV_SEL1	DIV_SEL0	Frequency Divider	
		fIN	fOUT
0	0	fIN	fIN/2
0	1	fIN	fIN/4
1	0	fIN	fIN/8
1	1	fIN	fIN/16

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	42.1°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			40		mA
I_{DDA}	Analog Supply Current			10		mA
I_{DDO}	Output Supply Current			160		mA

TABLE 4B. LVCMOS / LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	DIV_SEL0, DIV_SEL1, FB_IN, MR/nOE	$V_{DD} = V_{IN} = 3.465V$			150	µA
		PLL_SEL	$V_{DD} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	DIV_SEL0, DIV_SEL1, FB_IN, MR/nOE	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-5			µA
		PLL_SEL	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-150			µA
V_{OH}	Output High Voltage; NOTE 1			2.6			V
V_{OL}	Output Low Voltage; NOTE 1					0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{DDO}/2$. See Parameter Measurement Information, *3.3V Output Load Test Circuit.*

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK	$V_{DD} = V_{IN} = 3.465V$			150	µA
		nCLK	$V_{DD} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	CLK	$V_{DD} = 3.465$, $V_{IN} = 0V$	-5			µA
		nCLK	$V_{DD} = 3.465$, $V_{IN} = 0V$	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} - 0.85	V

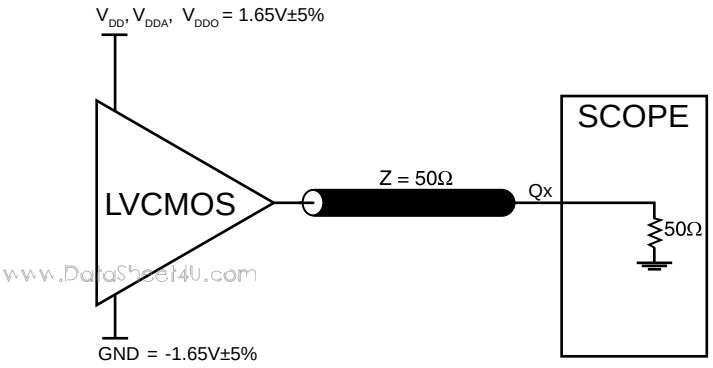
NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum voltage for CLK, nCLK is V_{DD} + 0.3V.

TABLE 5. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $70°C$

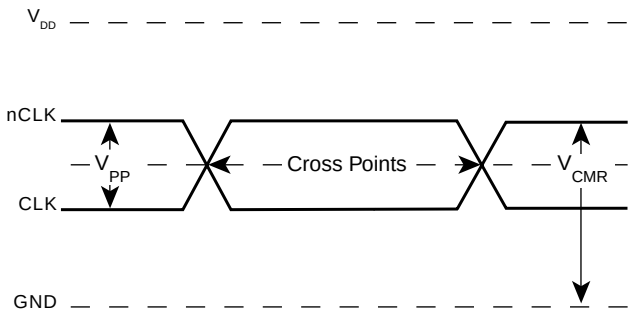
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency		15.625		250	MHz
tp_{LH}	Propagation Delay, Low-to-High; NOTE 1	PLL_SEL=0V, 0MHz ≤ f ≤ 250MHz	TBD		TBD	ns
t(Ø)	Static Phase Offset; NOTE 2	PLL_SEL = 3.3V, fREF = 133MHz, fVCO = 266MHz		TBD±100		ps
		PLL_SEL = 3.3V, fREF = 50MHz, fVCO = 100MHz		TBD±100		ps
*t*sk(o)	Output Skew; NOTE 3, 4	Measured on rising edge at $V_{DDO}/2$			125	ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 4	Measured on rising edge at $V_{DDO}/2$		36		ps
t_L	PLL Lock Time				1	ms
t_R	Output Rise Time	20% to 80% @ 50MHz	400		950	ps
t_F	Output Fall Time	20% to 80% @ 50MHz	400		950	ps
odc	Output Duty Cycle	f = 250MHz		50		%

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the output at $V_{DDO}/2$.
NOTE 2: Defined as the time difference between the input reference clock and the average feedback input signal when the PLL is locked and the input reference frequency is stable.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

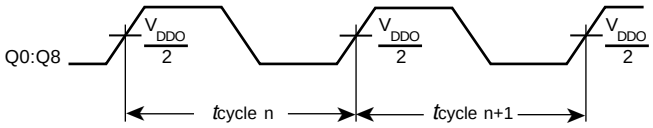
PARAMETER MEASUREMENT INFORMATION



3.3V OUTPUT LOAD AC TEST CIRCUIT



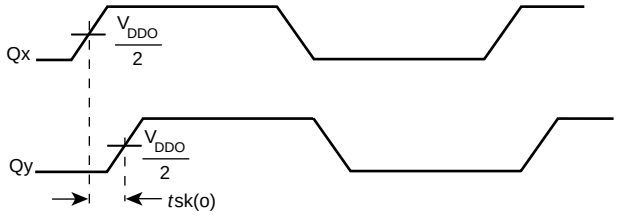
DIFFERENTIAL INPUT LEVEL



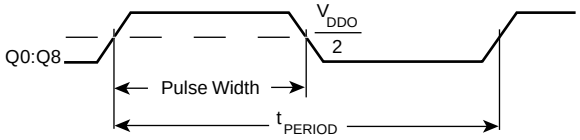
$t_{jit(cc)} = t_{cycle\ n} - t_{cycle\ n+1}$

1000 Cycles

CYCLE-TO-CYCLE JITTER

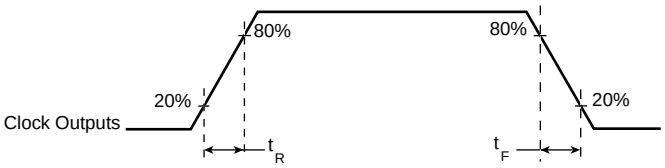


OUTPUT SKEW

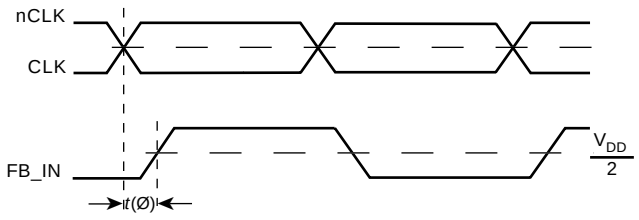


$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

odc & t_{PERIOD}



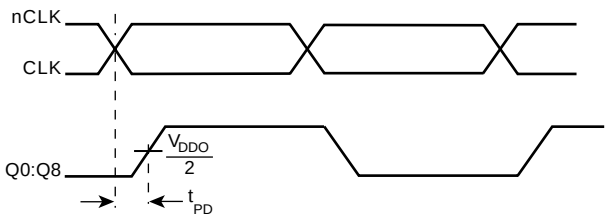
OUTPUT RISE/FALL TIME



$t(Ø)_{mean}$ = Static Phase Offset

(where $t(Ø)$ is any random sample, and $t(Ø)_{mean}$ is the average of the sampled cycles measured on controlled edges)

STATIC PHASE OFFSET



PROPAGATION DELAY

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

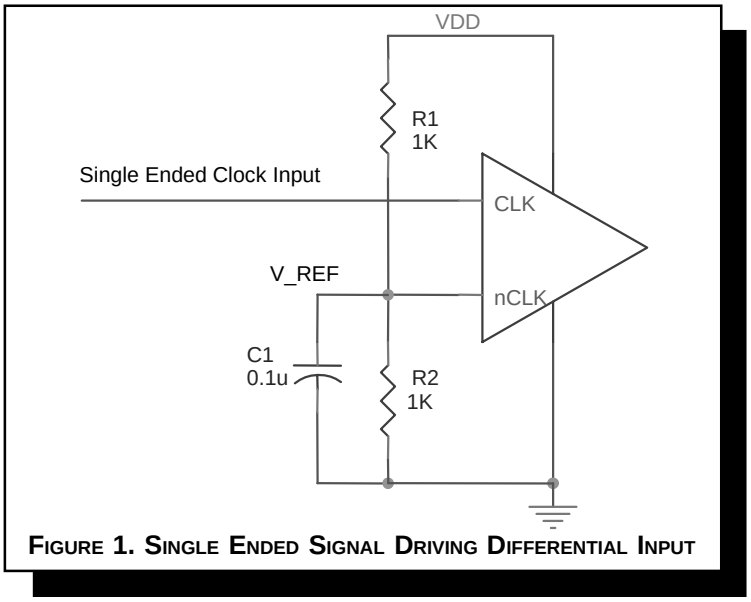


FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS8602 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, and V_{DDO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 2* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA} pin.

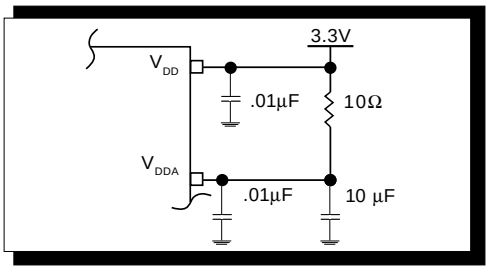


FIGURE 2. POWER SUPPLY FILTERING

DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 3A to 3D show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 3A,* the input termination applies for ICS HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

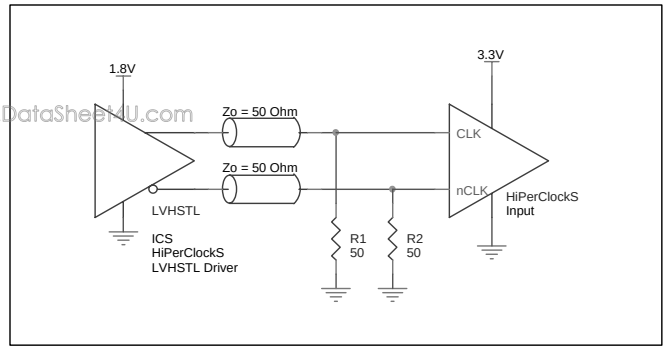


FIGURE 3A. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY ICS HIPERCLOCKS LVHSTL DRIVER

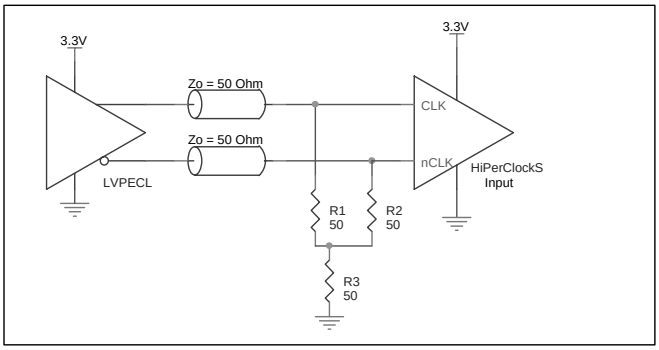


FIGURE 3B. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

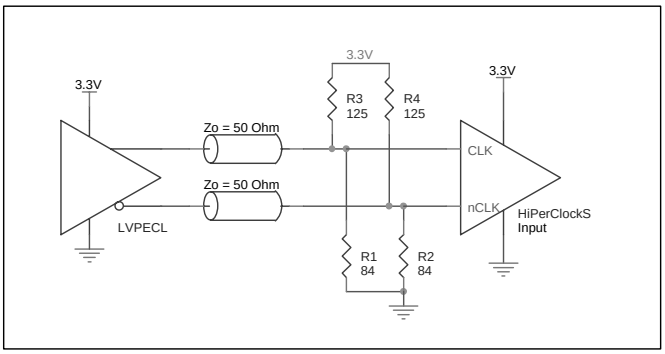


FIGURE 3C. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

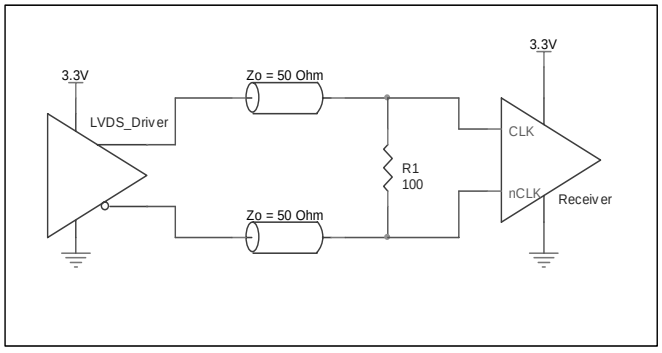


FIGURE 3D. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVDS DRIVER

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS8602 is: 1828

PACKAGE OUTLINE - Y SUFFIX

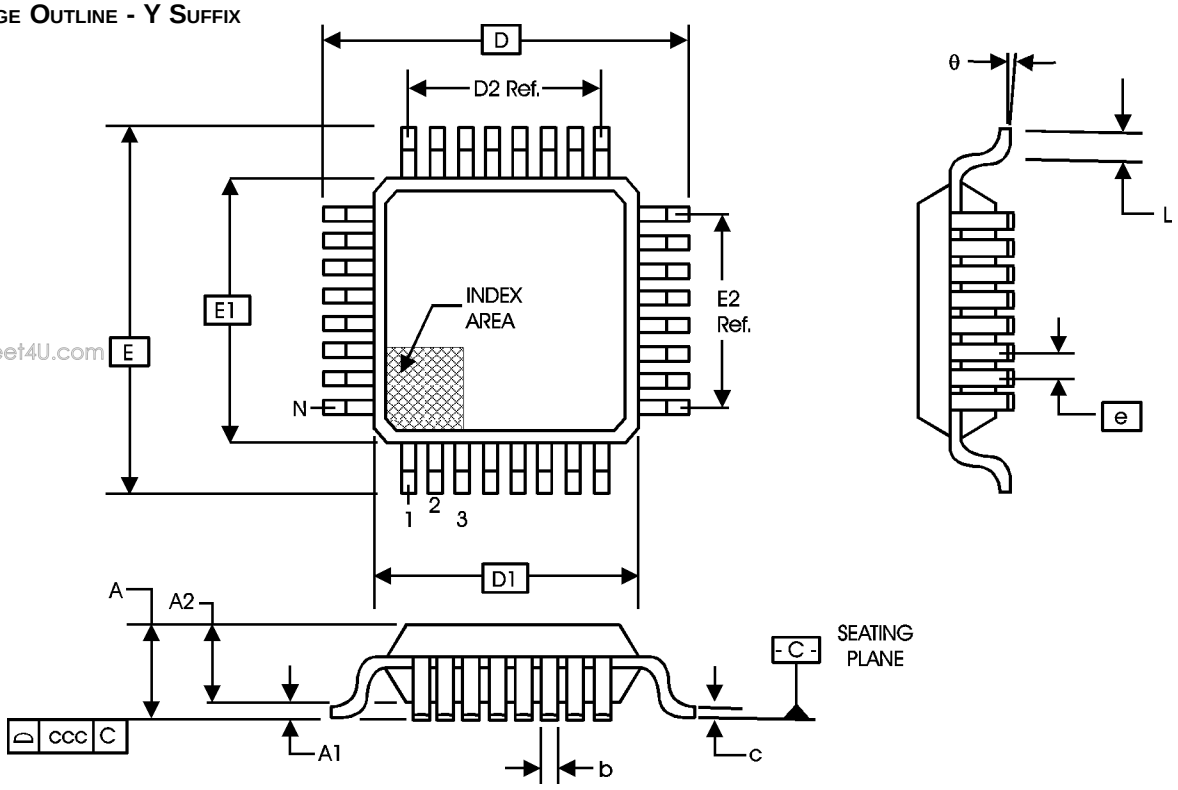


TABLE 7. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N		32	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.60 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.60 Ref.	
e		0.80 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.10

Reference Document: JEDEC Publication 95, MS-026

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS8602BY	ICS8602BY	32 Lead LQFP	250 per tray	0°C to 70°C
ICS8602BYT	ICS8602BY	32 Lead LQFP on Tape and Reel	1000	0°C to 70°C