T-45-23-05

National Semiconductor

54F/74F160A • 54F/74F162A
Synchronous Presettable BCD Decade Counter

General Description

The 'F160A and 'F162A are high-speed synchronous decade counters operating in the BCD (8421) sequence. They are synchronously presettable for applications in programmable dividers. There are two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The 'F160A has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. The 'F162A has a Synchronous Reset input that overrides counting and parallel loading and allows all outputs to be simultaneously reset on the rising edge of the clock. The 'F160A and 'F162A are high speed versions of the 'F160 and 'F162.

Features

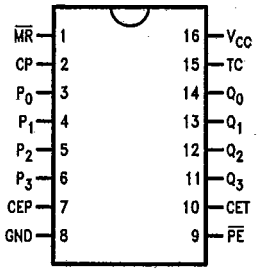
- Synchronous counting and loading
- High-speed synchronous expansion
- Typical count rate of 120 MHz
- Guaranteed 4000V minimum ESD protection

Ordering Code: See Section 5

Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak

'F160A



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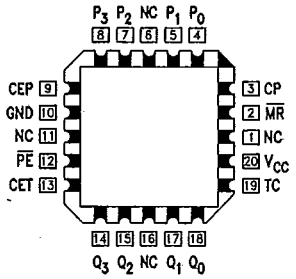
Pin Assignment for LCC

'F160A



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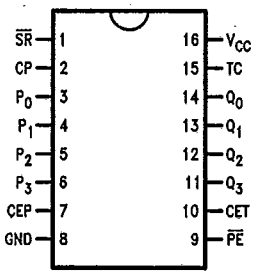
'F162A



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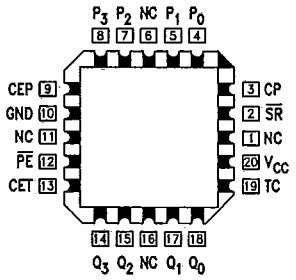
'F162A



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Logic Symbols

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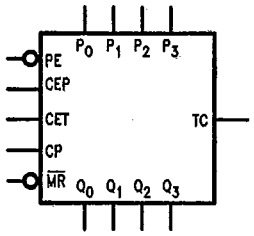

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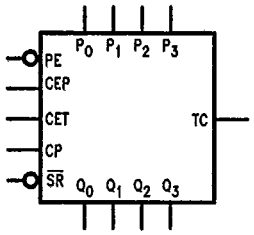
'F162A



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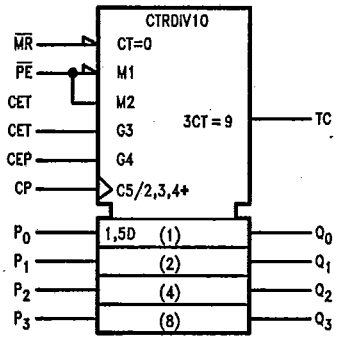
IEEE/IEC

'F160A



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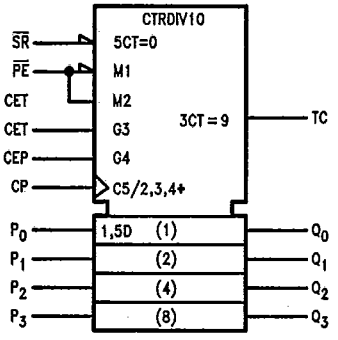
'F162A



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Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
CEP	Count Enable Parallel Input	1.0/1.0	20 μA/−0.6 mA
CET	Count Enable Trickle Input	1.0/2.0	20 μA/−1.2 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μA/−0.6 mA
$\overline{MR}$ ('F160A)	Asynchronous Master Reset Input (Active LOW)	1.0/1.0	20 μA/−0.6 mA
$\overline{SR}$ ('F162A)	Synchronous Reset Input (Active LOW)	1.0/2.0	20 μA/−1.2 mA
P_0–P_3	Parallel Data Inputs	1.0/1.0	20 μA/−0.6 mA
$\overline{PE}$	Parallel Enable Input (Active LOW)	1.0/2.0	20 μA/−1.2 mA
Q_0–Q_3	Flip-Flop Outputs	50/33.3	−1 mA/20 mA
TC	Terminal Count Output	50/33.3	−1 mA/20 mA

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Functional Description

The 'F160A and 'F162A count modulo-10 in the BCD (8421) sequence. From state 9 (HLLH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the ('F160A) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset ('F160A), synchronous reset ('F162A), parallel load, count-up and hold. Five control inputs—Master Reset ($\overline{MR}$, 'F160A), Synchronous Reset ($\overline{SR}$, 'F162A), Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET)—determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{MR}$ overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on $\overline{SR}$ overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{PE}$ and $\overline{MR}$ ('F160A) or $\overline{SR}$ ('F162A) HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The 'F160A and 'F162A use D-type edge-triggered flip-flops and changing the $\overline{SR}$, $\overline{PE}$, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is HIGH when CET is HIGH and counter is in state 9. To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. Please refer to the 'F568 data sheet. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers. In the 'F160A and 'F162A decade counters, the TC output is fully decoded and can only be HIGH in state 9. If a decade counter is preset to an illegal state, or assumes an illegal state when power is applied, it will return to the normal sequence within two counts, as shown in the State Diagram.

Logic Equations:

$$\text{Count Enable} = CEP \times CET \times \overline{PE}$$

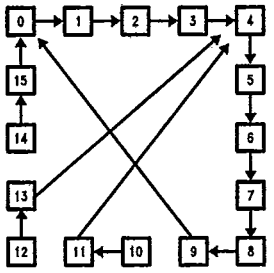
$$TC = Q_0 \times \overline{Q}_1 \times \overline{Q}_2 \times Q_3 \times CET$$

Mode Select Table

*$\overline{SR}$	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge (⌐‾)
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

*For 'F162A only
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

State Diagram



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Logic Diagram

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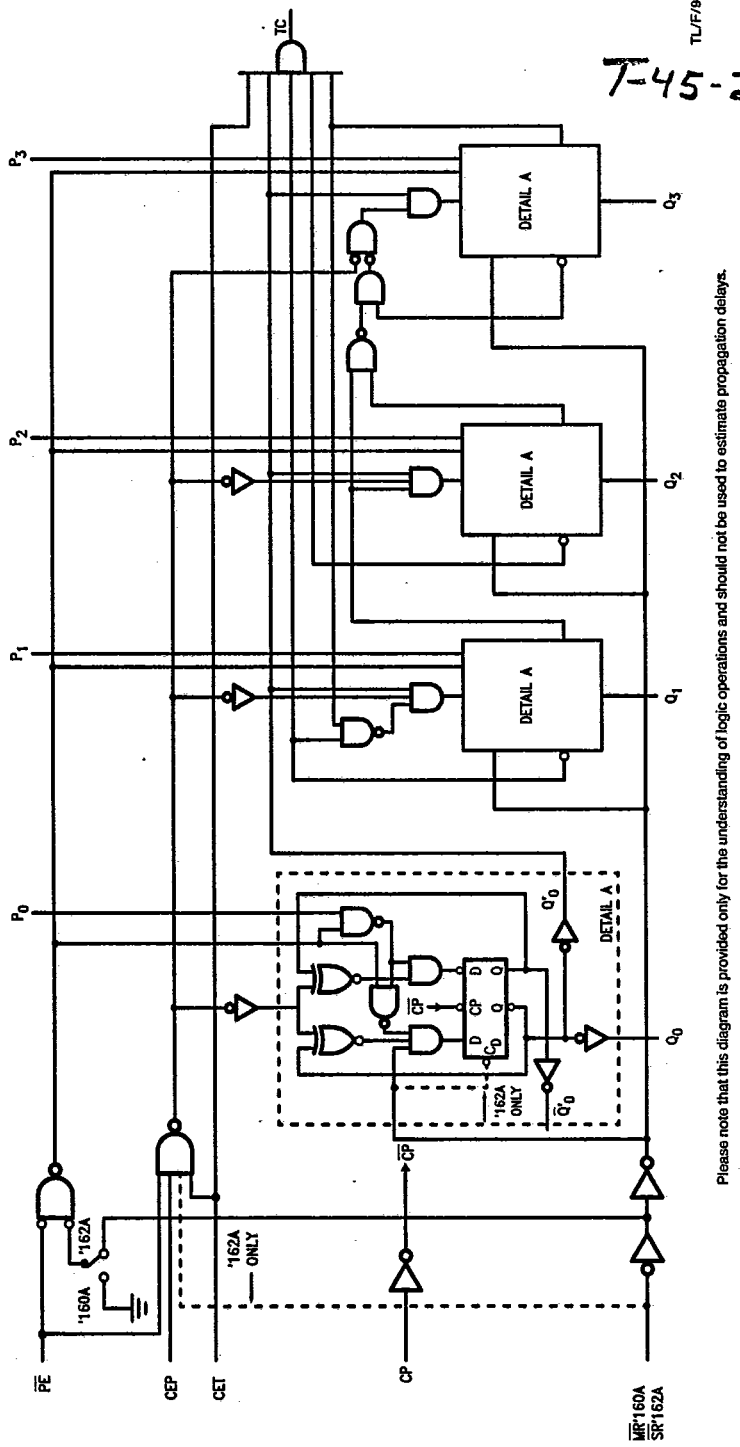

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE® Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

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Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		54F/74F Min	54F/74F Typ	54F/74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54F 10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
		74F 10% V_{CC}	2.5					I_{OH} = −1 mA
		74F 5% V_{CC}	2.7					I_{OH} = −1 mA
V_{OL}	Output LOW Voltage	54F 10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA
		74F 10% V_{CC}			0.5			I_{OL} = 20 mA
I_{IH}	Input HIGH Current	54F			20.0	μA	Max	V_{IN} = 2.7V
		74F			5.0			
I_{BVI}	Input HIGH Current Breakdown Test	54F			100	μA	Max	V_{IN} = 7.0V
		74F			7.0			
I_{CEX}	Output HIGH Leakage Current	54F			250	μA	Max	V_{OUT} = V_{CC}
		74F			50			
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V (CP, CEP, P_n, $\overline{MR}$ ('F160A))
					−1.2	mA	Max	V_{IN} = 0.5V (CET, $\overline{SR}$ ('F162A), $\overline{PE}$)
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{CC}	Power Supply Current			37	55	mA	Max	V_O = HIGH

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50\ pF$			54F $T_A, V_{CC} = Mil$ $C_L = 50\ pF$		74F $T_A, V_{CC} = Com$ $C_L = 50\ pF$		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Count Frequency	90	120		75		80		MHz	2–1
t_{PLH} t_{PHL}	Propagation Delay, Count CP to Q_n ($\overline{PE}$ Input HIGH)	3.5 3.5	5.5 7.5	7.5 10.0	3.5 3.5	9.0 11.5	3.5 3.5	8.5 11.0	ns	2–3
t_{PLH} t_{PHL}	Propagation Delay, Load CP to Q_n ($\overline{PE}$ Input LOW)	4.0 4.0	6.0 6.0	8.5 8.5	4.0 4.0	10.0 10.0	4.0 4.0	9.5 9.5	ns	2–3
t_{PLH} t_{PHL}	Propagation Delay CP to TC	5.0 5.0	10.0 10.0	14.0 14.0	5.0 5.0	16.5 15.5	5.0 5.0	15.0 15.0	ns	2–3
t_{PLH} t_{PHL}	Propagation Delay CET to TC	2.5 2.5	4.5 4.5	7.5 7.5	2.5 2.5	9.0 9.0	2.5 2.5	8.5 8.5	ns	2–3
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n ('F160A)	5.5	9.0	12.0	5.5	14.0	5.5	13.0	ns	2–3
t_{PHL}	Propagation Delay $\overline{MR}$ to TC ('F160A)	4.5	8.0	10.5	4.5	12.5	4.5	11.5	ns	2–3

AC Operating Requirements: See Section 2 for Waveforms

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Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$ Min	74F $T_A = +25°C$ $V_{CC} = +5.0V$ Max	54F T_A, V_{CC} = Mil Min	54F T_A, V_{CC} = Mil Max	74F T_A, V_{CC} = Com Min	74F T_A, V_{CC} = Com Max	Units	Fig. No.
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW P_n to CP ('F160A)	4.0 5.0		5.5 5.5		4.0 5.0		ns	2-6
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW P_n to CP ('F162A)	5.0 5.0		5.5 5.5		5.0 5.0		ns	2-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW P_n to CP	2.0 2.0		2.5 2.5		2.0 2.0			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	11.0 8.5		13.5 10.5		11.5 9.5		ns	2-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	2.0 0		2.0 0		2.0 0			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW CEP or CET to CP	11.0 5.0		13.0 6.0		11.5 5.0		ns	2-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW CEP or CET to CP	0 0		0 0		0 0			
$t_w(H)$ $t_w(L)$	Clock Pulse Width (Load) HIGH or LOW	5.0 5.0		5.0 5.0		5.0 5.0		ns	2-4
$t_w(H)$ $t_w(L)$	Clock Pulse Width (Count) HIGH or LOW	4.0 6.0		5.0 8.0		4.0 7.0		ns	2-4
$t_w(L)$	$\overline{MR}$ Pulse Width, LOW ('F160A)	5.0		5.0		5.0			
t_{rec}	Recovery Time $\overline{MR}$ to CP ('F160A)	6.0		6.0		6.0		ns	2-6