

# AZP92

## PECL/ECL $\div 1$ , $\div 2$ Clock Generation Chip with Selectable Enable

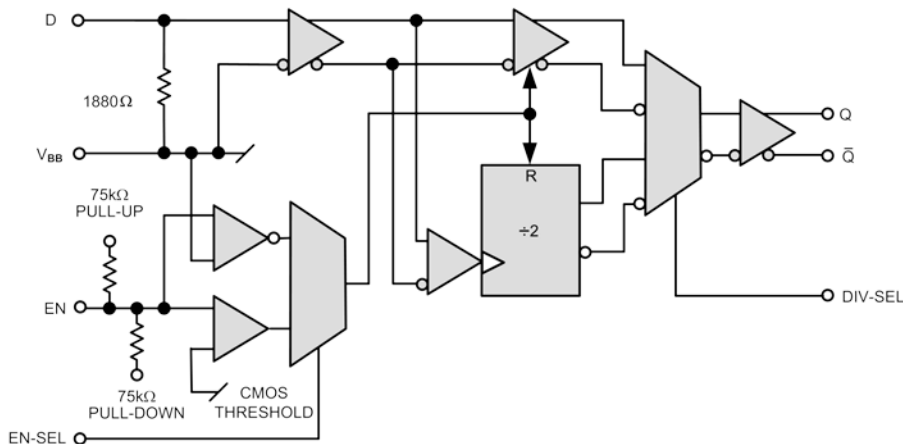
[www.azmicrotek.com](http://www.azmicrotek.com)

### DESCRIPTION

The [AZP92](#) is a  $\div 1$  or  $\div 2$  clock generation part specifically designed to accommodate Colpitts or Pierce based oscillators. Features are incorporated to reduce board components. A voltage reference and input biasing allows for easy oscillator interface.

The AZP92 provides a  $\div 2$  mode of operation for more frequency options and is selectable with a single connection. A selectable enable is also provided which doubles as a reset when the AZP92 is in  $\div 2$  mode. With a single connection, the enable can be selected to operate as active high or active low.

### BLOCK DIAGRAM



### FEATURES

- 3.0V to 5.5V Operation
- Selectable Divide Ratio
- Selectable Enable Polarity and Threshold (CMOS or PECL)
- High Bandwidth
  - 1.5+ GHz ( $\div 1$ )
  - 3.0+ GHz ( $\div 2$ )
- -145 dBc/Hz ( $\div 1$ ) Typical Noise Floor
- -151 dBc/Hz ( $\div 2$ ) Typical Noise Floor

### APPLICATIONS

- Colpitts or Pierce based oscillators

### PACKAGE AVAILABILITY

- MLP8
  - Green/RoHS Compliant/Pb-Free

Part Number (PN)	Package	Marking
AZP92NAG <sup>1</sup>	MLP8	PIG <Date Code> <sup>2</sup>

<sup>1</sup> [Tape & Reel](#) - Add 'R1' at end of PN for 7in (1k parts), 'R2' (2.5k) for 13in

<sup>2</sup> See [www.azmicrotek.com](http://www.azmicrotek.com) for [date code format](#)



## ENGINEERING NOTES

The AZP92's divide ratio is selected with the DIV-SEL pin. When DIV-SEL is open (NC), the AZP92 functions as a standard receiver. When the DIV-SEL is connected to  $V_{EE}$ , it functions as a  $\div 2$  divider. In  $\div 2$  mode, the latches reset to a logic 0 level when disabled.

The Enable (EN) functionality is selected with the EN-SEL pin which has three valid states: open (NC),  $V_{EE}$ , or connected to  $V_{EE}$  via a 20k $\Omega$  resistor. Leaving EN-SEL open or connecting it to  $V_{EE}$  will select the EN pin to function as an active high CMOS/TTL enable. When EN-SEL is open, an internal 75k $\Omega$  pull-up resistor is selected which enables the outputs whenever EN is left open. When EN-SEL is connected to  $V_{EE}$ , an internal 75k $\Omega$  pull-down resistor is selected which disables the outputs whenever EN is left open. Connecting the EN-SEL to  $V_{EE}$  with a 20k $\Omega$  resistor will select the EN pin to function as an active low PECL/ECL enable with an internal 75k $\Omega$  pull-down resistor. In this mode, outputs are enabled when EN is left open. This default logic condition can be overridden by connecting the EN to  $V_{CC}$  with an external resistor of  $\leq 20k\Omega$ .

**Table 2 - Divide Truth Table**

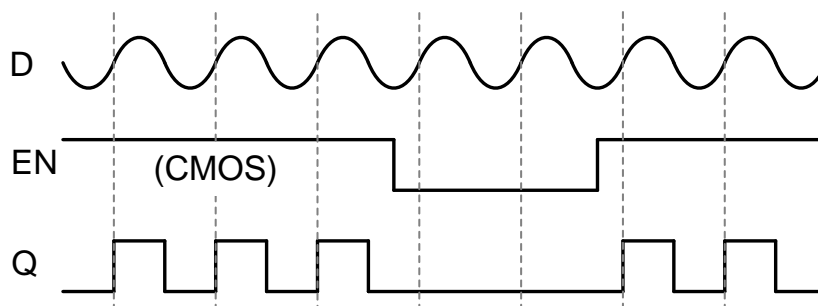
DIV-SEL	$\div$ Ratio
NC	$\div 1$
$V_{EE}$ <sup>1</sup>	$\div 2$

<sup>1</sup> DIV-SEL connection must be  $\leq 1\Omega$ .

**Table 3 - Enable Truth Table**

EN-SEL	EN	Q	Q
NC	CMOS Low or $V_{EE}$	Low	High
	CMOS High, $V_{CC}$ or NC	Data	Data
$V_{EE}$	CMOS Low, $V_{EE}$ or NC	Low	High
	CMOS High or $V_{CC}$	Data	Data
20k $\Omega$ to $V_{EE}$	PECL Low, $V_{EE}$ or NC	Low	High
	PECL High or $V_{CC}$	Data	Data

Figure 2 illustrates the timing sequences for the AZP92 in the  $\div 1$  mode which is determined by leaving the DIV-SEL open (NC). It also illustrates the enable in the active High mode being controlled by a CMOS signal. This mode is determined by leaving the EN-SEL open (NC).



**Figure 2 - Timing Diagram**

Figure 3 illustrates the timing sequences for the AZP92 in the ÷2 mode which is determined by connecting the DIV-SEL to V<sub>EE</sub>. It also illustrates the enable in the active Low mode being controlled by a PECL signal. This mode is determined by connecting the EN-SEL to V<sub>EE</sub> via 20kΩ resistor.

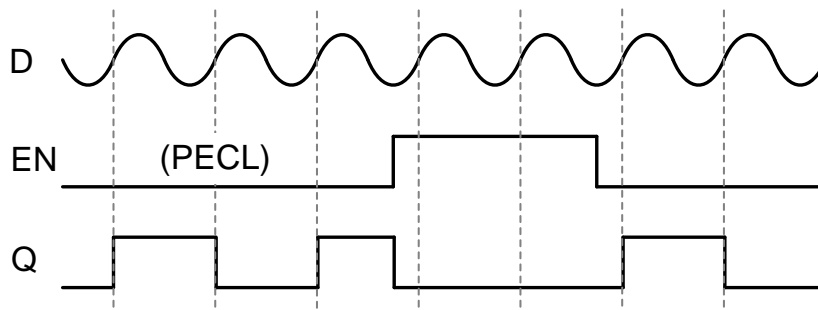


Figure 3 - Timing Diagram

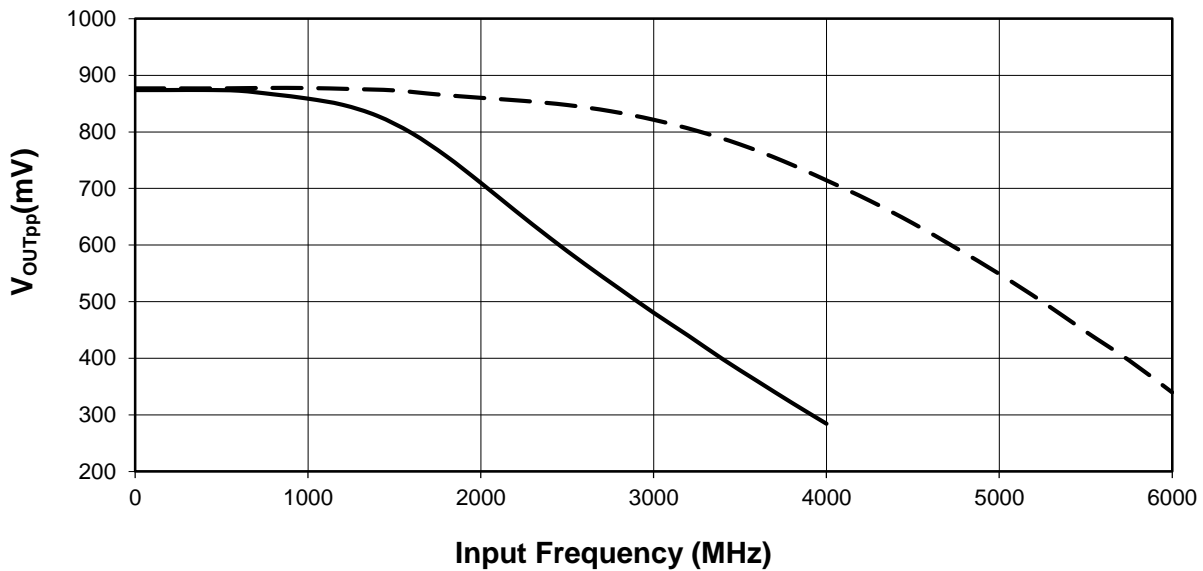


Figure 4 - Typical Large Signal Output Swing

Measured with 750mv D input, Q/Q each terminated to V<sub>CC</sub>-2V via 50 Ω resistors

**PERFORMANCE DATA**

Table 4 - Absolute Maximum Ratings

Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Characteristic	Condition	Rating	Unit
V <sub>CC</sub>	Power Supply	V <sub>EE</sub> = 0V	0 to + 6.0	V
V <sub>I</sub>	Input Voltage	V <sub>EE</sub> = 0V	0 to + 6.0	V
V <sub>D/D</sub>	D/D Input Voltage	Referenced to V <sub>BB</sub>	±1.2	V
I <sub>OUT</sub>	Output Current	Continuous	50	mA
		Surge	100	
T <sub>A</sub>	Operating Temperature Range	-	-40 to +85	°C
T <sub>STG</sub>	Storage Temperature Range	-	-65 to +150	°C
ESD <sub>HBM</sub>	Human Body Model Electro Static Discharge	-	2500	V
ESD <sub>MM</sub>	Machine Model Electro Static Discharge	-	200	V
ESD <sub>CDM</sub>	Charged Device Model Electro Static Discharge	-	2000	V

Table 5 - 100K ECL DC Characteristics

100K ECL DC Characteristics (V<sub>EE</sub> = -3.0V to -5.5V, V<sub>CC</sub> = GND)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V <sub>OH</sub>	Output HIGH Voltage <sup>1</sup>	-1085	-880	-1025	-880	-1025	-880	-1025	-880	mV
V <sub>OL</sub>	Output LOW Voltage <sup>1</sup>	-1900	-1555	-1900	-1620	-1900	-1620	-1900	-1620	mV
V <sub>BB</sub>	Reference Voltage	-1390	-1250	-1390	-1250	-1390	-1250	-1390	-1250	mV
V <sub>IH</sub>	Input HIGH Voltage D/EN <sup>2</sup>	-1165	-390	-1165	-390	-1165	-390	-1165	-390	mV
	Input HIGH Voltage EN <sup>3</sup>	V <sub>EE</sub> + 2000	V <sub>CC</sub>	V <sub>EE</sub> + 2000	V <sub>CC</sub>	V <sub>EE</sub> + 2000	V <sub>CC</sub>	V <sub>EE</sub> + 2000	V <sub>CC</sub>	mV
V <sub>IL</sub>	Input LOW Voltage D/EN <sup>2</sup>	-2250	-1475	-2250	-1475	-2250	-1475	-2250	-1475	mV
	Input LOW Voltage EN <sup>3</sup>	V <sub>EE</sub>	V <sub>EE</sub> + 800	V <sub>EE</sub>	V <sub>EE</sub> + 800	V <sub>EE</sub>	V <sub>EE</sub> + 800	V <sub>EE</sub>	V <sub>EE</sub> + 800	mV
I <sub>IH</sub>	Input HIGH Current EN		150		150		150		150	µA
I <sub>IL</sub>	Input LOW Current EN (ECL)	0.5		0.5		0.5		0.5		µA
I <sub>EE</sub>	Power Supply Current <sup>4</sup>		31		31		31		34	mA

1. Specified with outputs terminated through 50Ω resistors to V<sub>CC</sub> - 2V.
2. EN-SEL connected to V<sub>EE</sub> through a 20kΩ resistor.
3. EN-SEL connected V<sub>EE</sub> or left open (NC).
4. DIV-SEL left open (NC).

Table 6 - 100K LVPECL DC Characteristics

100K LVPECL DC Characteristics ( $V_{EE} = \text{GND}$ ,  $V_{CC} = +3.3\text{V}$ )

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$V_{OH}$	Output HIGH Voltage <sup>1,2</sup>	-1085	-880	-1025	-880	-1025	-880	-1025	-880	mV
$V_{OL}$	Output LOW Voltage <sup>1,2</sup>	-1900	-1555	-1900	-1620	-1900	-1620	-1900	-1620	mV
$V_{BB}$	Reference Voltage <sup>1</sup>	-1390	-1250	-1390	-1250	-1390	-1250	-1390	-1250	mV
$V_{IH}$	Input HIGH Voltage D <sup>1,3</sup>	-1165	-390	-1165	-390	-1165	-390	-1165	-390	mV
	Input HIGH Voltage EN <sup>1,4</sup>	-1165	$V_{CC}$	-1165	$V_{CC}$	-1165	$V_{CC}$	-1165	$V_{CC}$	mV
$V_{IL}$	Input LOW Voltage <sup>1,3</sup>	-2250	-1475	-2250	-1475	-2250	-1475	-2250	-1475	mV
	Input LOW Voltage EN <sup>1,4</sup>	$V_{EE}$	-1475	$V_{EE}$	-1475	$V_{EE}$	-1475	$V_{EE}$	-1475	mV
$I_{IH}$	Input HIGH Current EN		150		150		150		150	$\mu\text{A}$
$I_{IL}$	Input LOW Current EN (ECL)	0.5		0.5		0.5		0.5		$\mu\text{A}$
$I_{EE}$	Power Supply Current <sup>2</sup>		31		31		31		34	mA

1. For supply voltages other than 3.3V, use the ECL table values and ADD supply voltage value.
2. Specified with outputs terminated through 50 $\Omega$  resistors to  $V_{CC} - 2\text{V}$ .
3. EN-SEL connected to  $V_{EE}$  through a 20k $\Omega$  resistor.
4. EN-SEL connected  $V_{EE}$  or left open (NC).
5. DIV-SEL left open (NC).

Table 7 - 100K PECL DC Characteristics

100K PECL DC Characteristics ( $V_{EE} = \text{GND}$ ,  $V_{CC} = +5.0\text{V}$ )

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$V_{OH}$	Output HIGH Voltage <sup>1,2</sup>	-1085	-880	-1025	-880	-1025	-880	-1025	-880	mV
$V_{OL}$	Output LOW Voltage <sup>1,2</sup>	-1900	-1555	-1900	-1620	-1900	-1620	-1900	-1620	mV
$V_{BB}$	Reference Voltage <sup>1</sup>	-1390	-1250	-1390	-1250	-1390	-1250	-1390	-1250	mV
$V_{IH}$	Input HIGH Voltage D <sup>1,3</sup>	-1165	-390	-1165	-390	-1165	-390	-1165	-390	mV
	Input HIGH Voltage EN <sup>1,4</sup>	-1165	$V_{CC}$	-1165	$V_{CC}$	-1165	$V_{CC}$	-1165	$V_{CC}$	mV
$V_{IL}$	Input LOW Voltage <sup>1,3</sup>	-2250	-1475	-2250	-1475	-2250	-1475	-2250	-1475	mV
	Input LOW Voltage EN <sup>1,4</sup>	$V_{EE}$	-1475	$V_{EE}$	-1475	$V_{EE}$	-1475	$V_{EE}$	-1475	mV
$I_{IH}$	Input HIGH Current EN		150		150		150		150	$\mu\text{A}$
$I_{IL}$	Input LOW Current EN (ECL)	0.5		0.5		0.5		0.5		$\mu\text{A}$
$I_{EE}$	Power Supply Current <sup>2</sup>		31		31		31		34	mA

1. For supply voltages other than 5.0V, use the ECL table values and ADD supply voltage value.
2. Specified with outputs terminated through 50 $\Omega$  resistors to  $V_{CC} - 2\text{V}$ .
3. EN-SEL connected to  $V_{EE}$  through a 20k $\Omega$  resistor.
4. EN-SEL connected  $V_{EE}$  or left open (NC).
5. DIV-SEL left open (NC).

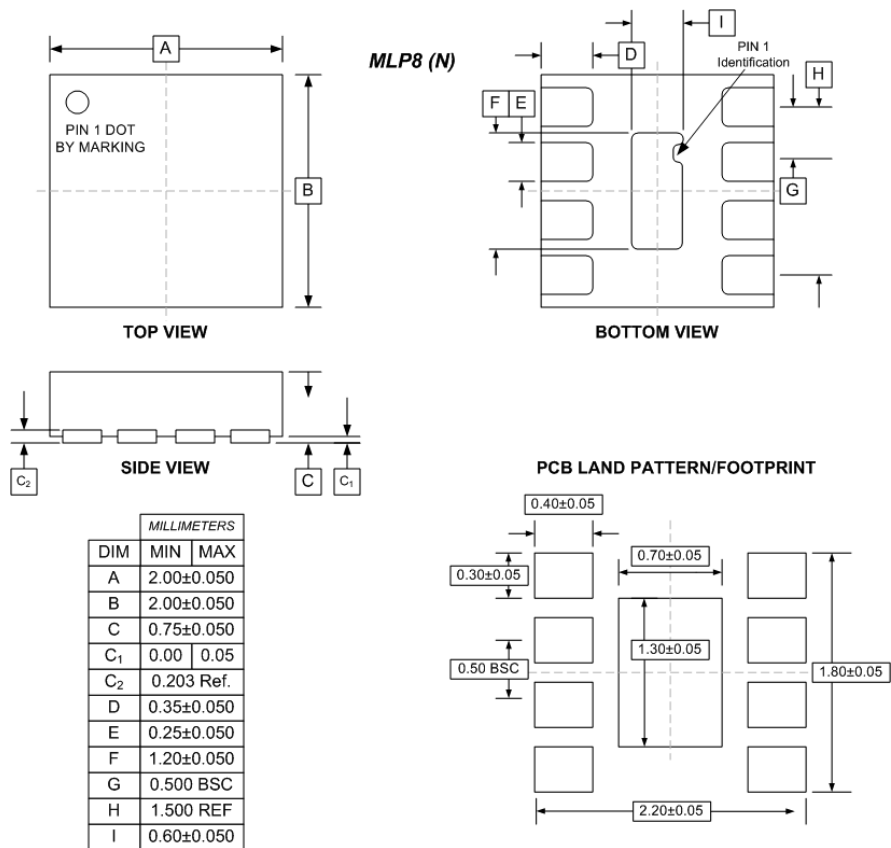
Table 8 - AC Characteristics

AC Characteristics ( $V_{EE} = -3.0V$  to  $-5.5V$ ;  $V_{CC}=GND$  or  $V_{EE}=GND$ ;  $V_{CC} = +3.0V$  to  $+5.5V$ )

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$t_{PLH}/t_{PHL}$	Propagation Delay													
	D to Q <sup>1</sup>			450			450			450			450	ps
	EN to Q <sup>1</sup>			600			600			600			600	ps
$t_{SKEW}$	Duty Cycle Skew <sup>2</sup>		5	20		5	20		5	20		5	20	ps
$V_{PP}$ (AC)	Input Swing <sup>3</sup>													
	Differential	150		1000	150		1000	150		1000	150		1000	mV
	Single Ended <sup>4</sup>	300		2000	300		2000	300		2000	300		2000	mV
$t_r/t_f$	Output Rise/Fall <sup>1</sup> (20%-80%)	80		200	80		200	80		200	80		200	ps

1. Specified with outputs terminated through 50Ω resistors to  $V_{CC} - 2V$ .
2. Duty cycle skew is the difference between a  $t_{PLH}$  and  $t_{PHL}$  propagation delay through a device.
3. The peak-to-peak input swing is the range for which AC parameters are guaranteed.
4. Range valid for AC coupled signals only.

**PACKAGE DIAGRAM**  
MLP8  
Green/RoHS compliant/Pb-Free  
MSL=1



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