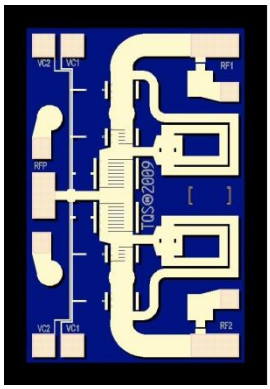
TGS2351

DC – 6 GHz High Power SPDT Switch

Applications

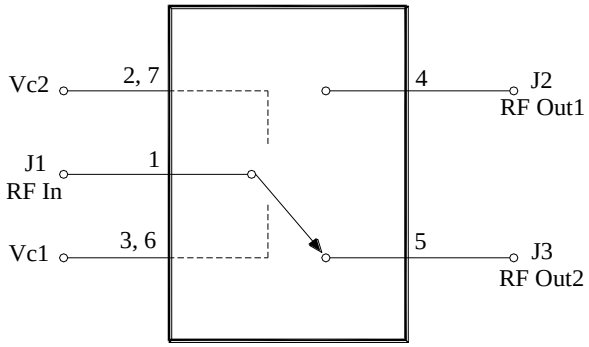
- High Power Switching



Product Features

- Frequency Range: DC – 6 GHz
- Power Handling: up to 40 W
- Insertion Loss: < 0.8 dB
- Isolation: -40 dB typical
- Switching Speed: < 15 ns
- Control Voltages: 0 V/-40 V from either side of MMIC
- Dimensions: 1.15 x 1.65 x 0.1 mm

Functional Block Diagram



General Description

The TriQuint TGS2351 is a Single-Pole, Double-Throw (SPDT) Switch. The TGS2351 operates from DC to 6 GHz and is designed using TriQuint's 0.25um GaN on SiC production process.

The TGS2351 typically provides up to 40 W input power handling at control voltages of 0/-40 V. This switch maintains low insertion loss < 0.8 dB, and high isolation -40 dB typical.

The TGS2351 is ideally suited for High Power Switching application.

Lead-free and RoHS compliant

Evaluation Boards are available upon request.

Bond Pad Configuration

Bond Pad #	Symbol
1	RF In
2, 7	Vc2
3, 6	Vc1
4	RF Out1
5	RF Out2

Ordering Information

Part No.	ECCN	Description
TGS2351	EAR99	DC – 6 GHz High Power SPDT Switch

Specifications

Absolute Maximum Ratings

Parameter	Rating
Control Voltage, Vc	- 50 V
Control Current, Ic	-1 to 7.8 mA
Power Dissipation, Pdiss	10 W
RF Input Power, CW, 50Ω,T = 25ºC	47 dBm
RF Input Power, Hot Switching, 50% switching Duty Cycle	40 dBm
Channel Temperature, Tch	275 °C
Mounting Temperature (30 Seconds)	320 °C
Storage Temperature	-55 to 150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Min	Typical	Max	Units
Vc1		-40 / 0		V
Vc2		0 / -40		V
Ic1 / Ic2		-0.4 to 0.1		mA

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: 25ºC, Vc1 = -40/0 V, Vc2 = 0/-40 V, see Function Table at Application Circuit on page 6.

Parameter	Min	Typical	Max	Units
Operational Frequency Range	DC		6	GHz
Control Current (Ic1/ Ic2)	-1		0.1	mA
Insertion Loss (On-State): DC to 6 GHz		0.5	1	dB
Input Return Loss – On-State (Common Port RL)	12	20		dB
Output Return Loss – On-State (Switched Port RL)	12	20		dB
Isolation (Off-State)		-40	-31	dB
Output Return Loss – Off-Sate (Isolated Port RL)		2.5		dB
Input Power [1/]		46		dBm
Output Power @ Pin = 46dBm, 1-6GHz	44.5	45	46	dBm
Insertion Loss Temperature Coefficient		-0.003		dB/°C
Output TOI @ Pin = 23 dBm		50		dBm
Switching Speed – On [2/]		15		ns
Switching Speed – Off [2/]		15		ns

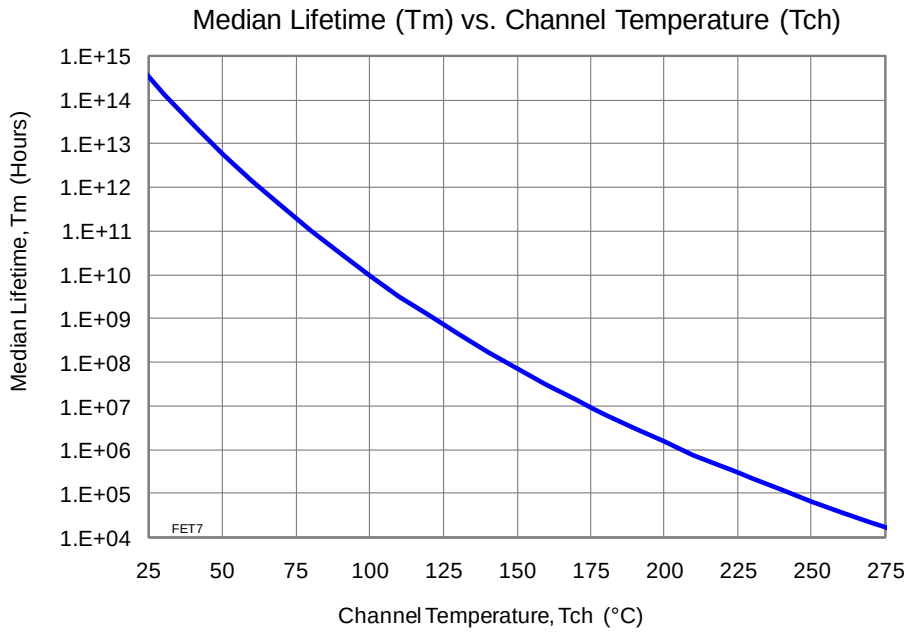
1/ The Input Power will be reduced if < 10 MHz.

2/ These Switching Speed dependent on Switch Driver circuit to deliver Vc = 0/-40 V. The rise and fall time of the Switch Driver which was used to perform for this data is 35 ns, as shown on page 5. For further technical information, see GaN SPDT Switch Drivers Application Note

Specifications (cont.)

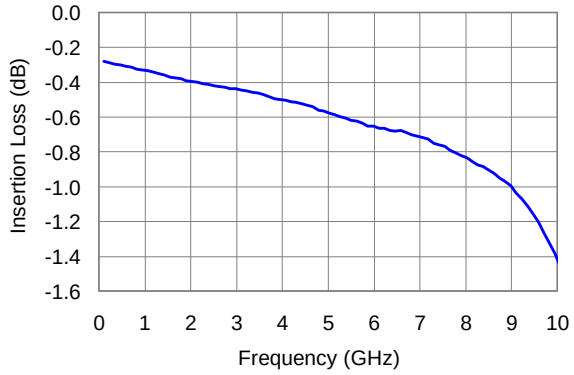
Thermal and Reliability Information

Parameter	Condition	Rating
Thermal Resistance, θ_{JC}, measured to back of carrier (die mounted to a 20 mil CuMo carrier using 1.5 mil 80/20 AuSn)	Tbase = 70 °C	θ_{JC} = 6.1 °C/W
Channel Temperature (Tch), and Median Lifetime (Tm)	Tbase = 70 °C, Vc1 = 0 V, Vc2 = -40 V, Pin = 40 W, Pdiss = 5.3 W	Tch = 102.5 °C Tm = 7.2 E+9 Hours

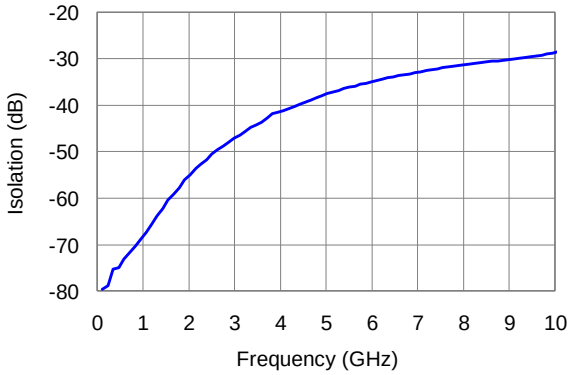


Typical Performance

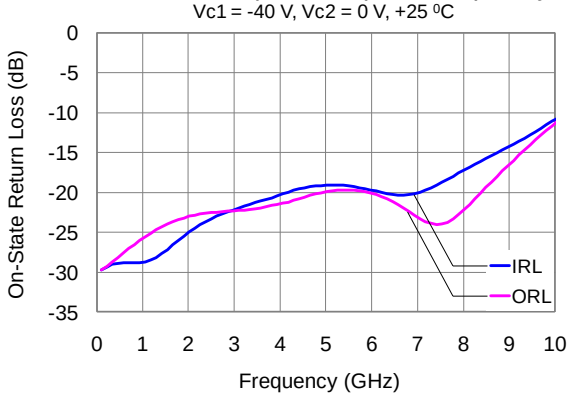
Insertion Loss (On-State) vs. Frequency
Vc1 = -40 V, Vc2 = 0 V, +25 °C



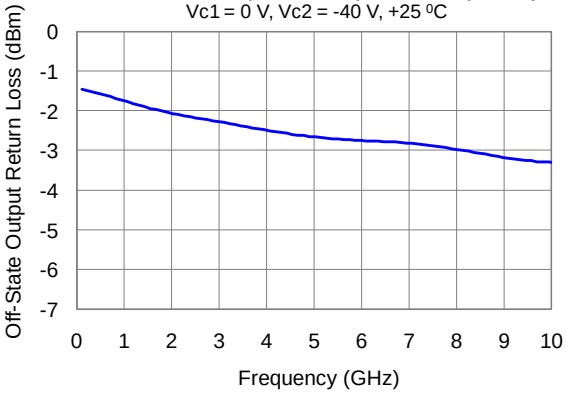
Isolation (Off-State) vs. Frequency
Vc1 = 0 V, Vc2 = -40 V, +25 °C



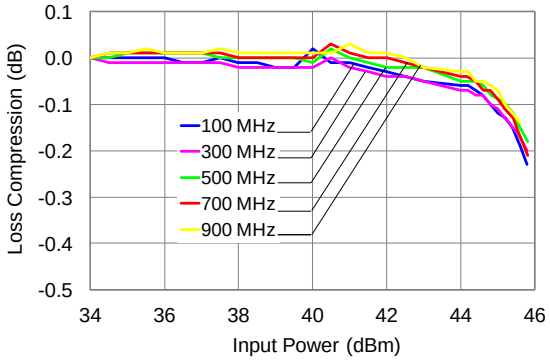
Return Loss (On-State) vs. Frequency
Vc1 = -40 V, Vc2 = 0 V, +25 °C



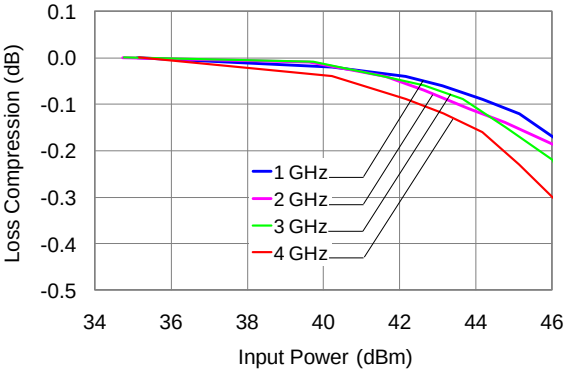
Return Loss (Off-State) vs. Frequency
Vc1 = 0 V, Vc2 = -40 V, +25 °C



Loss Compression vs. Pin vs. Frequency
Vc1 = -40 V, Vc2 = 0 V, +25 °C

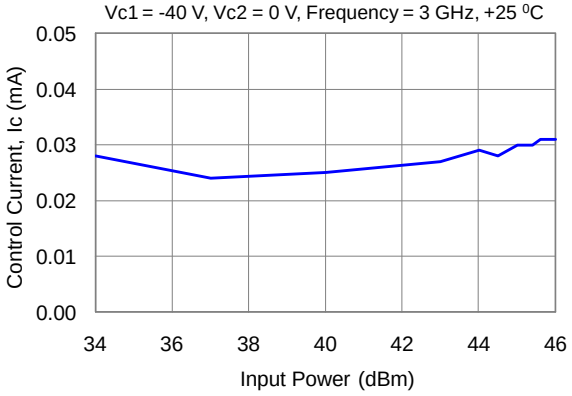


Loss Compression vs. Pin vs. Frequency
Vc1 = -40 V, Vc2 = 0 V, +25 °C

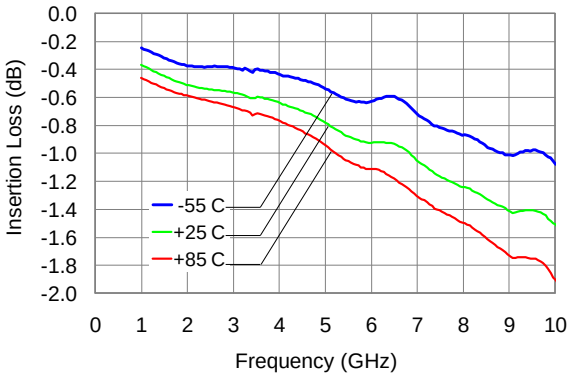


Typical Performance (cont.)

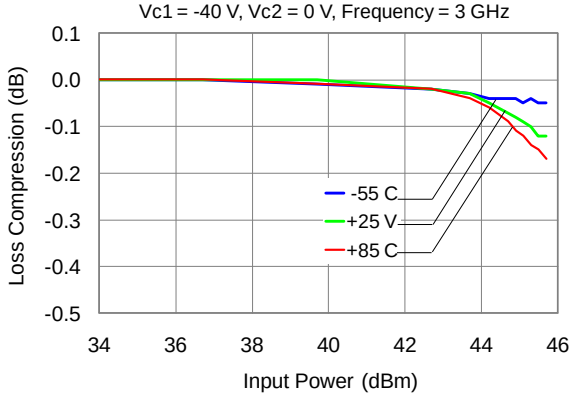
Control Current vs. Pin
Vc1 = -40 V, Vc2 = 0 V, Frequency = 3 GHz, +25 °C



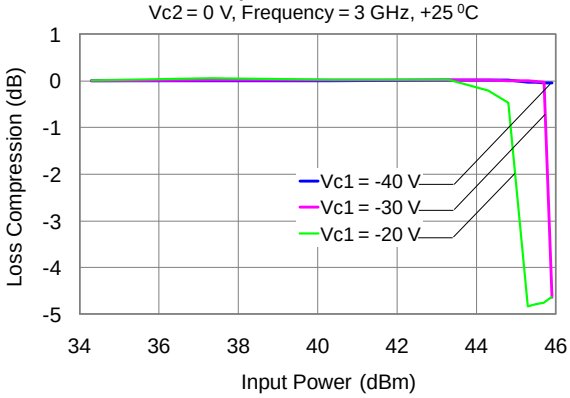
Insertion (On-State) vs. Freq vs. Temp
Vc1 = -40 V, Vc2 = 0 V



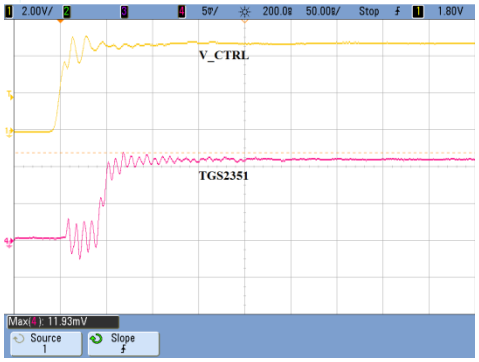
Loss Compression vs. Pin vs. Temp
Vc1 = -40 V, Vc2 = 0 V, Frequency = 3 GHz



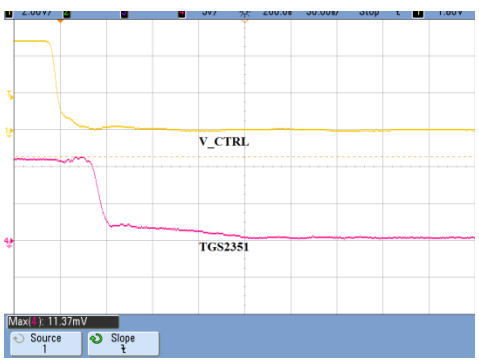
Loss Compression vs. Pin vs. Vc
Vc2 = 0 V, Frequency = 3 GHz, +25 °C



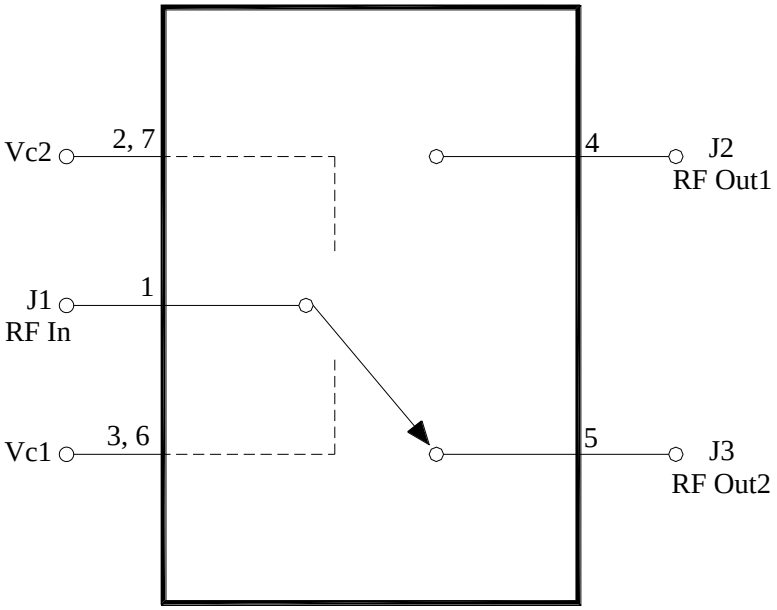
Switching Speed - On < 50 ns
Vc = 0/-40 V, Freq = 3 GHz, Pin = 30 dBm, +25 °C



Switching Speed - Off < 50 ns
Vc = 0/-40 V, Freq = 3 GHz, Pin = 30 dBm, +25 °C



Application Circuit



Vc1 can be biased from either bond pad 3 or 6, and the non-biased bond pad can be left open.
Vc2 can be biased from either bond pad 2 or 7, and the non-biased bond pad can be left open.

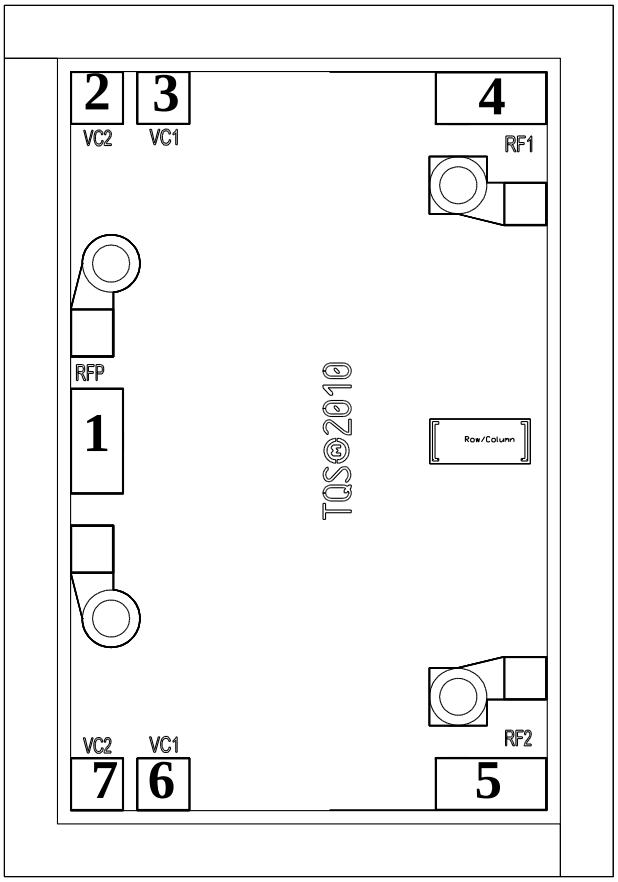
This switch can be configured as a Single Pole, Single Throw (SPST) by terminating one unused RF Out port with a 50 Ohm load.

Bias-up Procedure	Bias-down Procedure
Vc1 or Vc2 set to -40 V (see Function Table below for RF Path)	Turn off RF supply
Vc2 or Vc1 set to 0 V (see Function Table below for RF Path)	Turn Vc1 to 0V
Apply RF signal to RF Input	Turn Vc2 to 0 V

Function Table

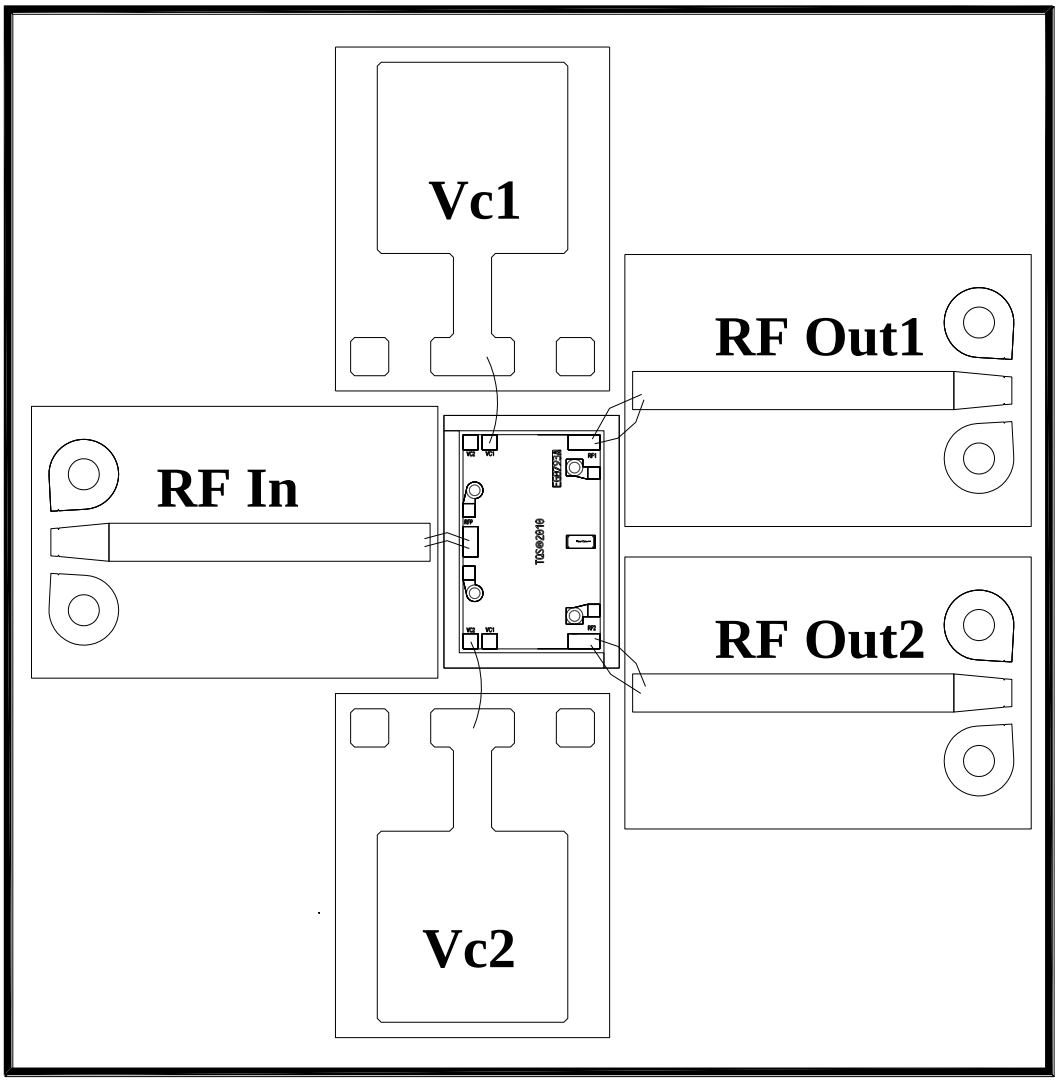
RF Path	State	Vc1	Vc2
RF In to RF Out1 (50 Ohm load to RF Out2)	On-State (Insertion Loss)	0 V	-40 V
	Off-State (Isolation)	-40 V	0 V
RF In to RF Out2 (50 Ohm load to RF Out1)	On-State (Insertion Loss)	-40 V	0 V
	Off-State (Isolation)	0 V	-40 V

Bond Pad Description

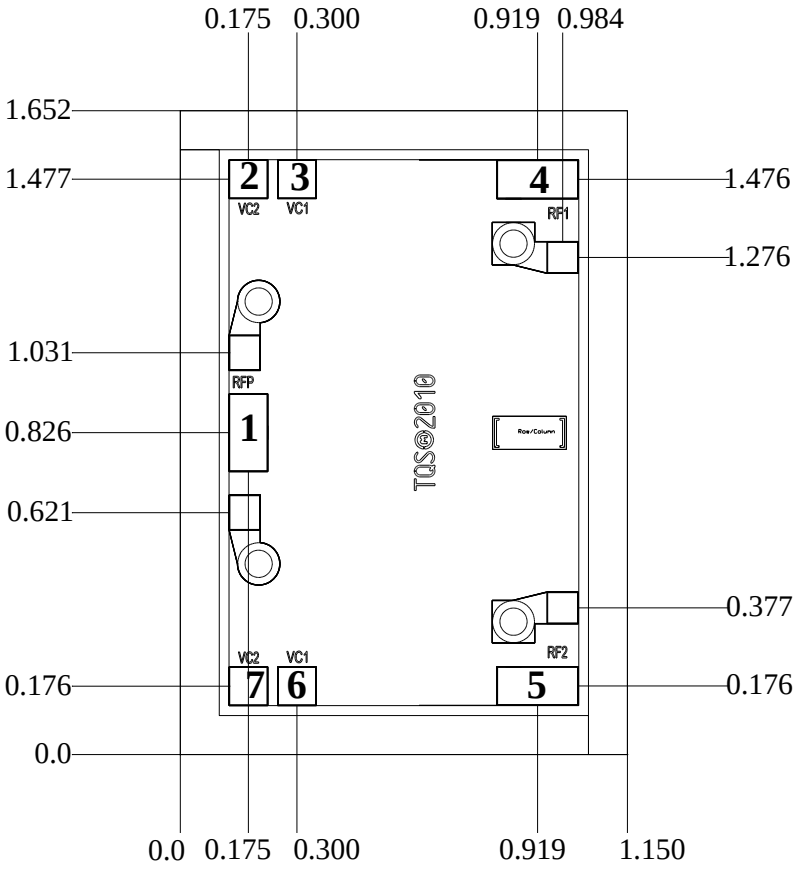


Bond Pad	Symbol	Description
1	RF In	Input, matched to 50 ohms, DC coupled
2, 7	Vc2	Control voltage #2; can be biased from either side (bond pad 2 or bond pad 7), and non-biased bond pad can be left opened; see Application Circuit on page 6 as an example
3, 6	Vc1	Control voltage #1; can be biased from either side (bond pad 3 or bond pad 6), and non-biased bond pad can be left opened; see Application Circuit on page 6 as an example
4	RF Out1	Output #1, matched to 50 ohms, DC coupled
5	RF Out2	Output #2, matched to 50 ohms, DC coupled

Assembly Drawing



Mechanical Information



Unit: millimeters
Thickness: 0.10
Die x, y size tolerance: +/- 0.050
Chip edge to bond pad dimensions are shown to center of pad
Ground is backside of die

Bond Pad	Symbol	Pad Size
1	RF In	0.100 x 0.200
2, 7	Vc2	0.100 x 0.100
3, 6	Vc1	0.100 x 0.100
4	RF Out1	0.200 x 0.100
5	RF Out2	0.200 x 0.100

Product Compliance Information

ESD Information

Caution! ESD-Sensitive Device

ESD Rating:	Class 1B
Value:	Passes ≥ 500 V min.
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22-A114

ECCN

US Department of Commerce EAR99

Solderability

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_40_2$) Free
- PFOS Free
- SVHC Free

Assembly Notes

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment (i.e. epoxy) can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.

Reflow process assembly notes:

- Use AuSn (80/20) solder and limit exposure to temperatures above 300°C to 3-4 minutes, maximum.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- Do not use any kind of flux.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonics are critical parameters.
- Aluminum wire should not be used.
- Devices with small pad sizes should be bonded with 0.0007-inch wire.

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com **Tel:** +1.972.994.8465
Email: info-sales@tqs.com **Fax:** +1.972.994.8504

For technical questions and application information:

Email: info-products@tqs.com

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