μPD100504
65,536 x 4-Bit
100K BiCMOS ECL RAM

PRELIMINARY INFORMATION

Description

The μPD100504 is a very high-speed BiCMOS RAM with full voltage and temperature compensation for a 100K ECL interface. Its unique design uses blended CMOS and bipolar peripheral circuits and N-channel MOS memory cells. The device is organized as 65,536 words by 4 bits and designed with an open-emitter output (noninverted) for low power consumption. A fast access time of 15 ns maximum is available in hermetic, 400-mil, 32-pin cerdip packaging.

Features

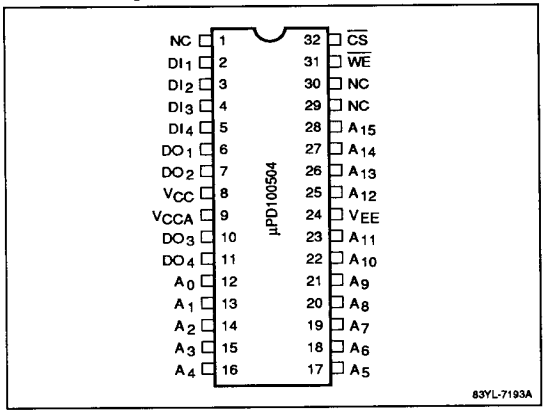
- BiCMOS technology
- 65,536-word x 4-bit organization
- 100K interface ECL with full voltage and temperature compensation
- Noninverted, open-emitter output
- Fast access time of 15 ns maximum
- Low power consumption
- 400-mil, 32-pin cerdip packaging

Ordering Information

Part Number	Access Time (max)	Power Consumption (max)	Package
μPD100504D-15	15 ns	810 mW	32-pin cerdip

Pin Configuration

32-Pin Cerdip



Pin Identification

Symbol	Function
A_0 - A_{15}	Address inputs
DI_1 - DI_4	Data inputs
D_{01} - D_{04}	Data outputs
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
V_{CC}, V_{CCA}	Ground
V_{EE}	−4.5-volt power supply
NC	No connection

8

Absolute Maximum Ratings

Supply voltage, V_{EE}	−7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	−30 to +0.1 mA
Storage temperature, T_{STG}	−65 to +150°C
Storage temperature under bias, T_{STG} (bias)	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Truth Table

$\overline{CS}$	$\overline{WE}$	DI	Output	Mode
H	X	X	L	Not selected
L	L	L	L	Write 0
L	L	H	L	Write 1
L	H	X	D_{OUT}	Read

Notes:

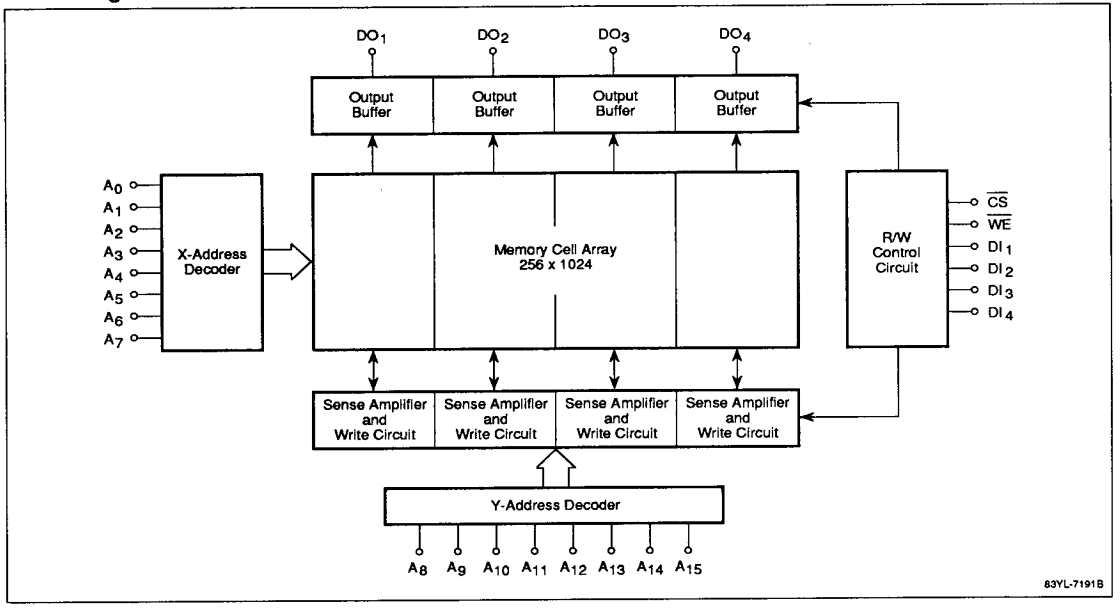
(1) X = don't care.

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		6		pF

Block Diagram



DC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V ±5%; output load = 50 Ω to −2.0 V; V_{CC} = 0 V

Parameter	Symbol	Min	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1025	−880	mV	V_{IN} = V_{IH} max or V_{IL} min
Output voltage, low	V_{OL}	−1810	−1620	mV	V_{IN} = V_{IH} max or V_{IL} min
Output threshold voltage, high	V_{OHC}	−1035		mV	V_{IN} = V_{IH} min or V_{IL} max
Output threshold voltage, low	V_{OLC}		−1610	mV	V_{IN} = V_{IH} min or V_{IL} max
Input voltage, high	V_{IH}	−1165	−880	mV	Guaranteed input voltage high for all inputs
Input voltage, low	V_{IL}	−1810	−1475	mV	Guaranteed input voltage low for all inputs
Input current, high	I_{IH}		220	μA	V_{IN} = V_{IH} max
Input current, low	I_{IL}	0.5	170	μA	For $\overline{CS}$: V_{IN} = V_{IL} min
		−50		μA	For all others: V_{IN} = V_{IL} min
Supply current	I_{EE}	−180		mA	All inputs and outputs open

Notes:

(1) The device under test is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

AC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V ± 5%; V_{CC} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Read Operation						
Address access time	t_{AA}			15	ns	
Chip select access time	t_{ACS}			10	ns	
Chip select recovery time	t_{RCS}			10	ns	
Write Operation						
Write pulse width	t_W	10			ns	
Data setup time	t_{WSD}	2			ns	
Data hold time	t_{WHD}	3			ns	
Address setup time	t_{WSA}	2			ns	
Address hold time	t_{WHA}	3			ns	
Chip select setup time	t_{WSCS}	2			ns	
Chip select hold time	t_{WHCS}	3			ns	
Write disable time	t_{WS}			10	ns	
Write recovery time	t_{WR}			18	ns	
Output Rise and Fall Times						
Rise time	t_R		2		ns	
Fall time	t_F		2		ns	

Notes:

(1) The device under test is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

(2) Input pulse levels = −1.7 to −0.9 V; input rise and fall times (measured between 20% and 80% or 80% and 20%) = 2.0 ns; input and output timing reference levels = 50%.

8

Figure 1. Loading Conditions Test Circuit

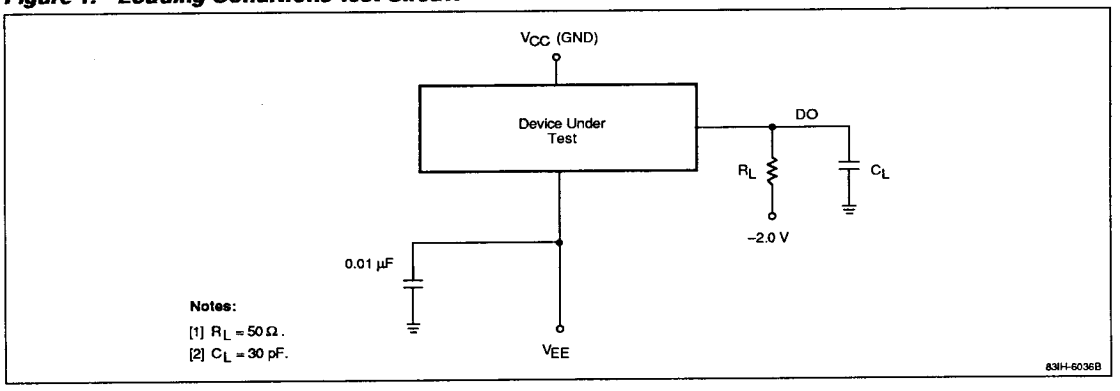
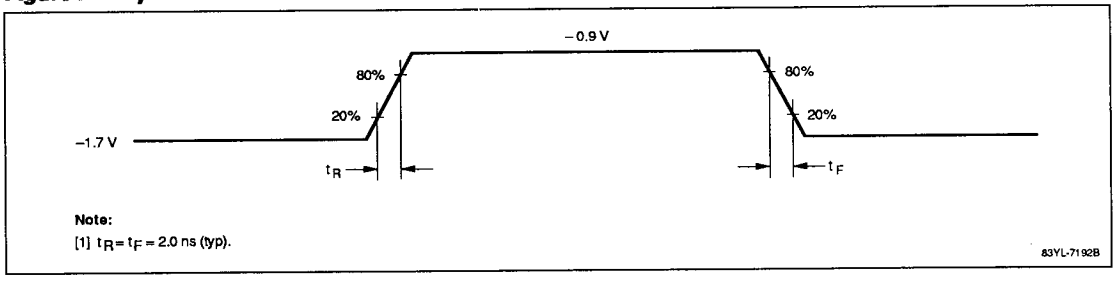
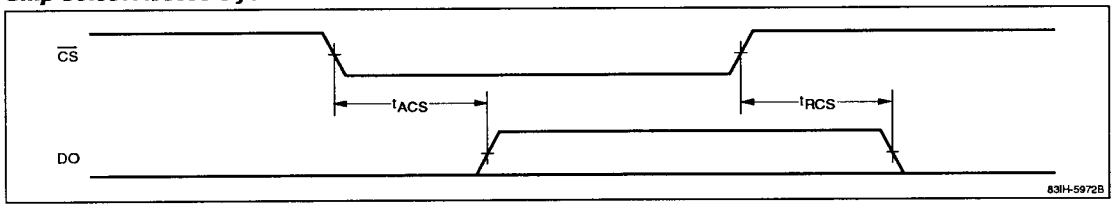


Figure 2. Input Pulse

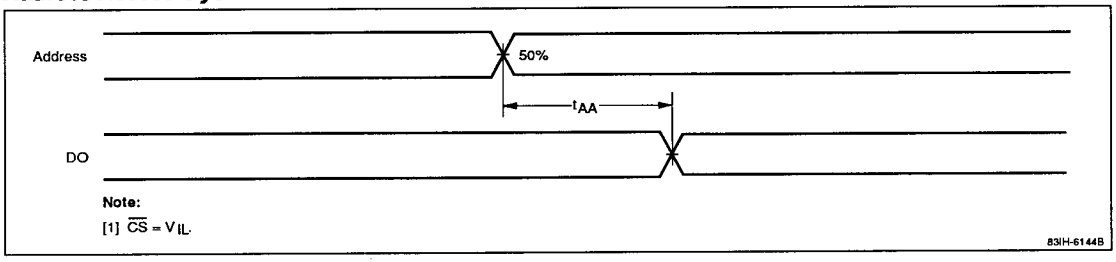


Timing Waveforms

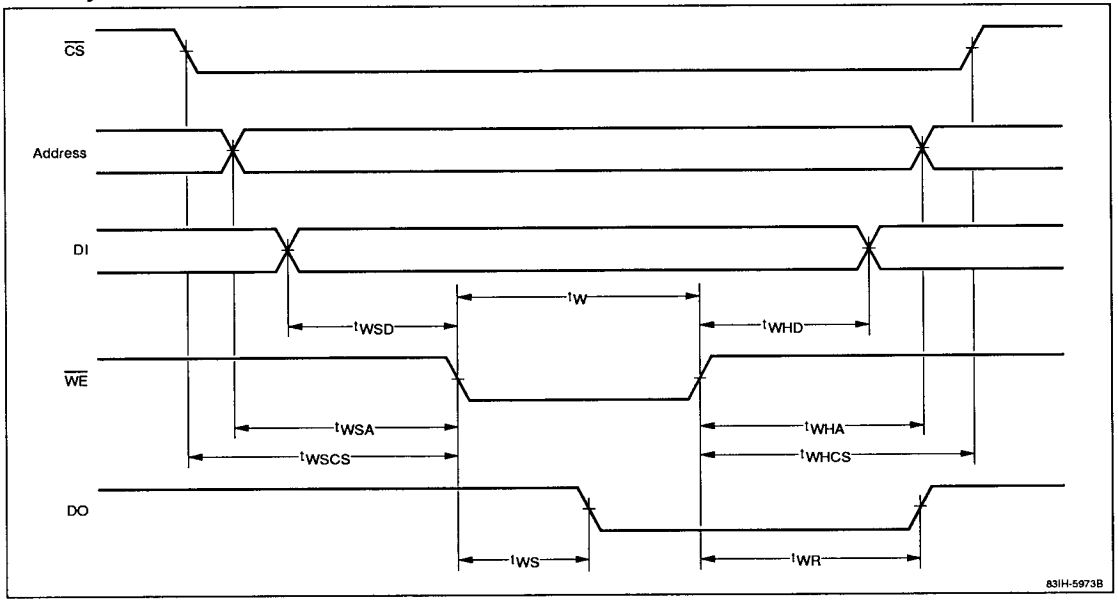
Chip Select Access Cycle



Address Access Cycle



Write Cycle



8