FAIRCHILD SEMICONDUCTOR®

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KA3842AC/KA3842AE
SMPS Controller

Features

- Low start current 0.2mA (Typ.)
- Operating range up to 500kHz
- Cycle by cycle current limiting
- Under Voltage Lock Out (UVLO) with hysteresis
- Short shutdown delay time: Typ.100ns
- High current totem-pole output
- Output swing limiting: 22V

Description

The KA3842AC/KA3842AE are fixed PWM controllers for Off Line and DC to DC converter applications. The internal circuits include UVLO, low start up current, temperature compensated reference, high gain error amplifier, current sensing comparator, and high current totem pole output for driving a POWER MOSFET. Also KA3842AC/KA3842AE provides low start up current below 0.3mA and short shutdown delay time, typically 100ns. The KA3842AC/KA3842AE has a UVLO threshold of 16V(on) and 10V(off). The KA3842AC/KA3842AE can operate within a 100% duty cycle.

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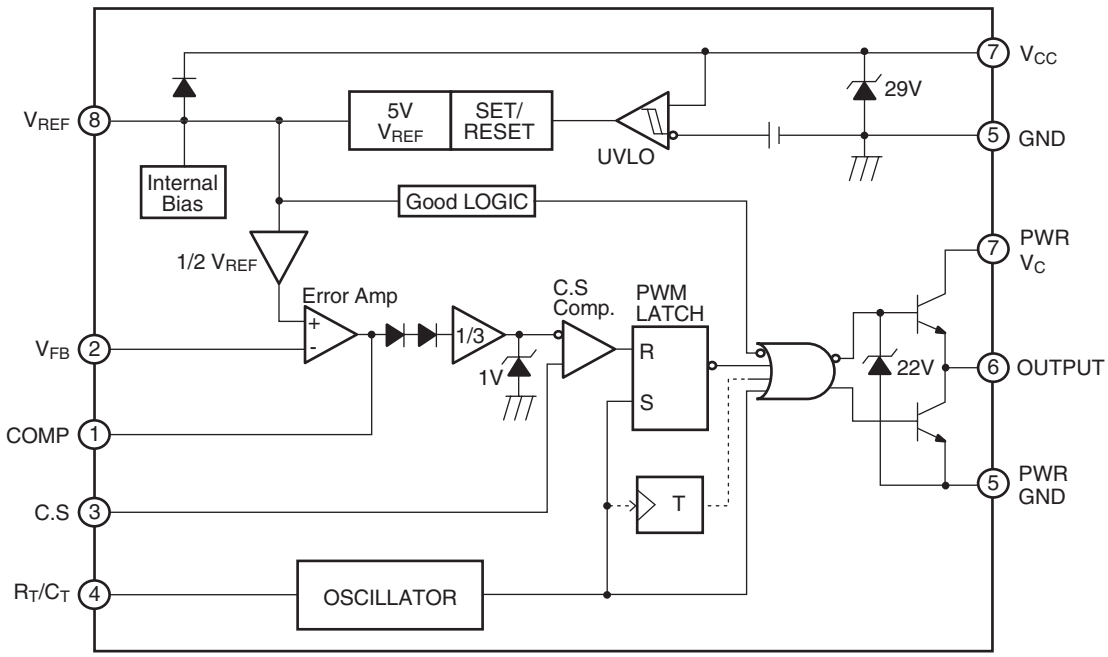
8-DIP

Ordering Information

Part Number	Operating Temp. Range	Pb-Free	Package	Packing Method
KA3842AC	-0 to +70°C	Yes	8-DIP	Tube
KA3842AE				

Internal Block Diagram



Absolute Maximum Ratings

The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	30	V
I_O	Output Current	±1	A
$V_{I(ANA)}$	Analog Inputs (Pins 2, 3)	-0.3 to 6.3	V
$I_{SINK(EA)}$	Error Amp. Output Sink Current	10	mA
P_D	Power Dissipation	1	W
Rθja	Thermal Resistance, Junction-to-Air(4)	95	°C/W

Electrical Characteristics

(V_{CC} = 15V, R_T = 10k¾, C_T = 3.3nF, T_A = 0°C to +70°C, unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
REFERENCE SECTION						
V_{REF}	Output Voltage	T_J = 25°C, I_O = 1mA	4.9	5.0	5.1	V
ΔV_{REF}	Line Regulation	V_{CC} = 12V to 25V	–	6	20	mV
	Load Regulation	I_O = 1mA to 20mA	–	6	25	mV
I_{SC}	Output Short Circuit	T_A = 25°C	–	-100	-180	mA
OSILLATOR SECTION						
F_{OSC}	Initial Accuracy	T_J = 25°C	47	52	57	kHz
ST_V	Voltage Stability	V_{CC} = 12V to 25V	–	0.2	1	%
V_{OSC}	Amplitude	V_{PIN4}, Peak to Peak	–	1.7	–	V
I_{DISCHG}	Discharge Current	T_J = 25°C, Pin 4 = 2V	7.8	8.3	8.8	mA
CURRENT SENSE SECTION						
G_V	Gain(2)(3)		2.85	3	3.15	V/V
$V_{I(MAX)}$	Maximum Input Signal(2)	V_{PIN1} = 5V	0.9	1.0	1.1	V
PSRR	PSRR(1)(2)	V_{CC} = 12V to 25V	–	70	–	dB
I_{BIAS}	Input Bias Current		–	-2	-10	µA
T_D	Delay to Output(1)	V_{PIN3} = 0 V to 2V	–	100	200	ns
ERROR AMPLIFIER SECTION						
V_I	Input Voltage	T_{PIN1} = 2.5V	2.42	2.50	2.58	V
I_{BIAS}	Input Bias Current		–	-0.3	-2	µA
G_{VO}	Open Loop Gain(1)	V_O = 2V to 4V	65	90	–	dB
GBW	Unity Gain Bandwidth(1)	T_J = 25°C	0.7	1	–	MHz
PSRR	PSRR(1)	V_{CC} = 12V to 25V	60	70	–	dB
I_{SINK}	Output Sink Current	V_{PIN2} = 2.7V V_{PIN1} = 1.1V	2	6	–	mA
I_{SOURCE}	Output Source Current	V_{PIN2} = 2.3V V_{PIN1} = 5.0V	-0.5	-0.8	–	mA
V_{OH}	Output High Voltage	V_{PIN2} = 2.3V, R1 = 15k¾ to GND	5	6	–	V
V_{OL}	Output Low Voltage	V_{PIN2} = 2.7V R1 = 15k¾ to Pin 8	–	0.8	1.1	V

Electrical Characteristics (Continued)

(V_{CC} = 15V, R_T = 10k¾, C_T = 3.3nF, T_A = 0°C to +70°C, unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
OUTPUT SECTION						
V_{OL}	Output Low Level	I_{SINK} = 20mA	–	0.1	0.4	V
		I_{SINK} = 200mA	–	1.5	2.2	V
V_{OH}	Output High Level	I_{SOURCE} = 20mA	13	13.5	–	V
		I_{SOURCE} = 200mA	12	13.5	–	V
t_R	Rise Time(1)	T_J = 25°C, C1 = 1nF	–	40	100	ns
t_F	Fall Time(1)	T_J = 25°C, C1 = 1nF	–	40	100	ns
V_{OLIM}	Output Voltage Swing Limit	V_{CC} = 27V, C1 = 1nF	–	22	–	V
UNDER VOLTAGE LOCKOUT SECTION						
V_{TH}	Start Threshold		15	16	17	V
V_{TL}	Min. Operating Voltage (After turn on)		9	10	11	V
PWM SECTION						
D_{MAX}	Maximum Duty Cycle		94	96	100	%
D_{MIN}	Minimum Duty Cycle		–	–	0	%
TOTAL STANDBY CURRENT						
I_{ST}	Start-Up Current		–	0.2	0.4	mA
I_{CC}	Operating Supply Current	V_{PIN2} = V_{PIN3} = 0V	–	11	17	mA
V_Z	V_{CC} Zener Voltage	I_{CC} = 25mA	–	29	–	V

* Adjust V_{CC} above the start threshold before setting at 15V

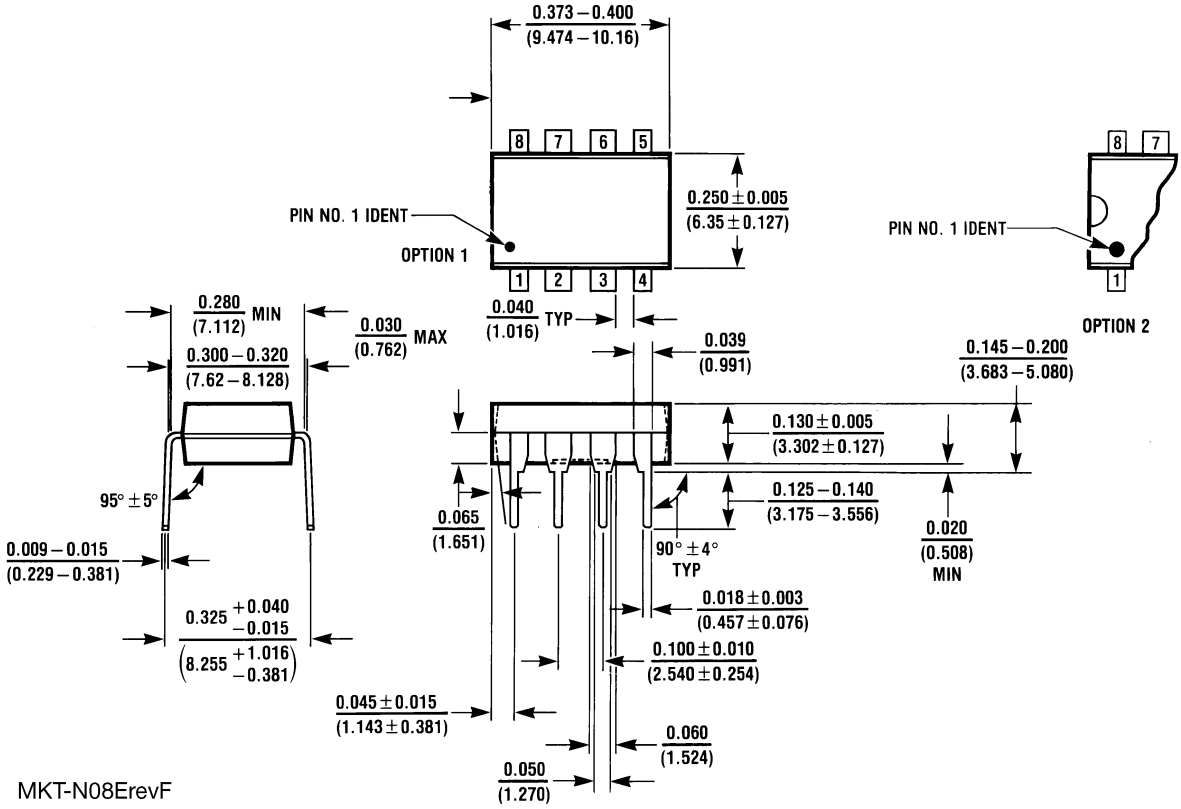
Notes:

1. These parameters, although guaranteed, are not 100% tested in production.
2. Parameter measured at trip point of latch with V2 = 0V.
3. Gain defined as: $G_V = \Delta V_{PIN1} \Delta V_{PIN3} (V_{PIN3}$ = 0 to 0.8V)
4. Junction-to-air thermal resistance test environments
   PCB information:
   Board thickness; 1.6mm, Board dimension: 76.2 X 114.3mm^2, Ref.: EIA/JSED51-3 and EIA/JSED51-7
   Board structure; Using the single layer PCB.

Package Dimensions

8-Pin DIP

Dimensions in millimeters



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