



2-7GHz Bidirectional I²C Bus Controlled Synthesiser

Advance Information

Supersedes July 1996 version, DS3743-4.3

DS3743 - 5.0 June 1998

The SP5655 is a single chip frequency synthesiser designed for TV tuning systems. Control data is entered in the standard I²C BUS format. The device contains 2 addressable current limited outputs and 4 addressable bidirectional open-collector ports, one of which is a 3-bit ADC. The information on these ports can be read via the I²C BUS. the device has one fixed I²C BUS address and 3 programmable addresses, programmed by applying a specific input voltage to one of the current limited outputs. This enables two or more synthesisers to be used in a system.

FEATURES

- Complete 2.7GHz Single Chip System
- High Sensitivity RF Inputs
- Programmable via I²C BUS
- Low Power Consumption (5V, 30mA)
- Low Radiation
- Phase Lock Detector
- Varactor Drive Amp Disable
- 6 Controllable Outputs, 4 Bidirectional
- 5-Level ADC
- Variable I²C BUS Address for Multi-tuner Applications
- ESD Protection: 4kV, Mil-Std-883C, Method 3015 (1)
- Switchable ÷512/1024 Reference Divider
- Pin and Function Compatible with SP5055S (2)
 - (1) Normal ESD handling precautions should be observed.
 - (2) The SP5055S does not have a switchable reference division ratio.

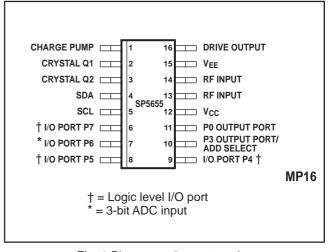


Fig. 1 Pin connections - top view

APPLICATIONS

- Satellite TV
- High IF Cable Tuning Systems

THERMAL DATA

 $\theta_{JC} = 41^{\circ}C/W$ $\theta_{JA} = 111^{\circ}C/W$

ORDERING INFORMATION

SP5655 KG/MPAS (Tubes) SP5655S KG/MPAD (Tape and reel)

SP5655

ELECTRICAL CHARACTERISTICS

 $T_{AMB} = -20^{\circ}\text{C}$ to $+80^{\circ}\text{C}$, $V_{CC} = +4.5\text{V}$ to +5.5V, reference frequency = 4MHz. These Characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Min. Typ. Max.	Characteristic	Din	Value			Hadita	O and distance	
Prescaler input voltage	Characteristic	Pin	Min.	Тур.	Max.	Units	Conditions	
Prescaler input impedance	Supply current	12		30	40			
Prescaler input capacitance 13, 14 2 pF	Prescaler input voltage	13,14	50		300	mVrms	, and the second se	
SDA, SCL Input high voltage 4,5 3 4,5 0 1.5 V Input voltage V _{CC} Input high current 4,5 0 1.5 V Input voltage = V _{CC} Input high current 4,5 1.0 μA Input voltage = 0V When V _{CC} = 0V	Prescaler input impedance			50				
Input high voltage	Prescaler input capacitance	13, 14		2		pF		
Input low voltage	SDA, SCL							
Input high current lnput low current low leakage current low lotage = 0			3		5.5			
Input low current Leakage current	Input low voltage		0		1.5	V		
Leakage current	Input high current				10	μΑ		
SDA Output voltage 4 Usink current = 3mA Charge pump current low 1 ±50 μA Byte 4, bit 2 = 0, pin 1 = 2V Charge pump current high 1 ±170 μA Byte 4, bit 2 = 0, pin 1 = 2V Charge pump current high 1 ±170 μA Byte 4, bit 2 = 0, pin 1 = 2V Charge pump current high 1 ±5 nA Byte 4, bit 2 = 1, pin 1 = 2V Charge pump drive output current 16 500 ±5 nA Byte 4, bit 2 = 0, pin 1 = 2V Charge pump amplifier gain 6400 #A Byte 4, bit 2 = 0, pin 1 = 2V Charge pump output leakage current 16 500 #A Byte 4, bit 2 = 0, pin 1 = 2V Charge pump amplifier gain 6400 #A Byte 4, bit 2 = 0, pin 1 = 2V Charge pump output leakage current 10 #A W pin 16 = 0.7V Charge pump amplifier gain 2 80 MV P-p Recommended crystal series resistance 2 750 1000 Ω External reference input frequency 2 2 8 MHz	Input low current				1	μΑ		
Output voltage 4 0·4 V Sink current = 3mA Charge pump current low 1 ±50 μA Byte 4, bit 2 = 0, pin 1 = 2V Charge pump current high 1 ±170 μA Byte 4, bit 2 = 1, pin 1 = 2V Charge pump output leakage current 1 ±50 μA Byte 4, bit 2 = 1, pin 1 = 2V Charge pump amplifier gain 6400 Exemple of the pin 1 = 2V μA Byte 4, bit 4 = 1, pin 1 = 2V Recommended crystal series resistance 10 200 Ω Parallel resonant crystal (note 2) Crystal oscillator drive level 2 80 mV p-p Q External reference input frequency 2 2 8 MHz AC coupled sinewave External reference input amplitude 2 70 8 MHz AC coupled sinewave P0, P3 sink current 11, 10 0·7 1 1·5 mA Vout = 12V P0, P3 leakage current 11, 10 0·7 1 1·5 mA Vout = 13·2V P4-P7 leakage current 9-6 10	Leakage current	4,5			10	μΑ	When $V_{CC} = 0V$	
Charge pump current low 1	SDA							
Charge pump current high Charge pump current high Charge pump output leakage current 1 1	Output voltage	4			0.4	V	Sink current = 3mA	
Charge pump output leakage current Charge pump drive output current Charge pump amplifier gain Recommended crystal series resistance Crystal oscillator drive level Crystal oscillator negative resistance External reference input frequency External reference input amplitude 2 750 1000 MHz AC coupled sinewave AC coupled sinewave Output Ports P0, P3 sink current P4-P7 sink current P4-P7 leakage current P3 input current high P3 input current low P4, P5, P7 input voltage low P4, P5, P7 input voltage high P6 input current high P7 AB Byte 4, bit 4 = 1, pin 1 = 2V V pin 16 = 0·7V V pin 10 = 2V Crystal oscillator regative resistance B8 MHz B	Charge pump current low	1		±50		μΑ	Byte 4, bit 2 = 0, pin 1 = 2V	
Charge pump drive output current Charge pump amplifier gain Recommended crystal series resistance Crystal oscillator drive level Crystal oscillator negative resistance External reference input frequency External reference input amplitude Cutput Ports P0, P3 sink current P4-P7 sink current P4-P7 leakage current P3 input current high P3 input current low P4, P5, P7 input voltage low P4, P5, P7 input voltage low P6 input voltage low P6 input current high P7 P4-P7 input voltage low P4, P5, P7 input voltage high P6 input current high P6 input current high P7 P4-P7 input voltage low P4, P5, P7 input voltage high P6 input current high P7 P4-P7 input voltage low P4, P5, P7 input voltage high P6 input current high P7 P4-P7 input voltage low P4, P5, P7 input voltage high P6 input current high P7 P5-P0 P5-P1 P6-P7 input voltage low P7-P1 P6-P7 input voltage low P7-P1 P6-P7 input voltage low P7-P7 P6-P7 input voltage low P7-P7 P6-P7 input voltage low P7-P7 P6-P7 P7-P7 P8-P8-P7 P8-P7 P9-P7 P9-P7 P9-P7 P0-P7 P0-P	Charge pump current high	1		±170		μΑ	Byte 4, bit 2 = 1, pin 1 = 2V	
Charge pump amplifier gain Recommended crystal series resistance Crystal oscillator drive level 2 750 1000 Ω mV p-p Crystal oscillator negative resistance 2 750 1000 Ω mV p-p Ω AC coupled sinewave External reference input amplitude 2 70 Ω mV p-p Ω AC coupled sinewave AC point in Ω mV p-p Ω and Ω mV p-p Ω and Ω mV p-p Ω are Ω mV p-p Ω and Ω mV p-p Ω are Ω mV p-p Ω and Ω mV p-p Ω are Ω mV p-p Ω and Ω mV p-p Ω are Ω mV p-p Ω and Ω mV p-p Ω are Ω mV p-p Ω and Ω mV p-p Ω are Ω mV p-p Ω and Ω mV p-p Ω are Ω mV p-p Ω are Ω mV p-p Ω and Ω mV p-p Ω are Ω mV p-p Ω and Ω point current Ω p-6 point current high Ω point current low p-6 point current low p-6 point current high point p	Charge pump output leakage current	1			±5	nA	Byte 4, bit 4 = 1, pin 1 = 2V	
Recommended crystal series resistance 10 80 Ω mV p-p Parallel resonant crystal (note 2) Crystal oscillator negative resistance 2 750 1000 Ω AC coupled sinewave External reference input frequency 2 2 8 MHz AC coupled sinewave External reference input amplitude 2 70 1 1·5 mA AC coupled sinewave Output Ports 11, 10 0·7 1 1·5 mA V _{OUT} = 12V P0, P3 sink current 11, 10 10 μ A V _{OUT} = 13·2V P4-P7 sink current 9-6 10 μ A V _{OUT} = 0·7V P4-P7 leakage current 9-6 10 μ A V _{OUT} = 13·2V Input Ports 10 μ A V pin 10 = V _{CC} P3 input current high 10 μ A V pin 10 = 0V P4, P5, P7 input voltage low 9,8,6 μ A V P4, P5, P7 input voltage high 9,8,6 μ A V P4 input current high 7 μ A V P4 input current high 7 μ A V	Charge pump drive output current	16	500			μΑ	V pin 16 = 0·7V	
Crystal oscillator drive level 2 750 1000 $\frac{1}{\Omega}$ $\frac{1}{\Omega}$ AC coupled sinewave External reference input frequency 2 2 2 $\frac{1}{\Omega}$ $\frac{1}{\Omega}$ AC coupled sinewave External reference input amplitude 2 70 $\frac{1}{\Omega}$ $\frac{1}{\Omega}$ AC coupled sinewave AC	Charge pump amplifier gain			6400				
Crystal oscillator negative resistance $2 \ 750 \ 1000$ Ω Ω External reference input frequency $2 \ 2 \ 70$ $0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 $	Recommended crystal series resistance		10		200	Ω	Parallel resonant crystal (note 2)	
External reference input frequency $2 2 70$ 200 mVrms AC coupled sinewave 200 mVrms AC co	Crystal oscillator drive level	2		80		mV p-p		
External reference input amplitude 2 70 200 mVrms AC coupled sinewave Output Ports P0, P3 sink current 11, 10 0·7 1 1·5 mA $V_{OUT} = 12V$ P0, P3 leakage current 11, 10 10 μ A $V_{OUT} = 13\cdot2V$ P4-P7 sink current 9-6 10 μ A $V_{OUT} = 0\cdot7V$ P4-P7 leakage current 9-6 10 μ A $V_{OUT} = 13\cdot2V$ Input Ports P3 input current high 10 μ A $V_{OUT} = 13\cdot2V$ P4, P5, P7 input voltage low P4, P5, P7 input voltage high P6 input current high 9,8,6 2·7 $V_{OUT} = 0.7V$ P6 input current high P3 $V_{OUT} = 0.7V$ P7 $V_{OUT} = 0.7V$ P8 $V_{OUT} = 0.7V$ P9 $V_{OUT} = 0.7V$ P10 $V_{$	Crystal oscillator negative resistance	2	750	1000		Ω		
Output Ports 11, 10 0·7 1 1·5 mA $V_{OUT} = 12V$ P0, P3 sink current 11, 10 10 μA $V_{OUT} = 13 \cdot 2V$ P4-P7 sink current 9-6 10 mA $V_{OUT} = 0 \cdot 7V$ P4-P7 leakage current 9-6 10 μA $V_{OUT} = 13 \cdot 2V$ Input Ports 10 μA $V_{OUT} = 13 \cdot 2V$ P3 input current high 10 +10 μA $V_{OUT} = 13 \cdot 2V$ P3 input current low 10 -10 μA $V_{OUT} = 13 \cdot 2V$ P4, P5, P7 input voltage low 10 -10 μA $V_{OUT} = 13 \cdot 2V$ P4, P5, P7 input voltage low 10 -10 μA $V_{OUT} = 13 \cdot 2V$ P4, P5, P7 input voltage high 9,8,6 $V_{OUT} = 13 \cdot 2V$ $V_{OUT} = 13 \cdot 2V$ P4, P5, P7 input voltage high 9,8,6 $V_{OUT} = 13 \cdot 2V$ $V_{OUT} = 13 \cdot 2V$ P6 input current high 7 $V_{OUT} = 13 \cdot 2V$ $V_{OUT} = 13 \cdot 2V$	External reference input frequency	2	2		8	MHz	AC coupled sinewave	
PO, P3 sink current 11, 10 0.7 1 1.5 mA $V_{OUT} = 12V$ P0, P3 leakage current 11, 10 10 μ A $V_{OUT} = 13.2V$ P4-P7 sink current 9-6 10 μ A $V_{OUT} = 0.7V$ P4-P7 leakage current 9-6 10 μ A $V_{OUT} = 13.2V$ Input Ports 10 μ A $V_{OUT} = 13.2V$ P3 input current high 10 μ A $V_{OUT} = 13.2V$ P3 input current low 10 μ A $V_{OUT} = 13.2V$ P4, P5, P7 input voltage low 10 μ A $V_{OUT} = 13.2V$ P4, P5, P7 input voltage low 10 μ A $V_{OUT} = 13.2V$ P4, P5, P7 input voltage high 9,8,6 $V_{OUT} = 13.2V$ P4, P5, P7 input voltage high 9,8,6 $V_{OUT} = 13.2V$ P4, P5, P7 input voltage high 9,8,6 $V_{OUT} = 13.2V$ P4, P5, P7 input voltage high 9,8,6 $V_{OUT} = 13.2V$ P4, P5, P7 input voltage high $V_{OUT} = 13.2V$ P5 input voltage high $V_{OUT} = 13.2V$ P5 input voltage high $V_{OUT} = 13.2V$ P6 inp	External reference input amplitude	2	70		200	mVrms	AC coupled sinewave	
P0, P3 leakage current	Output Ports							
P4-P7 sink current 9-6 10 μ A $V_{OUT} = 0.7V$ $V_{OUT} = 13.2V$ Input Ports P3 input current high 10 μ A $V_{OUT} = 13.2V$ P3 input current low 10 μ A $V_{OUT} = 13.2V$ P4, P5, P7 input voltage low 9,8,6 P4, P5, P7 input voltage high 9,8,6 P6 input current high 7 ν 4 See Table 3 for ADC levels	P0, P3 sink current	11, 10	0.7	1	1.5	mA	$V_{OUT} = 12V$	
P4-P7 leakage current9-610μA $V_{OUT} = 13 \cdot 2V$ Input PortsP3 input current high P3 input current low P4, P5, P7 input voltage low P4, P5, P7 input voltage high P6 input current high10+10μA $V_{DID} = 10 \cdot 2V_{CC}$ P4, P5, P7 input voltage high P6 input current high9,8,6 9,8,6 9,8,62-7 4-10 $V_{DID} = 10 \cdot 2V_{CC}$ 4-10 $V_{DID} = 10 \cdot 2V_{CC}$ 4-10	P0, P3 leakage current	11, 10			10	μΑ		
Input Ports 10 $+10$ μ A V pin 10 = V_{CC} P3 input current low 10 -10 μ A V pin 10 = V_{CC} P4, P5, P7 input voltage low 9,8,6 V V P4, P5, P7 input voltage high 9,8,6 V P6 input current high 7 V P6 input current high 7 P 3 input current high P 3 input voltage low P 4, P5, P7 input voltage high P 5 input current high P 6 input current high P 7 input voltage high P 7 input voltage high P 8 input current high P 8 input current high P 9 in	P4-P7 sink current	9-6	10			mA	$V_{OUT} = 0.7V$	
P3 input current high P3 input current low P4, P5, P7 input voltage low P4, P5, P7 input voltage high P6 input current high P6 input current high P3 input current high P3 input current high P4 P5, P7 input voltage high P6 input current high P5 P7	P4-P7 leakage current	9-6			10	μΑ	$V_{OUT} = 13.2V$	
P3 input current high P3 input current low P4, P5, P7 input voltage low P4, P5, P7 input voltage high P6 input current high P6 input current high P3 input current high P3 input current high P4 P5, P7 input voltage high P6 input current high P5 P7	Input Ports							
P3 input current low	•	10			+10	μΑ	V pin 10 = V _{CC}	
P4, P5, P7 input voltage low P4, P5, P7 input voltage high P6 input current high P9,8,6 P1, P5, P7 input voltage high P6 input current high P8,8,6 P9,8,6 P1, P5, P7 input voltage low P9,8,6 P1, P5, P7 input voltage low P9,8,6 P1, P5, P7 input voltage low P1, P5, P7 input voltage low P1, P5, P7 input voltage low P2, P5, P7 input voltage low P3,8,6 P4, P5, P7 input voltage low P4, P5, P7 input voltage high P5, P7 input voltage high P6 input current high P7, P5, P7 input voltage high P7, P5, P7 input voltage high P8,8,6 P9,8,6 P1, P5, P7 input voltage high P8,8,6 P9,8,6 P1, P5, P7 input voltage high P9,8,6 P1, P5, P7 input voltage high P9,8,6 P1, P5, P7 input voltage high P6 input current high		10			-10	1 '		
P4, P5, P7 input voltage high P6 input current high 9,8,6 2·7 +10 μ See Table 3 for ADC levels	·	9,8,6			0.8	V	-	
P6 input current high 7 +10 μA See Table 3 for ADC levels			2.7			V		
' ' '					+10	μΑ	See Table 3 for ADC levels	
P6 input current iow / -10 μA	P6 input current low	7			-10	μ A		

NOTES

^{1.} Maximum power consumption is 220mW with $V_{CC} = 5.5V$ and all ports off. 2. Resistance specified is maximum under all conditions.

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE} and pin 3 at 0V

Parameter	Pin	Va	lue	Units	Conditions
T drameter		Min.	Max.	Omto	Conditions
Supply voltage	12	-0.3	7	V	
RF input voltage	13,14		2.5	V p-p	
Port voltage	6-11	-0.3	14	V	Port in off state
	6-9	-0.3	6	V	Port in on state
	10, 11	-0.3	14	V	Port in on state
Total port output current	6-9		50	mA	
Address select voltage	10	-0.3	V _{CC} +0·3	V	
RF input DC offset	13-14	-0.3	V _{CC} +0·3	V	
Charge pump DC offset	1	-0.3	V _{CC} +0⋅3	V	
Drive output DC offset	16	-0.3	V _{CC} +0·3	V	
Crystal oscillator DC offset	2	-0.3	V _{CC} +0·3	V	
SDA, SCL input voltage	4,5	-0.3	6	V	
Storage temperature		-55	+150	°C	
Junction temperature			+150	°C	

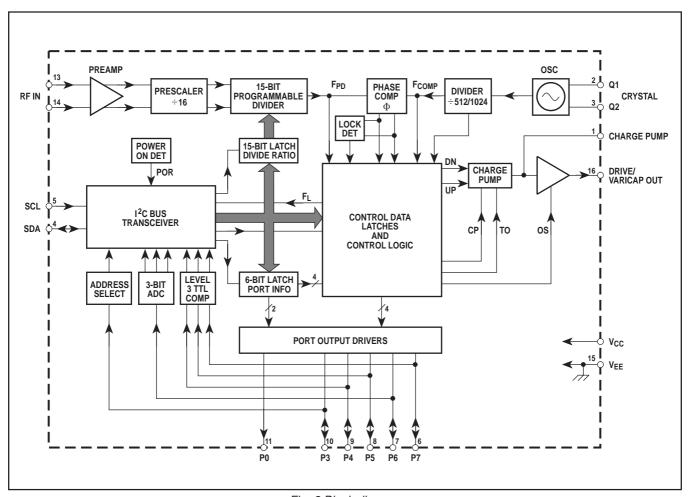


Fig. 2 Block diagram

FUNCTIONAL DESCRIPTION

The SP5655 is programmed from an I²C Bus. Data and Clock are fed in on the SDA and SCL lines respectively, as defined by the I²C Bus format. The synthesiser can either accept new data (write mode) or send data (read mode). The LSB of the address byte (R/W) sets the device into write mode if it is low and read mode if it is high. The Tables in Fig. 3 illustrate the format of the data. The device can be programmed to respond to several addresses, which enables the use of more than one synthesiser in an I²C Bus system. Table 4 shows how the address is selected by applying a voltage to P3.

When the device receives a correct address byte, it pulls the SDA line low during the acknowledge period, and during following acknowledge periods after further data bytes are programmed. When the device is programmed into the read mode, the controller accepting the data must pull the SDA line low during all status byte acknowledge periods to read another status byte. If the controller fails to pull the SDA line low during this period, the device generates an internal STOP condition, which inhibits further reading.

WRITE Mode (Frequency Synthesis)

When the device is in write mode bytes 2 and 3 select the synthesised frequency, while bytes 4 and 5 control the output port states, charge pump, reference divider ratio and various test modes.

Once the correct address is received and acknowledged, the first bit of the next byte determines whether that byte is interpreted as byte 2 or 4; a logic 0 for frequency information and a logic 1 for control and output port information. When byte 2 is received the device always expects byte 3 next. Similarly, when byte 4 is received the device expects byte 5 next. Additional data bytes can be entered without the need to readdress the device until an I²C stop condition is recognised. This allows a smooth frequency sweep for fine tuning or AFC purposes.

If the transmission of data is stopped mid-byte (for example, by another device on the bus) then the previously programmed byte is maintained.

Frequency data from bytes 2 and 3 are stored in a 15-bit register and used to control the division ratio of the 15-bit programmable divider. This is preceded by a divide-by-16 prescaler and amplifier to give excellent sensitivity at the local oscillator input, see Fig. 5. The input impedance is shown in Fig. 7.

The programmed frequency can be calculated by multiplying the programmed division ratio by 16 times the comparison frequency F_{COMP}. When frequency data is entered, the phase comparator, via a charge pump and varicap drive amplifier, adjusts the local oscillator control voltage until the output of the programmable divider is frequency and phased locked to the comparison frequency.

The reference frequency may be generated by an external source capacitively coupled into pin 2, or provided by an onchip crystal controlled oscillator. The comparison frequency F_{COMP} is derived from the reference frequency via the reference divider. The reference divider division ratio is switchable

from 512 to 1024, and is controlled by bit 7 of byte 4 (TS0); a logic 1 to 512, a logic 0 for 1024. The SP5655 differs from the SP5055 in this respect, only 512 being available on the SP5055. Note that the comparison frequency is 7.8125 kHz when a 4MHz reference is used, and divide by 512 is selected.

Bit 2 of byte 4 of the programming data (CP) controls the current in the charge pump circuit, a logic 1 for $\pm 170\mu A$ and a logic 0 for $\pm 50\mu A$, allowing compensation for the variable tuning slope of the tuner and also to enable fast channel changes over the full band. When the device is frequency locked, the charge pump current is internally set to $\pm 50\mu A$ regardless of CP.

Bit 4 of byte 4 (T0) disables the charge pump when it is set to a logic 1.

Bit 8 of byte 4 (OS) switches the charge pump drive amplifier's output off when it is set to a logic 1.

Bit 3 of byte 4 (T1) enables various test modes when set high. These modes are selected by bits 5, 6 and 7 of byte 4 (TS2, and TS1, TS0) as detailed in Table 5. When T1 is set low, TS2 and TS1 are assigned a 'don't care' condition, and TS0 selects the reference divider ratio as previously described.

Byte 5 programs the output ports P0 and P3 to P7; a logic 0 for a high impedance output and a logic 1 for low impedance (on).

READ Mode

When the device is in read mode the status byte read from the device on the SDA line takes the form shown in Table 2.

Bit 1 (POR) is the power-on reset indicator and is set to a logic 1 if the $V_{\rm CC}$ supply to the device has dropped below 3V (at $25\,^{\circ}{\rm C}$), for example, when the device is initially turned on. The POR is reset to 0 when the read sequence is terminated by a stop command. When POR is set high (at low $V_{\rm CC}$), the programmed information is lost and the output ports are all set to high impedance.

Bit 2 (FL) indicates whether the device is phase locked, a logic 1 is present if the device is locked, and a logic 0 if the device is unlocked.

Bits 3, 4 and 5 (I2, I1, I0) show the status of the I/O Ports P7, P5 and P4 respectively. A logic 0 indicates a low level and a logic 1 a high level. If the ports are to be used as inputs they should be programmed to a high impedance state (logic 1). These inputs will then respond to data complying with TTL type voltage levels.

Bits 6, 7 and 8 (A2, A1, A0) combine to give the output of the 5-level ADC. The ADC can be used to feed AFC information to the microprocessor from the IF section of the receiver, as illustrated in the typical application circuit.

APPLICATION

A typical application is shown in Fig. 4. All input/output interface circuits are shown in Fig. 6. The SP5655 is function and pin equivalent to the SP5055 device apart from the switchable reference divider, and has much lower power dissipation, improved RF sensitivity and better ESD performance.

N	ISB	LSB

Address	1	1	0	0	0	MA1	MA0	0	Α	Byte 1
Programmable divider	0	214	2 ¹³	2 ¹²	211	2 ¹⁰	2 ⁹	2 ⁸	Α	Byte 2
Programmable divider	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰	Α	Byte 3
Charge pump and test bits	1	СР	T1	T0	TS2	TS1	TS0	os	Α	Byte 4
I/O port control bits	P7	P6	P5	P4	P3	Х	Х	P0	Α	Byte 5

Table 1 Write data format (MSB transmitted first)

Address	1	1	0	0	0	MA1	MA0	1	Α	Byte 1
Status byte	POR	FL	12	l1	10	A2	A1	A0	Α	Byte 2

Table 2 Read data format

A2	A 1	Α0	Voltage input to P6
1	0	0	0.6V _{CC} to 13.2V
0	1	1	0·45V _{CC} to 0·6V _{CC}
0	1	0	0.3V _{CC} to 0.45V _{CC}
0	0	1	0·15V _{CC} to 0·3V _{CC}
0	0	0	0V to 0·15V _{CC}

MA1	MA0	Address select input voltage
0	0	0V to 0·2V _{CC}
0	1	Always valid
1	0	0.3V _{CC} to 0.7V _{CC}
1	1	0.8V _{CC} to 13.2V

Table 3 ADC levels

Table 4 Address selection

T1	TS2	TS1	TS0	Operation mode description
0	Х	Х	0	Normal operation, test modes disabled, reference divider ratio = 1024
0	Х	Х	1	Normal operation, test modes disabled, reference divider ratio = 512
1	0	0	Х	Charge pump source (down). Status bit FL set to 0
1	0	1	Х	Charge pump sink (up). Status bit FL set to 1
1	1	0	0	Ports P4, P5, P6, P7set to state X
1	1	0	1	Port P7 = F _{PD} /2; P4, P5, P6 set to state X
1	1	1	Х	Port P7 = F_{PD} ; P6 = F_{COMP} ; P4, P5 set to state X

Table 5 Operation modes

NOTES

X = don't care

For further details of test modes, see Table 6

A : Acknowledge bit

MA1, MA0 : Variable address bits (see Table 4)
CP : Charge Pump current select

T1 : Test mode selection
T0 : Charge pump disable

TS2, TS1, TS0 : Operation mode control bits (see Table 5)
OS : Varactor drive Output disable Switch

P7, P6, P5, P4, P3, P0 : Control output port states
POR : Power On Reset indicator
FL : Phase lock detect flag

I2, I1, I0 : Digital information from ports P7, P5 and P4 respectively

A2, A1, A0 : 5-level ADC data from P6 (see Table 3)

X : Don't care

Fig. 3 Data formats

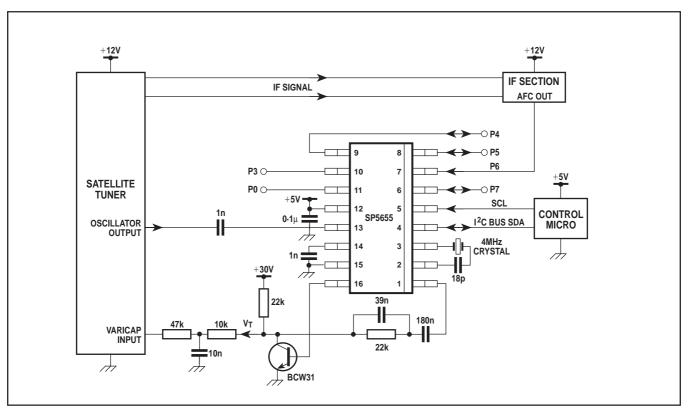


Fig. 4 Typical application

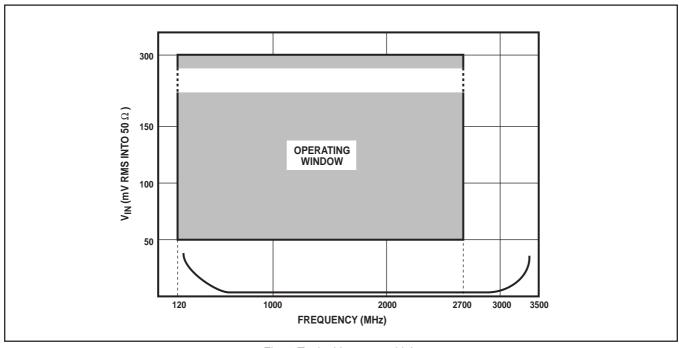


Fig. 5 Typical input sensitivity

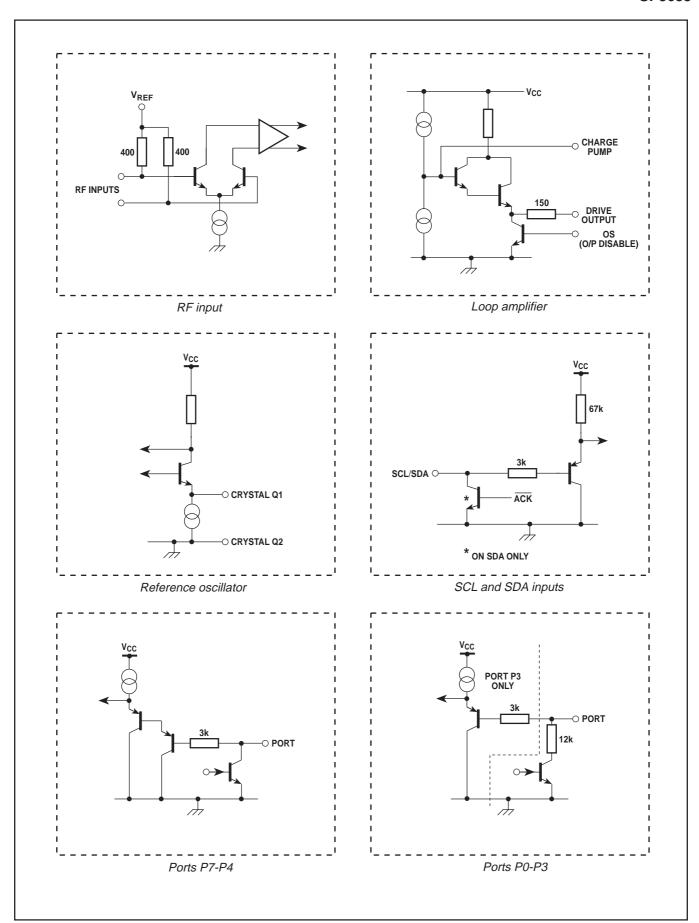


Fig. 6 SP5655 input/output interface circuits

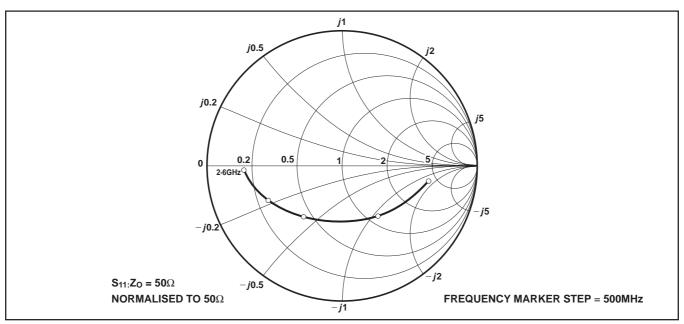


Fig. 7 Typical input impedance,

APPLICATION NOTES

An application note, AN168, is available for designing with synthesisers such as the SP5655. It covers aspects such as loop filter design, decoupling and I²C bus radiation problems.

The application note is published in the Mitel Semiconductor Media IC Handbook. A generic test/demonstration board has been produced, which can be used for the SP5655. A circuit diagram and layout for the board are shown in Figs. 8 and 9.

The board can be used for the following purposes:

- (A) Measuring RF sensitivity perforance
- (B) Indicating port function
- (C) Synthesising a voltage controlled oscillator
- (D)Testing external reference sources

The programming codes relevant to these tests are given in Table 6.

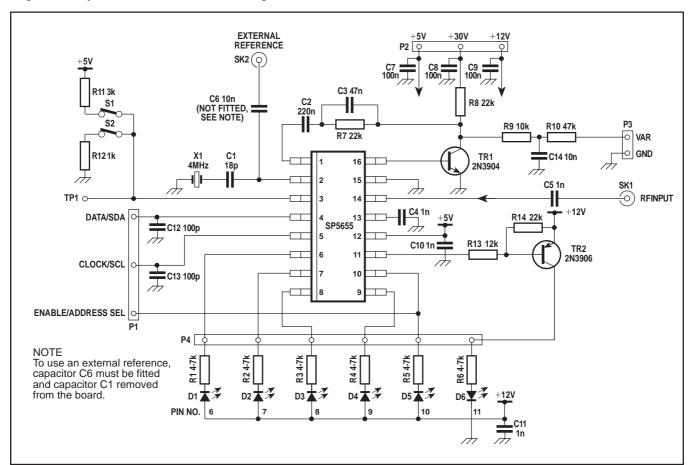
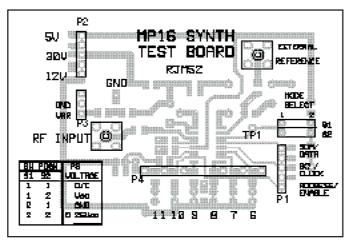
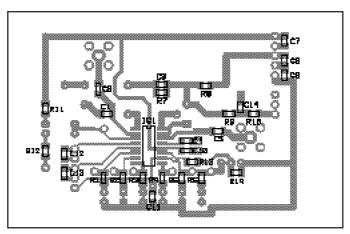


Fig. 8 Test board circuit



TP1 = PIN 3 DC BIAS

Top view (ground plane)



Underside (surface mounted components side)

NOTES

- 1. CIRCUIT SCHEMATIC IS SHOWN IN FIG. 8
- 2. ALL SUFACE MOUNT COMPONENTS ARE MOUNTED ON UNDERSIDE OF BOARD

Fig. 9 Test board layout

SP5655

TEST MODES

As explained in the functional description, The SP5655 can be programmed into a number of test modes. These are invoked by programming Hex codes into byte 4, those most commonly used being shown in Table 6.

Other codes will also apply due to don't care conditions, which are assumed to be 1 in the Table.

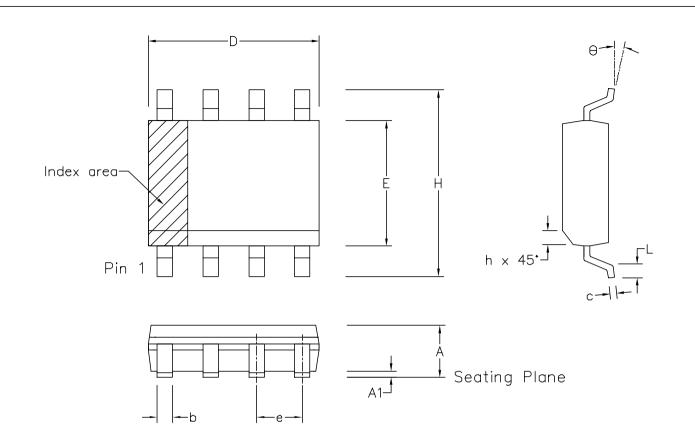
NOTE:

When looking at F_{PD} or F_{COMP} signals from ports P7 and P6. byte should be sent twice, first to set the desired reference division ratio then to switch on the chosen test mode.

The pulses can then be measured by simply connecting an oscilloscope or counter to the relevant output pin on the test board.

On anation woods described	Hex code (byte 4)				
Operation mode description	CP high mode	CP low mode			
Normal operation, reference divider ratio = 1024	CC	8C			
Normal operation, reference divider ratio = 512	CE	8E			
Charge pump source (down), FL set to 0	E2	A2			
Charge pump sink (up), FL set to 1	E6	A6			
Port P7 = F _{PD} /2	EA	AA			
Port P7 = F_{PD} , P6 = F_{COMP}	EE	AE			
Charge pump disable, reference divider ratio = 512	DE	9E			
Varactor line disable, reference divider ratio = 512	CF	8F			
Charge pump and varactor line disable, reference divider ratio = 512	DF	9F			

Table 5 Operation modes



	Min	Max	Min	Max	
	mm	mm	inch	inch	
Α	1.35	1.75	0.053	0.069	
A1	0.10	0.25	0.004	0.010	
D	9.80	10.00	0.386	0.394	
Н	5.80	6.20	0.228	0.244	
Е	3.80	4.00	0.150	0.157	
L	0.40	1.27	0.016	0.050	
е	1.27	BSC	0.050 BSC		
b	0.33	0.51	0.013	0.020	
U	0.00				
С	0.19	0.25	0.008	0.010	
				0.010 8°	
С	0.19	0.25	0.008	i	
С	0.19 0°	0.25 8° 0.50	0.008 0°	8°	
С	0.19 0° 0.25	0.25 8° 0.50	0.008 0° 0.010 eatures	8°	

Notes:

- 1. The chamfer on the body is optional. If it not present, a visual index feature, e.g. a dot, must be located within the cross—hatched area.
- 2. Controlling dimension are in inches.

- 3. Dimension D do not include mould flash, protusion or gate burrs. These shall not exceed 0.006" per side.
 4. Dimension E1 do not include inter—lead flash or protusion. These shall not exceed 0.010" per side.
 5. Dimension b does not include dambar protusion/intrusion. Allowable dambar protusion shall be 0.004" total in excess of b dimension.

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ISSUE	1	2	3	4			Title: Package Outline Drawing for 16 Ids SOIC(N)-0.150" Body Width (MP)
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