Data Sheet **February 15, 2007** **FN3159.2**

8-Digit LED Microprocessor-Compatible Multiplexed Display Decoder Driver

The ICM7218 series of universal LED driver systems provide, in a single package, all the circuitry necessary to interface most common microprocessors or digital systems to an LED display. Included on chip are an 8-byte static display memory, two types of 7-segment decoders, multiplex scan circuitry, and high current digit and segment drivers for either common-cathode or common-anode displays.

The ICM7218A and 1CM7218B feature two control lines (WRITE and MODE) which write either 4 bits of control information (DATA COMING, SHUTDOWN, DECODE, and HEXA/CODE B) or 8 bits of display input data. Display data is automatically sequenced into the 8-byte internal memory on successive positive going WRITE pulses. Data may be displayed either directly or decoded in Hexadecimal or Code B formats.

The ICM7218C and ICM7218D feature two control lines (WRITE and HEXA/CODE B/SHUTDOWN), 4 separate display data input lines, and 3 digit address lines. Display data is written into the internal memory by setting up a digit address and strobing the WRITE line low. Only Hexadecimal and Code B formats are available for display outputs.

Features

- Microprocessor Compatible

- Total Circuit Integration On Chip Includes:
  - Digit and Segment Drivers
  - All Multiplex Scan Circuitry
  - 8-Byte Static Display Memory
  - 7-Segment Hexadecimal and Code B Decoders

- Output Drive Suitable for LED Displays Directly

- Common Anode and Common Cathode Versions

- Single 5V Supply Required

- Data Retention to 2V Supply

- Shutdown Feature - Turns Off Display and Puts Chip Into Low Power Dissipation Mode

- Sequential and Random Access Versions

- Decimal Point Drive On Each Digit

Related Literature

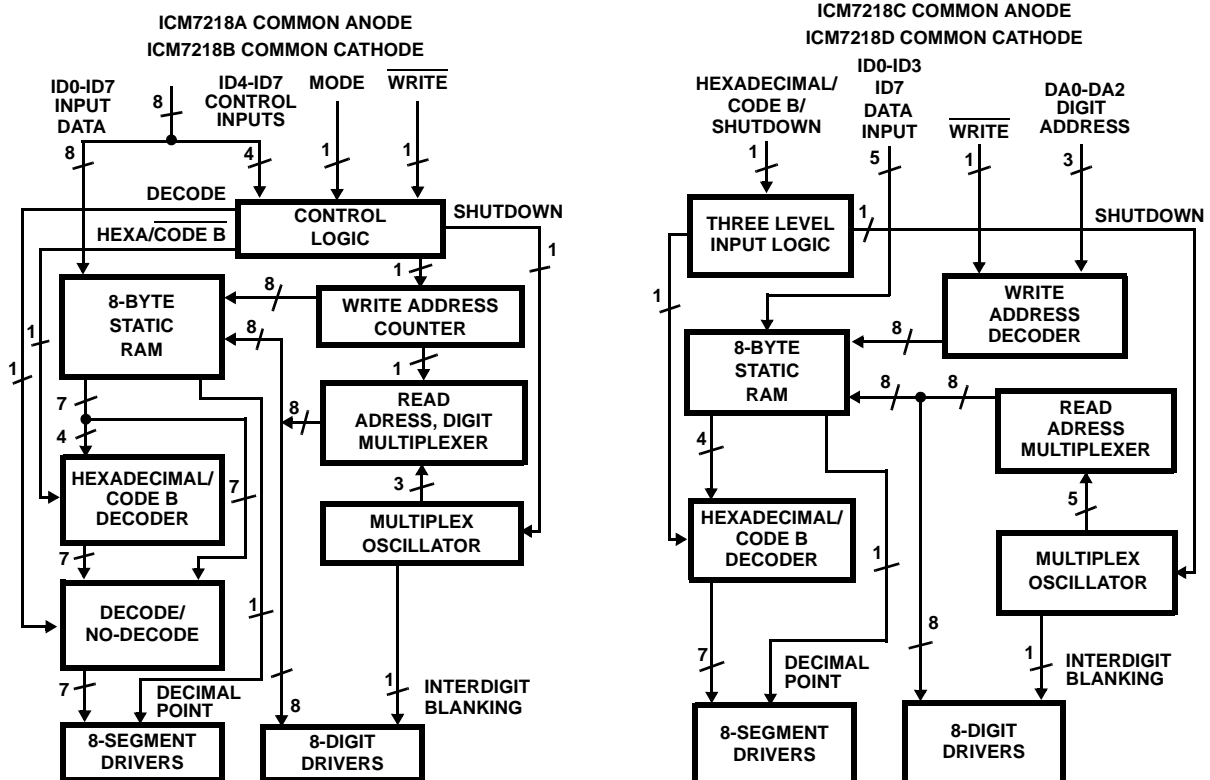- Technical Brief TB363 "Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)"
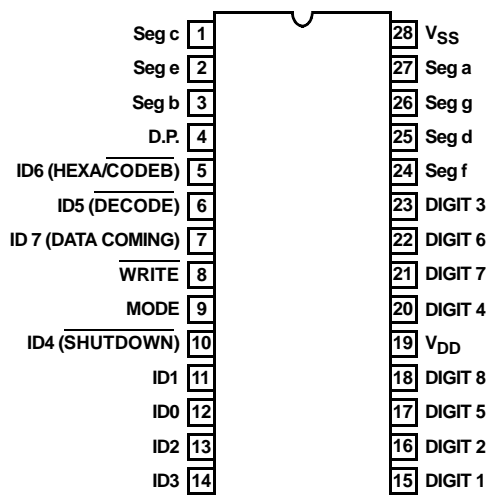

FIGURE 1. FUNCTIONAL DIAGRAMS

Ordering Information

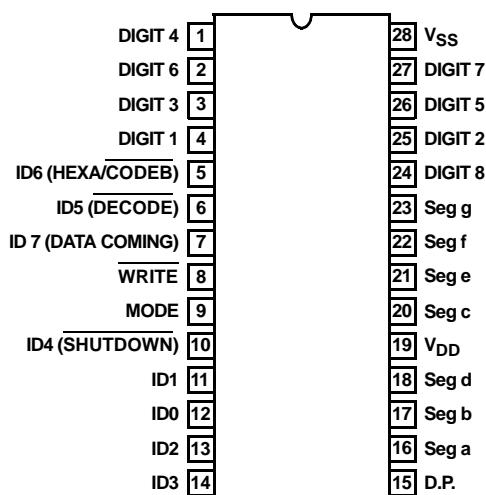| PART NUMBER	PART MARKING	DISPLAY TYPE	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ICM7218AIJI	ICM7218AIJI	Common Anode	-40 to +85	28 Ld CERDIP	F28.6
ICM7218AIJIR5254 (Note)	ICM7218AIJI R5254	Common Anode	-40 to +85	28 Ld CERDIP (Note)	F28.6
ICM7218BIJI	ICM7218BIJI	Common Cathode	-40 to +85	28 Ld CERDIP	F28.6
ICM7218BIJIR5254 (Note)	ICM7218BIJI R5254	Common Cathode	-40 to +85	28 Ld CERDIP (Note)	F28.6
ICM7218CIJI	ICM7218CIJI	Common Anode	-40 to +85	28 Ld CERDIP	F28.6
ICM7218CIJIR5254 (Note)	ICM7218CIJI R5254	Common Anode	-40 to +85	28 Ld CERDIP (Note)	F28.6
ICM7218DIJI	ICM7218DIJI	Common Cathode	-40 to +85	28 Ld CERDIP	F28.6
ICM7218DIJIR5254 (Note)	ICM7218DIJI R5254	Common Cathode	-40 to +85	28 Ld CERDIP (Note)	F28.6

NOTE: Intersil Pb-free hermetic packaged products employ SnAgCu or Au termination finish, which are RoHS compliant termination finishes and compatible with both SnPb and Pb-free soldering operations. Ceramic dual in-line packaged products (CerDIPs) do contain lead (Pb) in the seal glass and die attach glass materials. However, lead in the glass materials of electronic components are currently exempted per the RoHS directive. Therefore, ceramic dual inline packages with Pb-free termination finish are considered to be RoHS compliant.
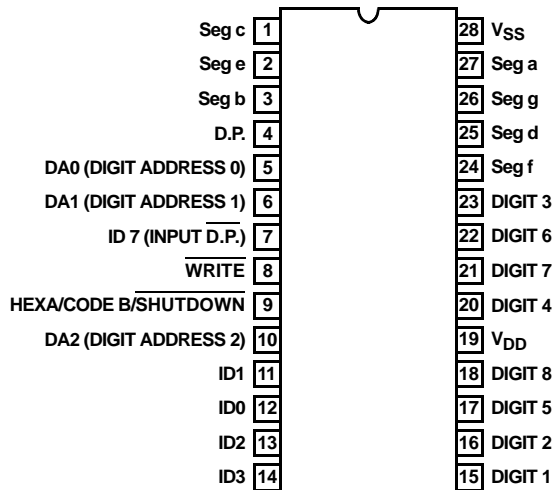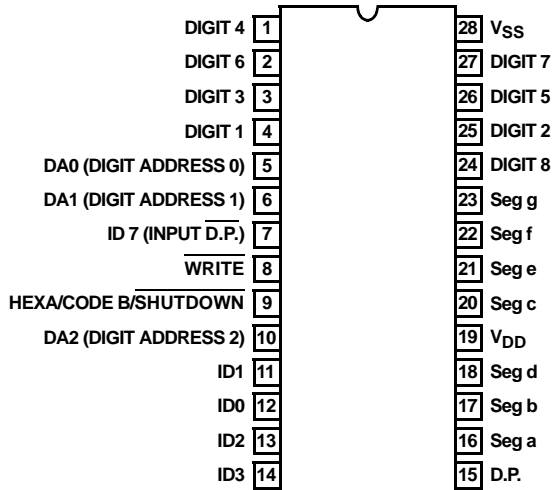
Pinouts

ICM7218A (28 LD CERDIP)
TOP VIEW

Pin	Signal		Pin	Signal
1	Seg c		28	V_{SS}
2	Seg e		27	Seg a
3	Seg b		26	Seg g
4	D.P.		25	Seg d
5	ID6 (HEXA/CODEB)		24	Seg f
6	ID5 (DECODE)		23	DIGIT 3
7	ID 7 (DATA COMING)		22	DIGIT 6
8	WRITE		21	DIGIT 7
9	MODE		20	DIGIT 4
10	ID4 (SHUTDOWN)		19	V_{DD}
11	ID1		18	DIGIT 8
12	ID0		17	DIGIT 5
13	ID2		16	DIGIT 2
14	ID3		15	DIGIT 1

ICM7218B (28 LD CERDIP)
TOP VIEW

Pin	Signal		Pin	Signal
1	DIGIT 4		28	V_{SS}
2	DIGIT 6		27	DIGIT 7
3	DIGIT 3		26	DIGIT 5
4	DIGIT 1		25	DIGIT 2
5	ID6 (HEXA/CODEB)		24	DIGIT 8
6	ID5 (DECODE)		23	Seg g
7	ID 7 (DATA COMING)		22	Seg f
8	WRITE		21	Seg e
9	MODE		20	Seg c
10	ID4 (SHUTDOWN)		19	V_{DD}
11	ID1		18	Seg d
12	ID0		17	Seg b
13	ID2		16	Seg a
14	ID3		15	D.P.

ICM7218A (28 LD CERDIP)
TOP VIEW

Pin	Signal		Pin	Signal
1	Seg c		28	V_{SS}
2	Seg e		27	Seg a
3	Seg b		26	Seg g
4	D.P.		25	Seg d
5	DA0 (DIGIT ADDRESS 0)		24	Seg f
6	DA1 (DIGIT ADDRESS 1)		23	DIGIT 3
7	ID 7 (INPUT D.P.)		22	DIGIT 6
8	WRITE		21	DIGIT 7
9	HEXA/CODE B/SHUTDOWN		20	DIGIT 4
10	DA2 (DIGIT ADDRESS 2)		19	V_{DD}
11	ID1		18	DIGIT 8
12	ID0		17	DIGIT 5
13	ID2		16	DIGIT 2
14	ID3		15	DIGIT 1

ICM7218B (28 LD CERDIP)
TOP VIEW

Pin	Signal		Pin	Signal
1	DIGIT 4		28	V_{SS}
2	DIGIT 6		27	DIGIT 7
3	DIGIT 3		26	DIGIT 5
4	DIGIT 1		25	DIGIT 2
5	DA0 (DIGIT ADDRESS 0)		24	DIGIT 8
6	DA1 (DIGIT ADDRESS 1)		23	Seg g
7	ID 7 (INPUT D.P.)		22	Seg f
8	WRITE		21	Seg e
9	HEXA/CODE B/SHUTDOWN		20	Seg c
10	DA2 (DIGIT ADDRESS 2)		19	V_{DD}
11	ID1		18	Seg d
12	ID0		17	Seg b
13	ID2		16	Seg a
14	ID3		15	D.P.

Absolute Maximum Ratings

Supply Voltage (V_{DD} to V_{SS}). 6V
Digit Output Current. 300mA
Segment Output Current 50mA
Input Voltage (Any Terminal)(Note 1). . . . . V_{SS} -0.3V to V_{DD} + 0.3V

Operating Conditions

Temperature Range. . . . . -40°C to +85°C

Thermal Information

Thermal Resistance (Typical, Note 2) θ_{JA} (°C/W) θ_{JC} (°C/W)
  CERDIP Package.   55   14
Maximum Storage Temperature Range . . . .-65°C to +150°C
Maximum Lead Temperature (Soldering 10s) . . . . +300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. Due to the SCR structure inherent in the CM0S process used to fabricate these devices, connecting any terminal to a voltage greater than V_{DD} or less than V_{SS} may cause destructive device latchup. For this reason it is recommended that no inputs from sources operating on a different power supply be applied to the device before its own supply is established, and when using multiple supply systems the supply to the ICM7218 should be turned on first.

2. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications V_{DD} = 5V, V_{SS} = 0V, T_A = +25°C, Display Diode Drop = 1.7V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{SUPPLY}	Operating	4	-	6	V
		Power Down Mode	2	-	6	V
Quiescent Supply Current	I_Q	Shutdown (Note 3)	6	10	300	μA
Operating Supply Current - Outputs Open Circuit	I_{DD}	Common Anode SEGS On (Note 6)	-	-	2.5	mA
		Common Anode SEGS Off (Note 6)	-	-	500	μA
		Common Cathode SEGS On (Note 6)	-	-	700	μA
		Common Cathode SEGS Off (Note 6)	-	-	500	μA
Digit Drive Current	I_{DIG}	Common Anode V_{OUT} = V_{DD} -2.0V	140	200	-	mA
		Common Cathode V_{OUT} = V_{SS} +1.0V	50	100	-	mA
Digit Leakage Current - Shutdown Mode	I_{DLK}	Common Anode V_{OUT} = 2V	-	-	100	μA
		Common Cathode V_{OUT} = 5V	-	-	100	μA
Peak Segment Drive Current	I_{SEG}	Common Anode V_{OUT} = V_{SS} +1.0V	20	40	-	mA
		Common Anode V_{OUT} = V_{DD} -2.0V	-10	-20	-	mA
Segment Leakage Current - Shutdown Mode	I_{SLK}	Common Anode V_{OUT} = V_{DD}	-	-	100	μA
		Common Cathode V_{OUT} = V_{SS}	-	-	100	μA
Display Scan Rate	f_{MUX}	Per Digit	-	250	-	Hz
Three Level Input (Pin 9 ICM7218C/D)						
Logical "1" Input Voltage	V_{IH}	Hexadecimal	4.5	-	-	V
Floating Input	V_{IF}	Code B	2.0	-	3.0	V
Logical "0" Input Voltage	V_{IL}	Shutdown	-	-	0.4	V
Three Level Input Impedance	Z_{IN}	Note 3	-	100	-	kΩ
Logical "1" Input Voltage	V_{IH}		3.5	-	-	V
Logical "0" Input Voltage	V_{IL}		-	-	0.8	V
Wrtie Pulse Width (Low)	t_{WL}	7218A, 7218B	550	400	-	ns
		7218C, 7218D	400	250	-	ns
Mode Hold Time	t_{MH}	7218A, 7218B	150	-	-	ns
Mode Setup Time	t_{MS}	7218A, 7218B	500	-	-	ns
Data Setup Time	t_{DS}		500	-	-	ns
Data Hold Time	t_{DH}	7218A, 7218B	50	-	-	ns
		7218C, 7218D	125	-	-	ns
Digital Address Setup Time	t_{AS}	7218C, 7218D	500	-	-	ns

Electrical Specifications V_{DD} = 5V, V_{SS} = 0V, T_A = +25°C, Display Diode Drop = 1.7V   **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Digital Address Hold Time	t_{AH}	7218C, 7218D	0	-	-	ns
Data Input Impedance	Z_{IN}	5-10pF Gate Capacitance	-	10^{10}	-	Ω

Pin Descriptions

INPUT		TERMINAL	LOGIC LEVEL	FUNCTION
ICM7218A AND ICM7218B				
WRITE		8	High	Input Not Loaded
			Low	Input Loaded
MODE		9	High	Load Control Bits on Write Pulse
			Low	Load Input Data on Write Pulse
ID4 (SHUTDOWN)	MODE High	10	High	Normal Operation
			Low	Shutdown (Oscillator, Decoder and Display Disabled)
ID5 (DECODE)		6	High	No Decode
			Low	Decode
ID6 (HEXA/CODE B)		5	High	Hexadecimal Decoding
			Low	Code B Decoding
ID7 (DATA COMING)		7	High	Data Coming } Control Word
			Low	No Data Coming
ID0-ID7	MODE Low	11, 12, 13, 14, 5, 6, 10, 7		Display Data Inputs (Notes 4, 5)
ICM7218C AND ICM7218D				
WRITE		8	High	Input Not Loaded into Memory
			Low	Input Loaded into Memory
HEXA/CODE B/ SHUTDOWN		9 (Note 3)	High	Hexadecimal Decoding
			Floating	Code B Decoding
			Low	Shutdown (Oscillator, Decoder and Display Disabled)
DA0 - DA2		10, 6, 5		Digit Address Inputs
ID0 - ID3		14, 13, 11, 12		Display Data Inputs
ID7 (INPUT D.P.)		7		Decimal Point Input

NOTES:

3. In the ICM7218C and D (random access versions) the HEXA/CODE B/SHUTDOWN input (Pin 9) has internal biasing resistors to hold it at V_{DD}/2 when Pin 9 is open-circuited. These resistors consume power and result in a quiescent supply current (I_Q) of typically 50µA. The ICM7218A, and B devices do not have these biasing resistors and thus are not subject to this condition.

4. ID0-ID3 = Don't Care when writing control data.
ID4-ID6 = Don't Care when writing Hex/Code B data.
ID7 = Decimal Point data.
(The display blanks on ICM7218A/B versions when writing in data).

5. In the No Decode format, "Ones" represents "on" segments for all inputs except for the Decimal Point, where "Zero" represents an "on" segment (i.e., segments are positive true, decimal point is negative true).

6. Common Anode segment drivers and Common Cathode Digit Drivers have 20kΩ pullup resistors.
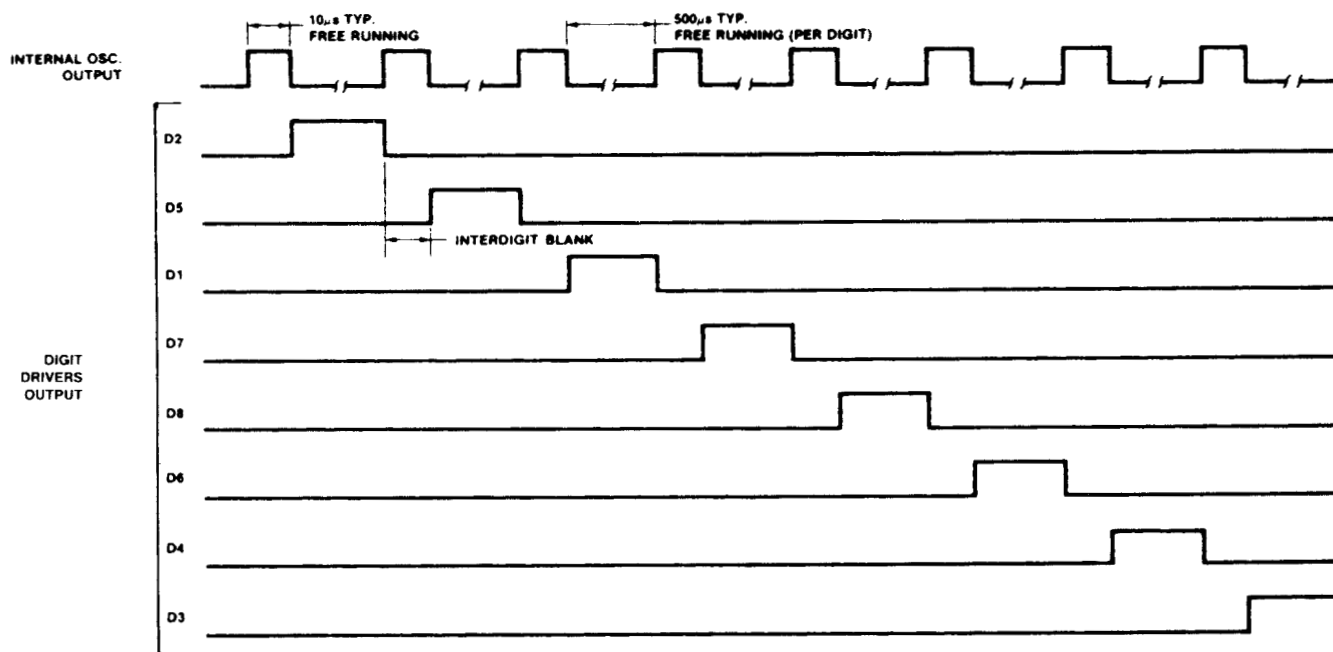
FIGURE 2. MULTIPLEX TIMING (COMMON CATHODE VERSION)
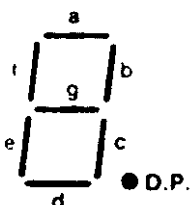
FIGURE 3. SEGMENT ASSIGNMENTS

Detailed Description

DECODE Operation

For the ICM7218A/B products, there are 3 input data formats possible; either direct segment and decimal point information (8 bits per digit) or two Binary formats plus decimal point information (Hexadecimal/Code B formats with 5 bits per digit).

The 7-segment decoder on chip is disabled when direct segment information is to be written. In this format, the inputs directly control the outputs as follows:

Input Data:	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
Output Segments:	D.P.	a	b	c	e	g	f	d

Here, "Ones" represent "on" segments for all inputs except the Decimal Point. For the Decimal Point "zero" represents an "on" segment.

HEXAdecimal/CODE B Decoding

For all products, a choice of either HEXA or Code B decoding may be made. HEXA decoding provides 7-segment numeric plus six alpha characters while Code B provides a negative

sign (-), a blank (for leading zero blanking), certain useful alpha characters and all numeric formats.

The four bit binary code is set up on inputs ID3-ID0, and decimal point data is set up on ID7.

DECIMAL	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
HEXA CODE	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
CODE B	0	1	2	3	4	5	6	7	8	9	-	E	H	L	P	(BLANK)

SHUTDOWN

SHUTDOWN performs several functions: it puts the device into a very low dissipation mode (typically $10\mu A$ at $V_{DD} = 5V$), turns off both the digit and segment drivers, and stops the multiplex scan oscillator (this is the only way the scan oscillator can be disabled). However, it is still possible to input data to the memory during shutdown - only the display output sections of the device are disabled in this mode.

Powerdown

In the Shutdown Mode, the supply voltage may be reduced to 2V without data in memory being lost. However, data should not be written into memory if the supply voltage is less than 4V.

Output Drive

The common anode output drive is approximately 200mA per digit at a 12% duty cycle. With segment peak drive current of 40mA typically, this results in 5mA average drive. The common cathode drive capability is approximately one-half that of the common anode drive. If high impedance LED displays are used, the drive current will be correspondingly less.

Inter Digit Blanking

A blanking time of approximately 10μs occurs between digit strobes. This ensures that the segment information is correct before the next digit drive, thereby avoiding display ghosting.

Driving Larger Displays

If a higher average drive current per digit is required, it is possible to connect digit drive outputs together. For example, by paralleling pairs of digit drivers together to drive a 4 digit display, 5mA average segment drive current can be obtained.

Power Dissipation Considerations

Assuming common anode drive at V_{DD} = 5V and all digits on with an average of 5 segments driven per digit, the average current would be approximately 200mA. Assuming a 1.8V drop across the LED display, there will be a 3.2V drop across the ICM7218. The device power dissipation will therefore be 640mW, rising to about 900mW, for all '8' 's displayed. **Caution: Position device in system such that air can flow freely to provide maximum cooling. The common cathode dissipation is approximately one-half that of the common anode dissipation.**

Sequential Addressing Considerations (ICM7218A/B)

The control instructions are read from the input bus lines if MODE is high and WRITE low. The instructions occur on 4 lines and are - DECODE/no Decode, type of Decode (if desired), SHUTDOWN/no Shutdown and DATA COMING/not Coming. After the control word has been written (with the Data Coming instruction), display data can be written into memory with each successive negative going WRITE pulse. After all 8-digit memory locations have been written to, additional transitions of the WRITE input are ignored until a new control word is written. It is not possible to change one individual digit without refreshing the data for all the other digits.

Random Access Input Drive Considerations (ICM7218C/D)

Control instructions are provided to the ICM7218C/D by a single three level input terminal (Pin 9), which operates independently of the WRITE pulse.

Data can be written into memory on the ICM7218C/D by setting up a 3 bit binary code (one of eight) on the digit address inputs and applying a low level to the WRITE pin. For example, it is possible to change only digit 7 without altering the data for the other digits. (See Figure 6).

Supply Capacitor

A 0.1μF plus a 47μF capacitor is recommended between V_{DD} and V_{SS} to bypass display multiplexed noise.
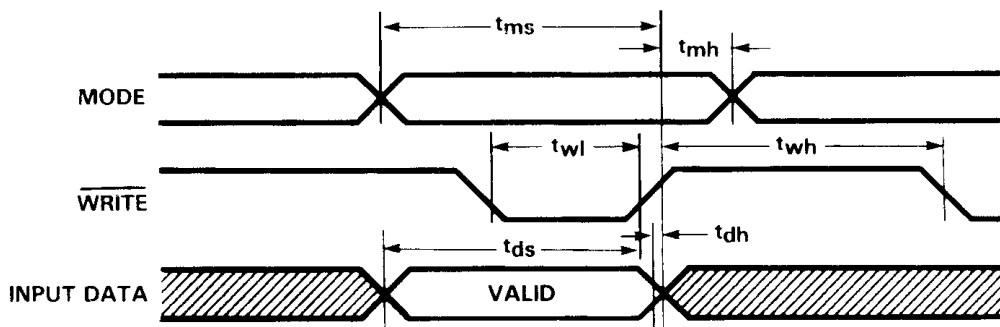
FIGURE 4. TIMING DIAGRAM FOR ICM7218A/B
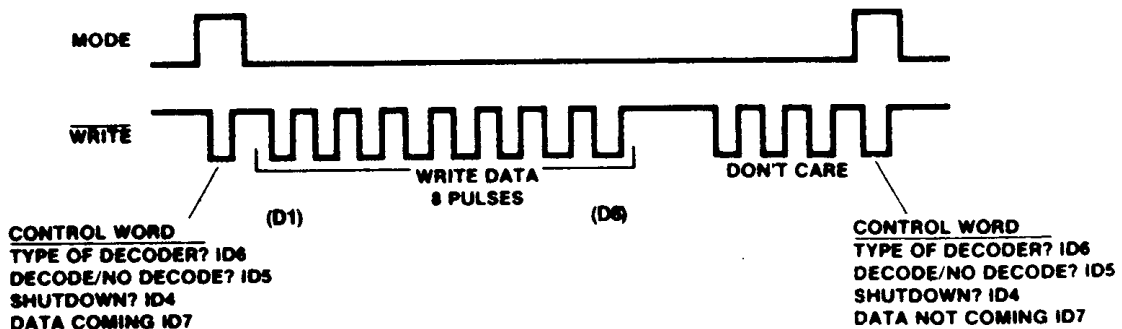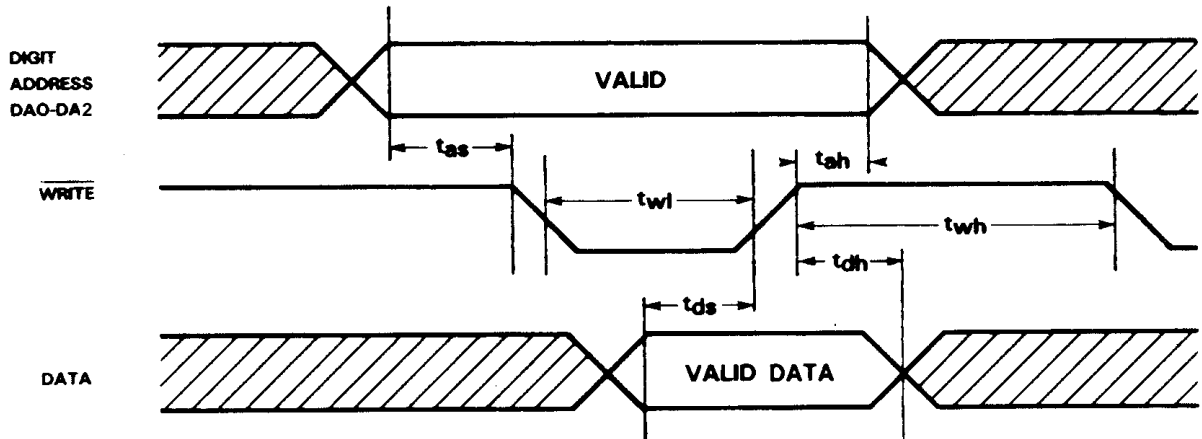

FIGURE 5. LOAD SEQUENCE ICM7218A/B

FIGURE 6. TIMING DIAGRAM FOR ICM7218C/D

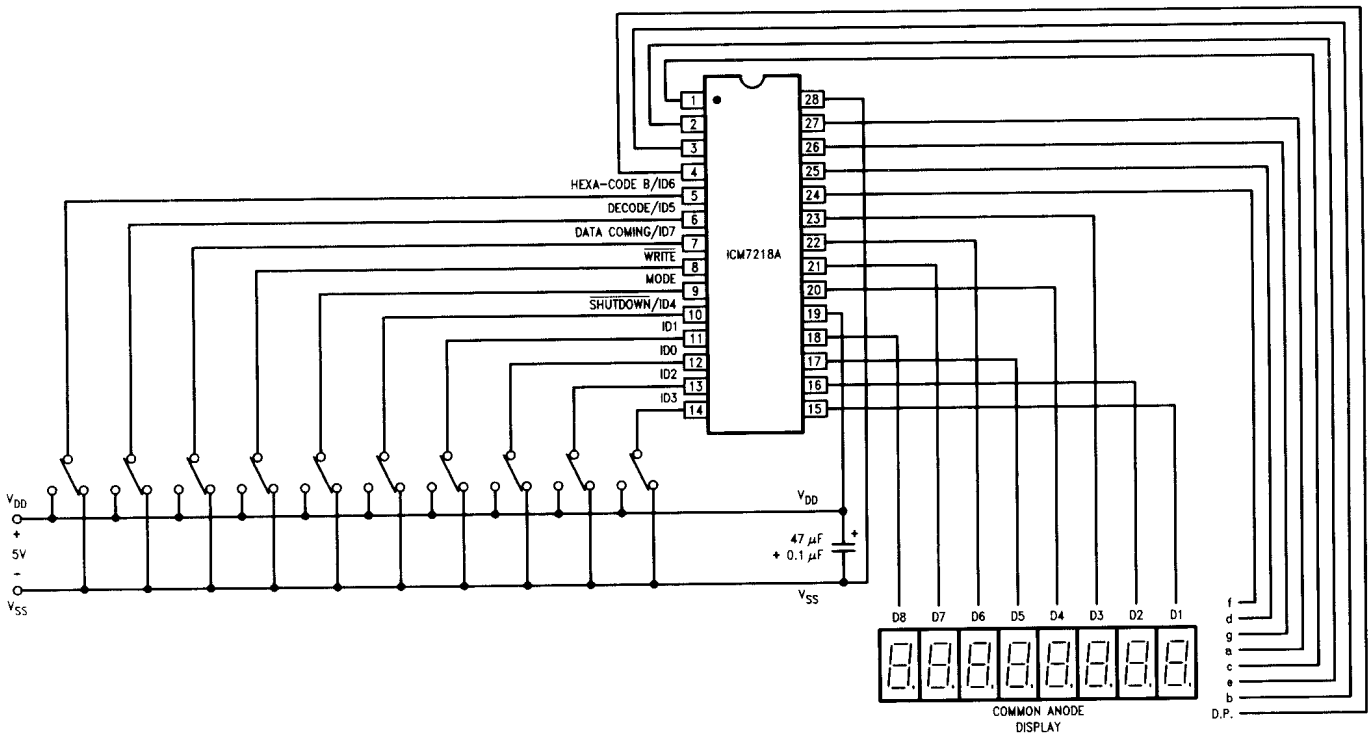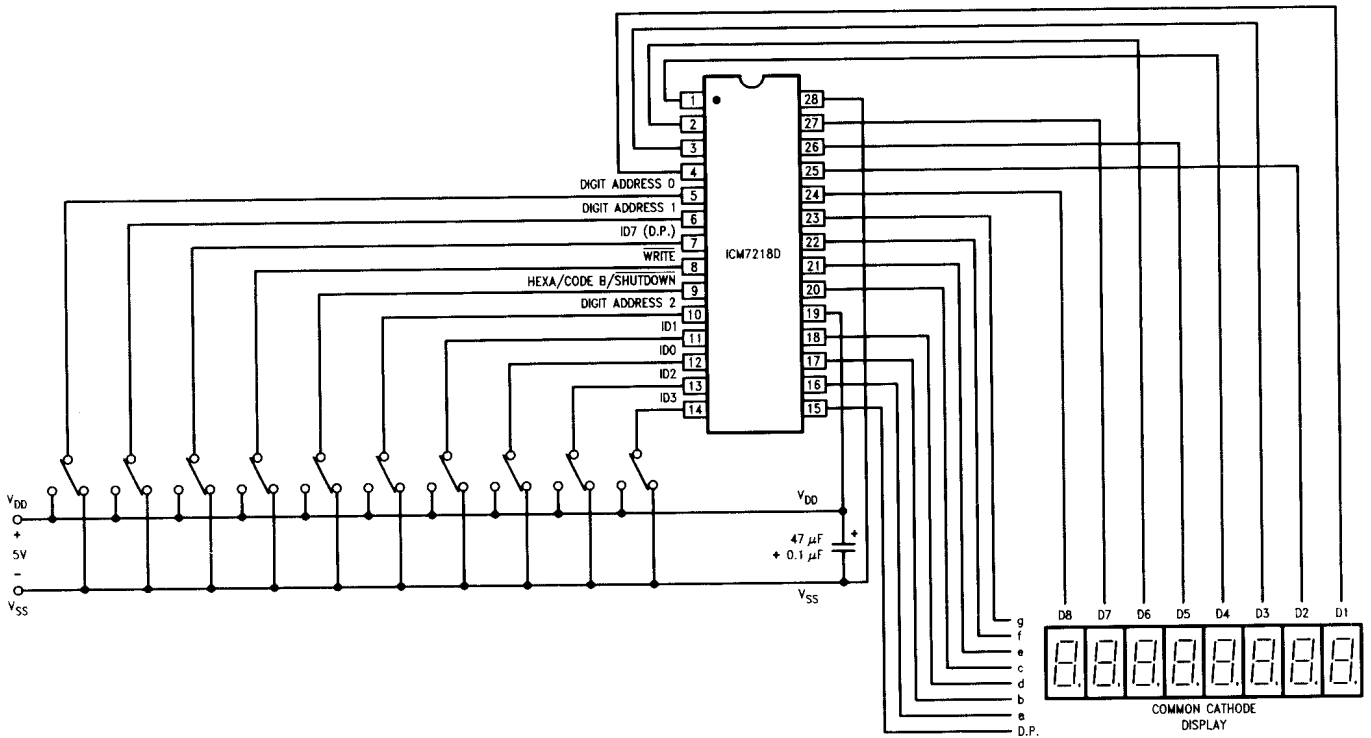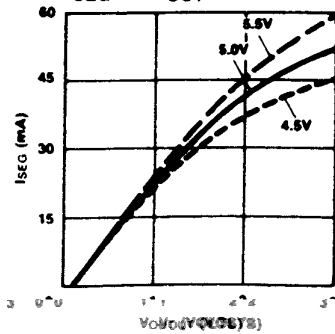**FIGURE 7. COMMON ANODE DISPLAY FUNCTIONAL TEST CIRCUIT**

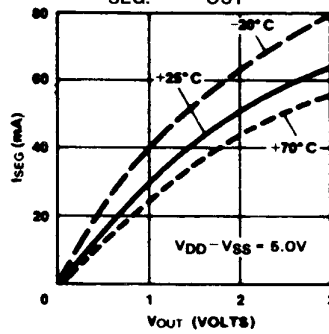**FIGURE 8. COMMON CATHODE DISPLAY FUNCTIONAL TEST CIRCUIT**

Typical Performance Characteristics
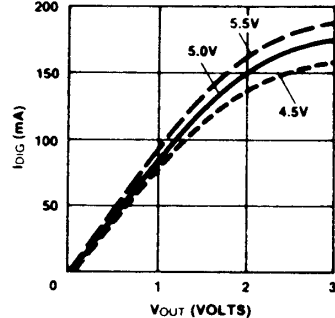

COMMON ANODE SEG. DRIVER
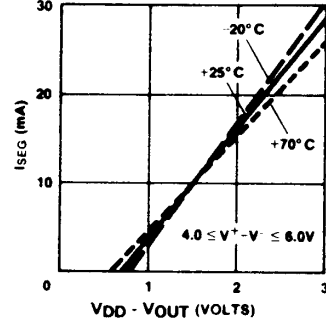I_{SEG} vs. V_{OUT} AT 25°C

COMMON ANODE SEG. DRIVER
I_{SEG} vs. V_{OUT}

COMMON ANODE DIGIT DRIVER
I_{DIG} vs. $(V_{DD} - V_{OUT})$
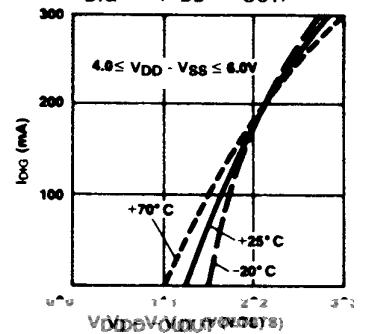
COMMON CATHODE DIGIT DRIVER
I_{DIG} vs. V_{OUT} AT 25°C

COMMON CATHODE SEG. DRIVER
I_{SEG} vs. $(V_{DD} - V_{OUT})$

COMMON CATHODE DIGIT DRIVER
I_{DIG} vs. V_{OUT}
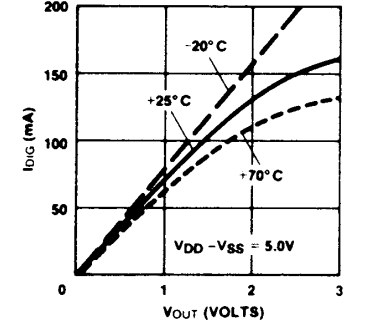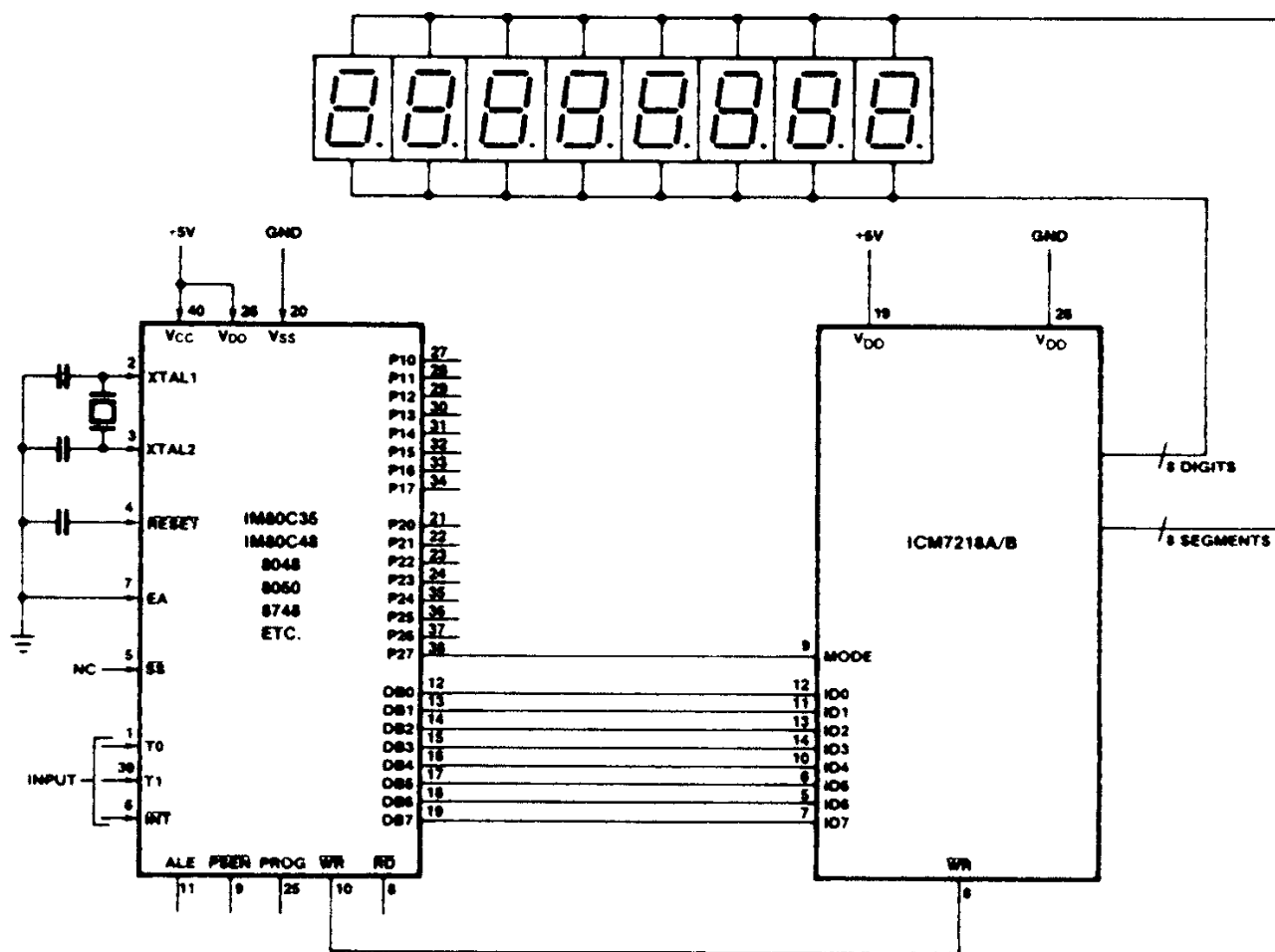
FIGURE 9. 8-DIGIT MICROPROCESSOR DISPLAY

Application Examples

8-Digit Microprocessor Display Application

Figure 9 shows a display interface using the ICM7218A/B with an 8048 family microcontroller. The 8 bit data bus (DB0/DB7-ID0/ID7) transfers control and data information to the 7218 display interface on successive $\overline{\text{WRITE}}$ pulses. The MODE input to the 7218 is connected to one of the I/O port pins on the microcontroller, When MODE is high a control word is transferred; when MODE is low data is transfered. Sequential locations in the 8-byte static memory are automatically loaded on each successive $\overline{\text{WRITE}}$ pulse. After eight $\overline{\text{WRITE}}$ pulses have occurred, further pulses are ignored until a new control word is transferred (See Figure 5). This also allows writing to other peripheral devices without disturbing the ICM7218A/B.

16-Digit Microprocessor Display

In this application (see Figure 10), both ICM7218s are addressed simultaneously with a 3 bit word, DA2-DA0. Display data from the 8048 I/O bus (DB7-D80) is transferred to both ICM7218s simultaneously.

The display digits from both ICM7218s are interleaved to allow adjacent pairs of digits to be loaded simultaneously from a single 8 bit data bus.

Decimal point information is supplied to the ICM7218s from the processor on port lines P26 and P27.

No Decode Application

The ICM7218 can also be used as a microprocessor based LED status panel driver. The microprocessor selected control word must include "No Decode" and "Data Coming". The processor writes "Ones" and "Zeroes" into the ICM7218 which in turn directly drives appropriate discrete LEDs. LED indicators can be red or green (8 segments x 8 digits = 64 dots/2 per red or green = 32 channels).

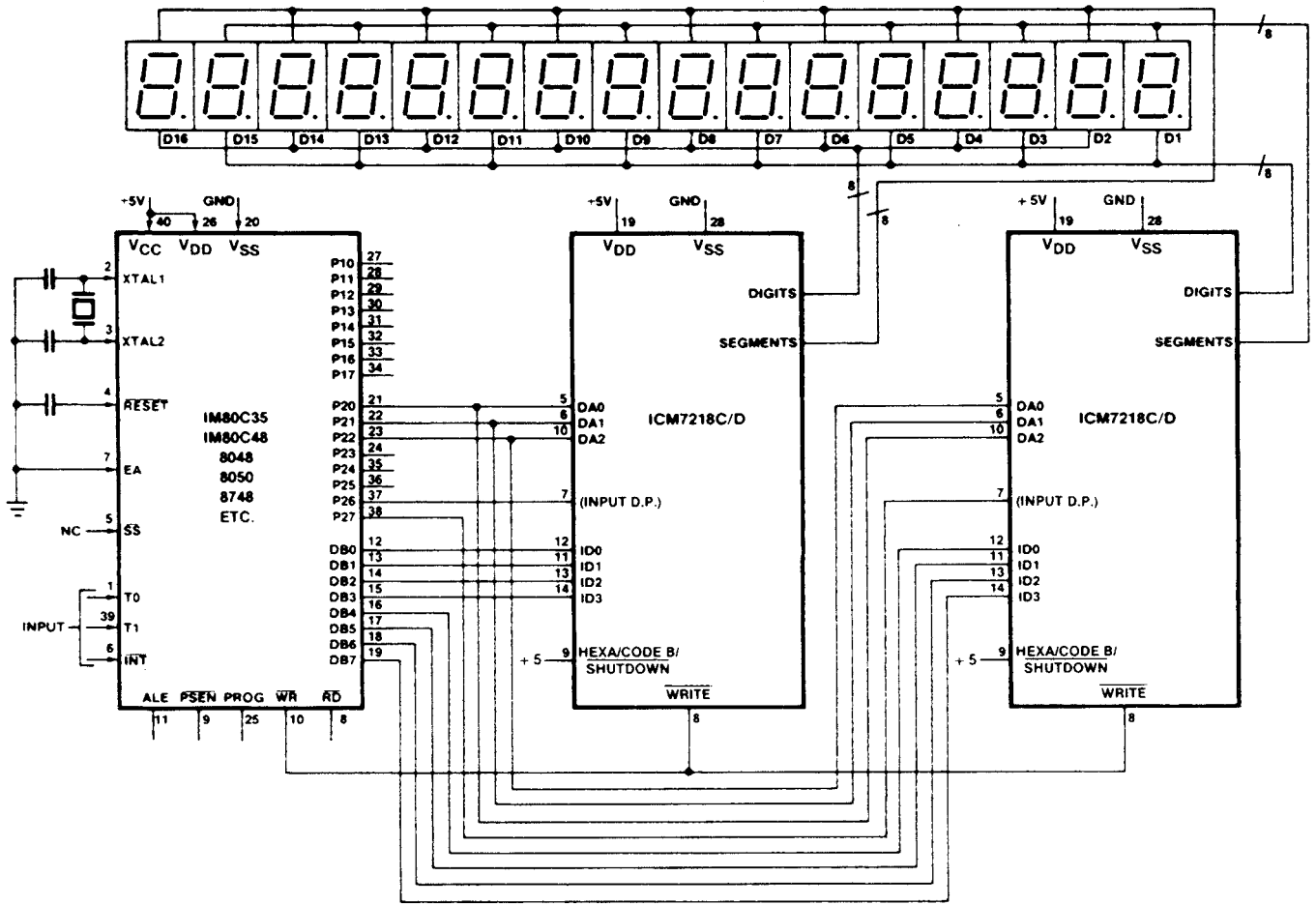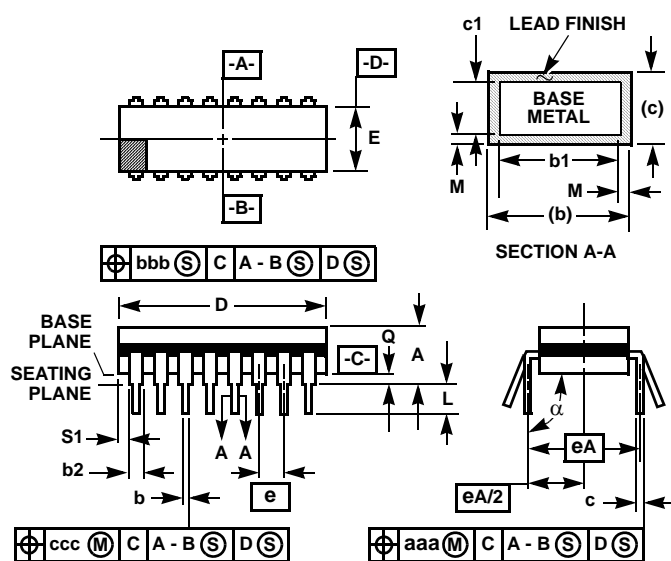**FIGURE 10. 16-DIGIT DISPLAY**

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)

F28.6 MIL-STD-1835 GDIP1-T28 (D-10, CONFIGURATION A)
28 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.232	-	5.92	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.490	-	37.85	5
E	0.500	0.610	12.70	15.49	5
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	28		28		8

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NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.

2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.

3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.

4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.

5. This dimension allows for off-center lid, meniscus, and glass overrun.

6. Dimension Q shall be measured from the seating plane to the base plane.

7. Measure dimension S1 at all four corners.

8. N is the maximum number of terminal positions.

9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.

10. Controlling dimension: INCH.

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