PT6552
½ Duty LCD Driver with On-Chip Key Input Function

DESCRIPTION

The PT6552 is ½ duty dynamic LCD display driver. In addition to being able to directly Drive LCD panels with up to 90 segments, it can also control up to 4 general purpose output ports. This product also includes a key scan circuit that allows it to accept input from keypads with up to 30 keys. This allows the end product front panel wiring to be simplified.

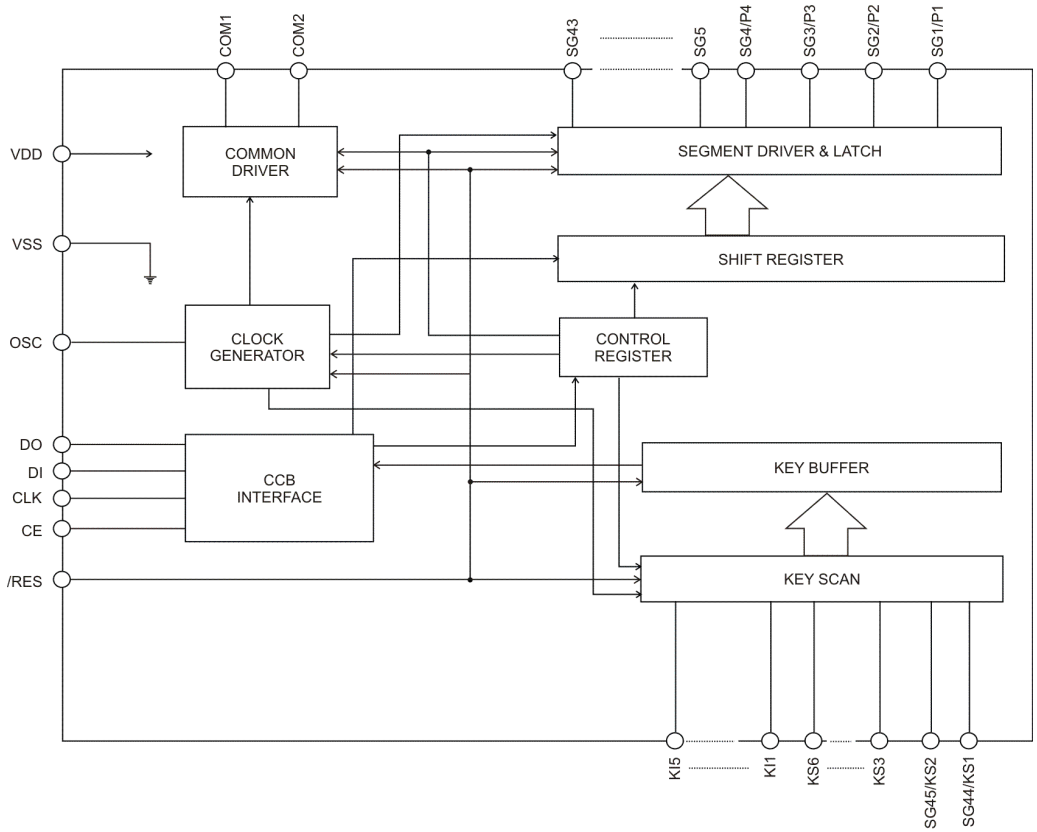
APPLICATIONS

- Cellular phone
- Data bank, organizer
- Electronic dictionary/translator
- P.D.A.
- P.O.S.
- Information appliance
- Caller ID
- Pager
- Electronic equipment with LCD display

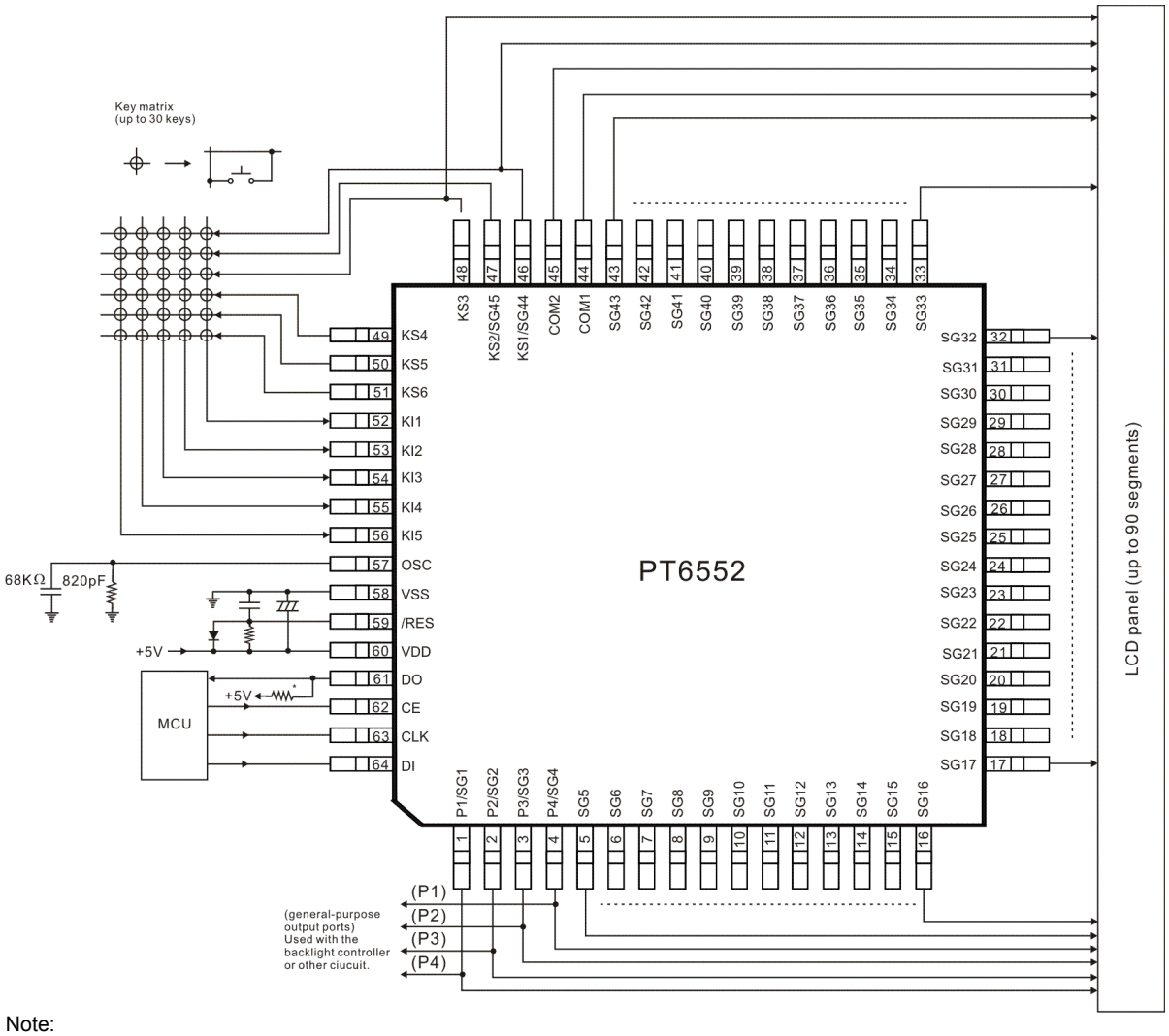
FEATURES

- Up to 4 general purpose output ports
- Up to 90 segments outputs
- Up to 30 key inputs (Key scan is only performed when a key is pressed)
- ½ duty - ½ bias (up to 90 segments)
- Serial data control sleep mode and the all segments off function
- Serial data controlled segment output port/general-purpose output port usage
- Serial data I/O supports CCB format communication with the system controller
- High generality since display data is displayed directly without decoder intervention
- Reset pin that can establish the initial state
- Available in 64 pin QFP and 64 pin LQFP package

BLOCK DIAGRAM



APPLICATION CIRCUIT

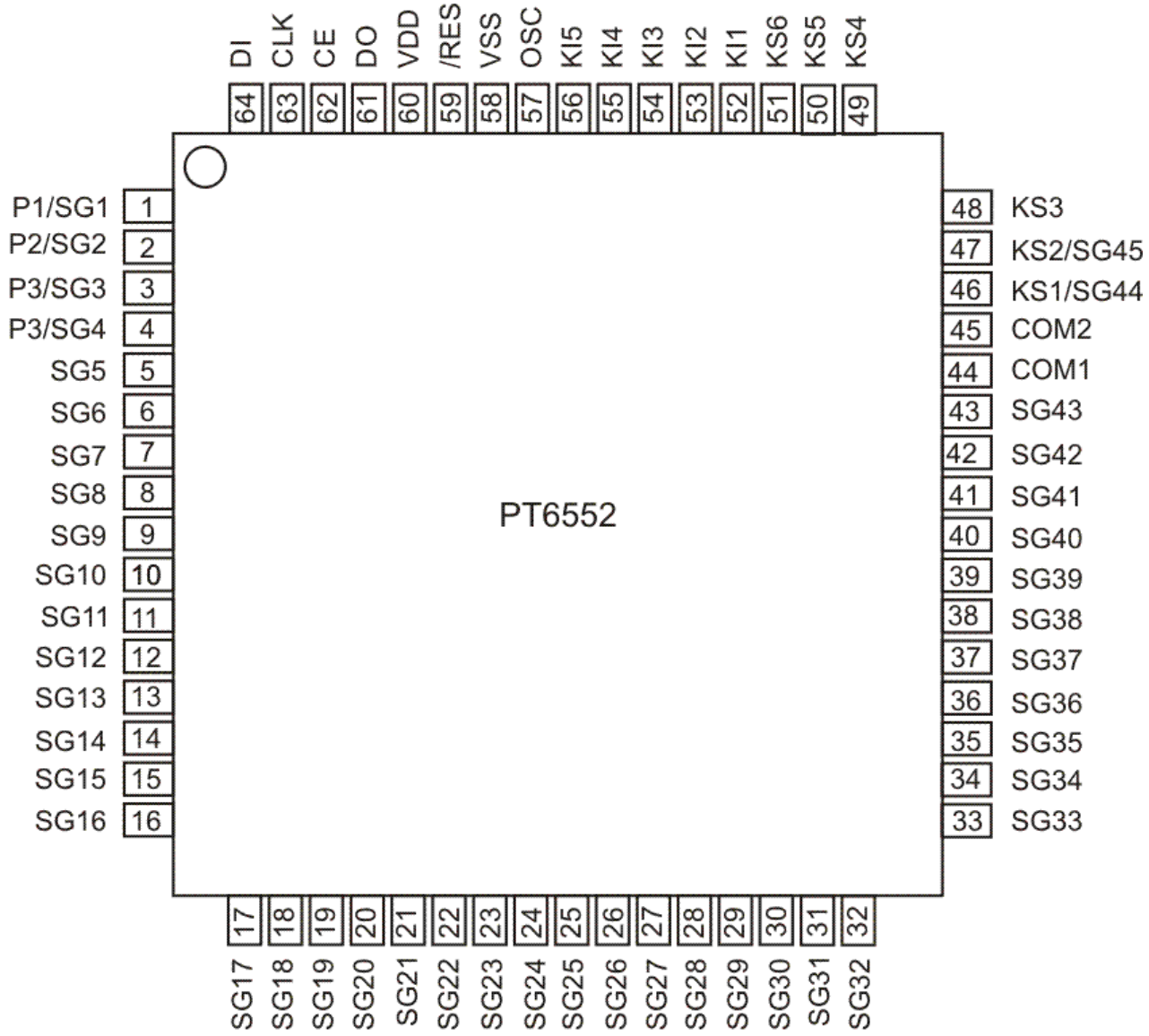


Note:
* Since DO is an open-drain output, a pull-up resistor is required. Select a value (between 1k and 10KΩ) that is appropriate for the capacitance of the external wiring so that the waveforms are not distorted.

ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT6552	64 Pin, QFP	PT6552
PT6552LQ	64 Pin, LQFP	PT6552LQ

PIN CONFIGURATION



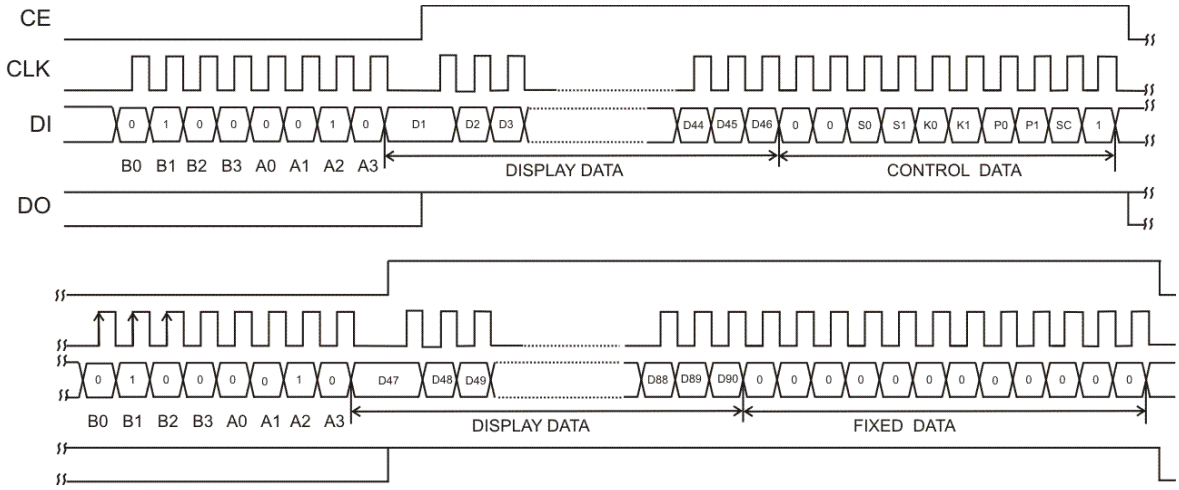
PIN CONFIGURATIONS

Pin Name	I/O	Function		Active	Handing when unused	Pin No.
SG1/P1 to SG4/P4 SG5 to SG43	O	Segment outputs: Used to output the display data that is transmitted over the serial data input. Pins SG1/P1 to SG4/P2 can be used as general-purpose outputs according to control data specification.		-	Open	1 to 4 5 to 43
COM1 COM2	O	Common driver outputs. The frame frequency fo is (fosc/512)Hz		-	Open	44 45
KS1/SG44, KS2/SG45, KS3 to KS6	O	Key scan outputs. When a key matrix is formed, normally a diode will be attached to the key scan timing line to prevent shorts. However, since the output transistor impedance is an unbalanced CMOS output, it will not be damaged if shorted. Pins KS1/SG44 and KS2/SG45 can be used as segment outputs according to control data specification.		-	Open	46 47 48 to 51
KI1 to KI5	I	Key scan inputs: Pin with a built-in pull-down resistor.		H	GND	52 to 56
OSC	I/O	Oscillator connection: Oscillator circuit can be formed by connecting the pin to a resistor and a capacitor		-	V_{DD}	57
V_{SS}	-	Power supply ground connected. Must be connected to GND.		-	-	58
/RES	I	Reset input that re-initializes the LSI internal states. During a reset, the display segments are turned off forcibly regardless of the internal display data. All internal key data is reset to low and the key scan operation is disabled. However, serial data can input during a reset.		L	GND	59
V_{DD}	-	Power supply connection. A supply voltage of between 4.5 and 6.0V must be provided.		-	-	60
DO	O	Serial data interface: Connected to the controller. Since DO is an open-drain output, it required a pull-up resistor.	CE: Chip enable CLK: Synchronization clock DI: Transfer data DO: Output data	-	Open	61
CE	I			H	GND	62
CLK	I			↑		63
DI	I			-		64

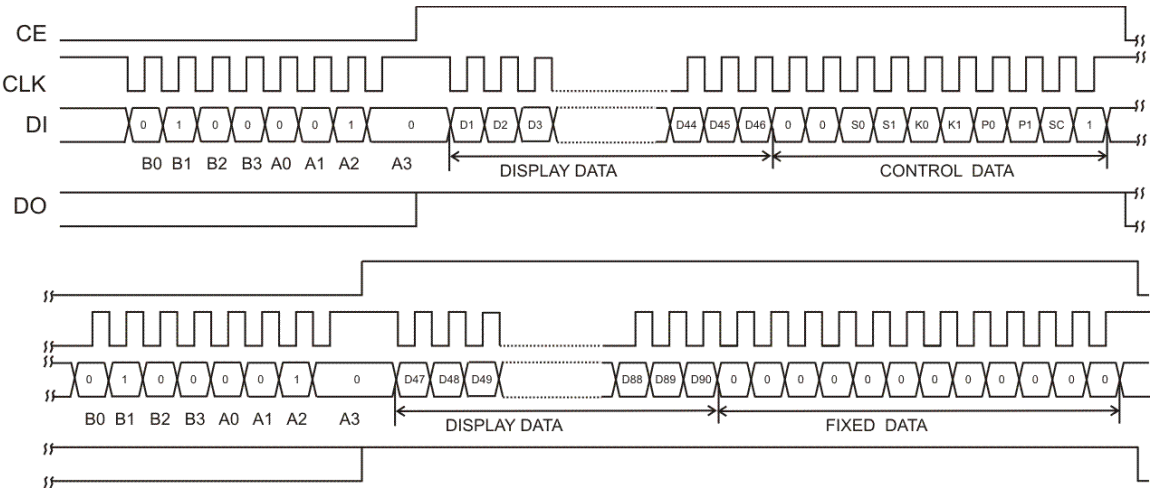
FUNCTION DESCRIPTION

SERIAL DATA INPUT

WHEN STOPPED WITH CLK AT THE LOW LEVEL



WHEN STOPPED WITH CLK AT THE HIGH LEVEL



CCB address: 42H
D1 to D90: Display data
S0, S1: Sleep control data
K0, K1: Key scan output/segment output selection data
P0, P1: Segment output port/general-purpose output port selection data
SC: Segment on/off control data

CONTROL SERIAL DATA FUNCTION

1. S0, S1: SLEEP CONTROL DATA

This control data switches the LSI between normal mode and sleep mode. It also sets the key scan output standby states for pinsKS1 to KS6.

Control Data		Mode	Oscillator	Segment outputs Common outputs	Key scan standby mode output pin states					
S0	S1				KS1	KS2	KS3	KS4	KS5	KS6
0	0	Normal	Oscillator	Operation	H	H	H	H	H	H
0	1	Sleep	Stopped	L	L	L	L	L	L	H
1	0	Sleep	Stopped	L	L	L	L	L	H	H
1	1	Sleep	Stopped	L	H	H	H	H	H	H

2. K0, K1: KEY SCAN OUTPUT/SEGMENT OUTPUT SELECTION DATA

This control data switches the KS1/SG44 and KS2/SG45 output pins between the key scan output and segment output function.

Control data		Output pin states		Maximum number of key inputs
K0	K1	KS1/SG44	KS2/SG45	
0	0	KS1	KS2	30
0	1	SG44	KS2	25
1	X	SG44	SG45	20

X: don't care

3. P0, P1: SEGMENT OUTPUT PORT/GENERAL-PURPOSE OUTPUT PORT SELECTION DATA

This control data switches the SG1/P1 to SG4/P4 output pins between the segment output port and the general-purpose output port function.

Control data		Output pin states			
P0	P1	SG1/P1	SG2/P2	SG3/P3	SG4/P4
0	0	SG1	SG2	SG3	SG4
0	1	P1	P2	SG3	SG4
1	0	P1	P2	P3	SG4
1	1	P1	P2	P3	P4

The table below lists the correspondence between the display data and the output pins when the general-purpose output port function is selected.

Output pin	Corresponding display data
SG1/P1	D1
SG2/P2	D3
SG3/P3	D5
SG4/P4	D7

For example, if the output pin SG4/P4 is set for use as a general-purpose output port, the output pin SG4/P4 will output a high level when the display data D7 is 1.

4. SC: SEGMENT ON/OFF CONTROL DATA

This control data controls the segment on/off states.

SC	Display states
0	On
1	Off

DISPLAY DATA L SERIAL DATA FUNCTION

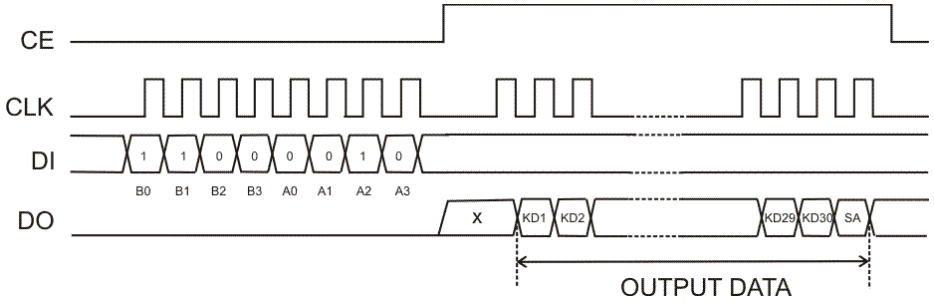
Output Pin	COM1	COM2
SG1/P1	D1	D2
SG2/P2	D3	D4
SG3/P3	D5	D6
SG4/P4	D7	D8
SG5	D9	D10
SG6	D11	D12
SG7	D13	D14
SG8	D15	D16
SG9	D17	D18
SG10	D19	D20
SG11	D21	D22
SG12	D23	D24
SG13	D25	D26
SG14	D27	D28
SG15	D29	D30
SG16	D31	D32
SG17	D33	D34
SG18	D35	D36
SG19	D37	D38
SG20	D39	D40
SG21	D41	D42
SG22	D43	D44
SG23	D45	D46
SG24	D47	D48
SG25	D49	D50
SG26	D51	D52
SG27	D53	D54
SG28	D55	D56
SG29	D57	D58
SG30	D59	D60
SG31	D61	D62
SG32	D63	D64
SG33	D65	D66
SG34	D67	D68
SG35	D69	D70
SG36	D71	D72
SG37	D73	D74
SG38	D75	D76
SG39	D77	D78
SG40	D79	D80
SG41	D81	D82
SG42	D83	D84
SG43	D85	D86
KS1/SG44	D87	D88
KS2/SG45	D89	D90

For example, the output states of output pin SG11 are listed in the table below.

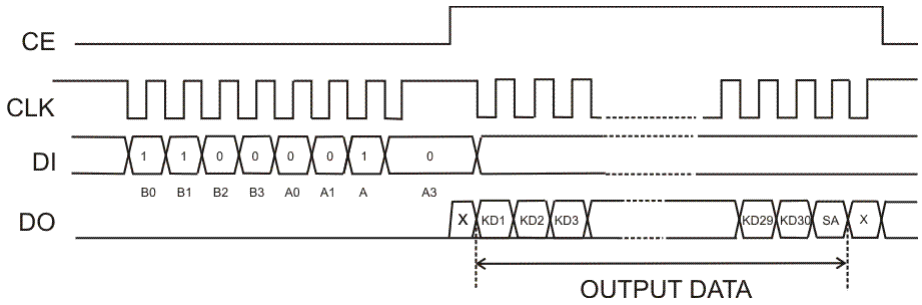
Display data		Output pin state
D21	D22	SG11
0	0	Segment off for both COM1 and COM2
0	1	Segment on for COM2
1	0	Segment on for COM1
1	1	Segment on for both COM1 and COM2

SERIAL DATA OUTPUT

WHEN STOPPED WITH CLK AT THE LOW LEVEL



WHEN STOPPED WITH CLK AT THE HIGH LEVEL



CCB address: 43H
KD1 to KD30: Key data
SA: Sleep acknowledge data

Note: If key data is read when DO is high, the key data (KD1 to KD30) and sleep acknowledge data (SA) will be invalid.

OUTPUT DATA

KD1 TO KD30: KEY DATA

When a key matrix with up to 30 keys is formed using the KS1 to KS6 output pins and the KI1 to KI5 input pins, the key data corresponding to given key will be 1 if that key is pressed. The table below lists that correspondence.

Item	KI1	KI2	KI3	KI4	KI5
KS1/SG44	KD1	KD2	KD3	KD4	KD5
KS2/SG45	KD6	KD7	KD8	KD9	KD10
KS3	KD11	KD12	KD13	KD14	KD15
KS4	KD16	KD17	KD18	KD19	KD20
KS5	KD21	KD22	KD23	KD24	KD25
KS6	KD26	KD27	KD26	KD29	KD30

When the output pins KS1/SG44 and KS2/SG45 are selected for segment output by the control data K0 and K1, the key data items KD1 to KD10 will be 0.

SA: SLEEP ACKNOWLEDGE DATA

This output data is set according to the state when the key was pressed. If the LSI was in sleep mode, SA will be 1, and if the LSI was in normal mode, SA will be 0.

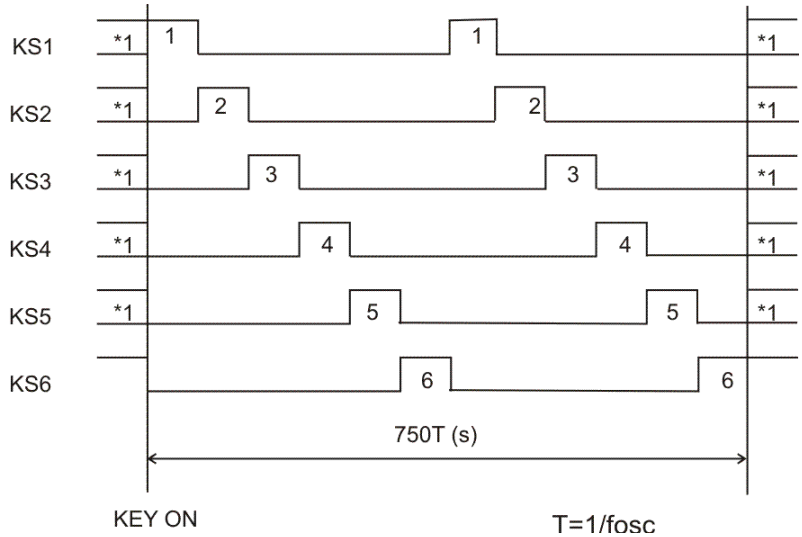
SLEEP MODE

When S0 or S1 in the control data is set to 1, the oscillator at the OSC pin will stop (it will restart if a key is pressed) and the segment and common outputs will all go to the low level. This reduces the LSI power dissipation. However, the SG1/P1 to SG4/P4 output pins can be used as general-purpose output ports even in sleep mode if selected for such use by the P0 and P1 control data bits

KEY SCAN OPERATING

KEY SCAN TIMING

The key scan period is 375T[s]. The key scan is performed twice to reliably determine the key on/off states, and the LSI detects key data agreement. When the key data agrees, the LSI determines that a key has been pressed, and outputs a key read request (by setting DO low) 800T[s] after the key scan started. If a key is pressed again without the key data agreeing, a key scan is performed 1=once more. Thus key on/off operations shorter than 800T[s] cannot be detected.

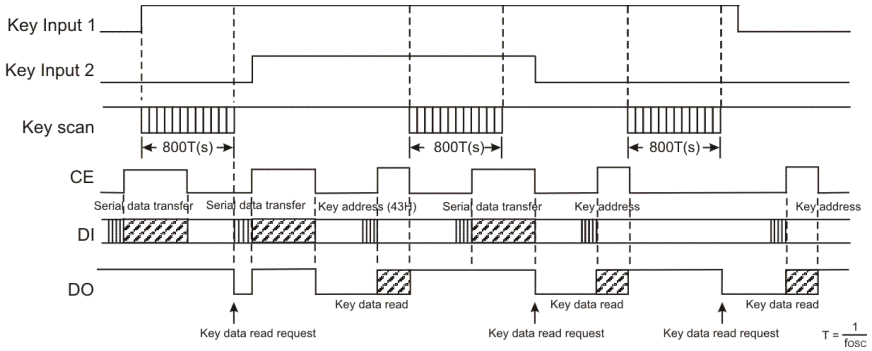


Note:
*1: The high or low states of these signals in sleep mode are determined by the S0 and S1 control data bits.

KEY SCAN DURING NORMAL MODE

The pins KS1 to KS6 are set high. A key scan starts if any key is pressed, and the scan continues until all keys have been released. Multiple key pressed can be recognized be determining if multiple key data bits have been set. When a key has been pressed for 800T[s] (when T=1/fosc) or longer, a key data read request (DO is set to low) is output to the controller. The controller acknowledges this request and reads the key data; however, DO will go high when CE is high during a serial data transfer.

After the controller has finished reading the key data, the LSI clears the key data read request (by setting DO high) and performs another key scan. Note that since DO is an open drain output, a pull-up resistor of between 1K and 10KΩ is required.

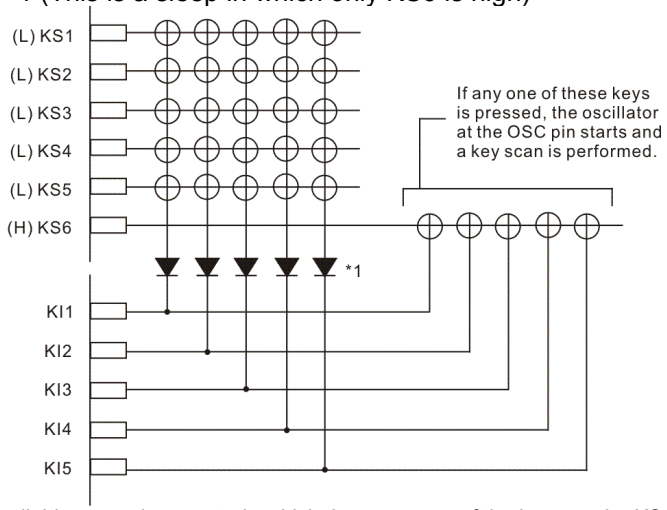


KEY SCAN DURING SLEEP MODE

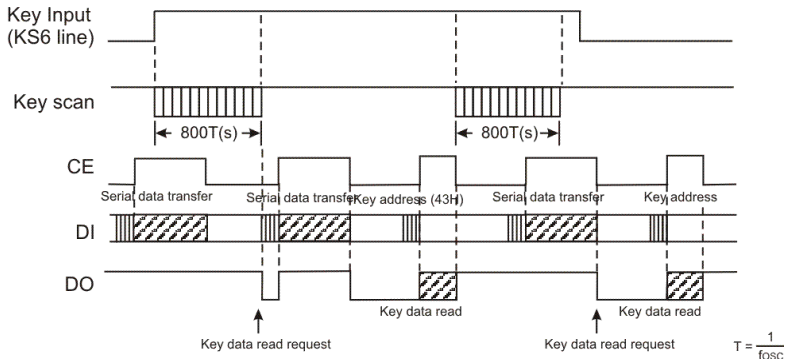
The pins KS1 to KS6 are set high or low according to the S0 and S1 control data bits. (see the description of the control data function for details)If a key for a line corresponding to one of the pins KS1 to KS6 which is high is pressed, the oscillator at the OSC pin starts and a key scan is performed. The key scan continues until all keys have been released.

Multiple key presses can be recognized by determining if multiple key data bits have been set. When a key has been pressed for 800T[s] (where T=1/fosc) or longer, a key data read request (D0 is set to low) is output to the controller. The controller acknowledges this request and reads the key data; however, DO will go high when CE is high during a serial data transfer. After the controller has finished reading the key data, the LSI clears the key data read request (by setting DO high) and performs another key scan. Note that since DO is an open drain output, a pull-up resistor of between 1k and 10KΩ is required. Key scan example in sleep mode.

Example: Here S0 = 0 and S1 = 1 (This is a sleep in which only KS6 is high)



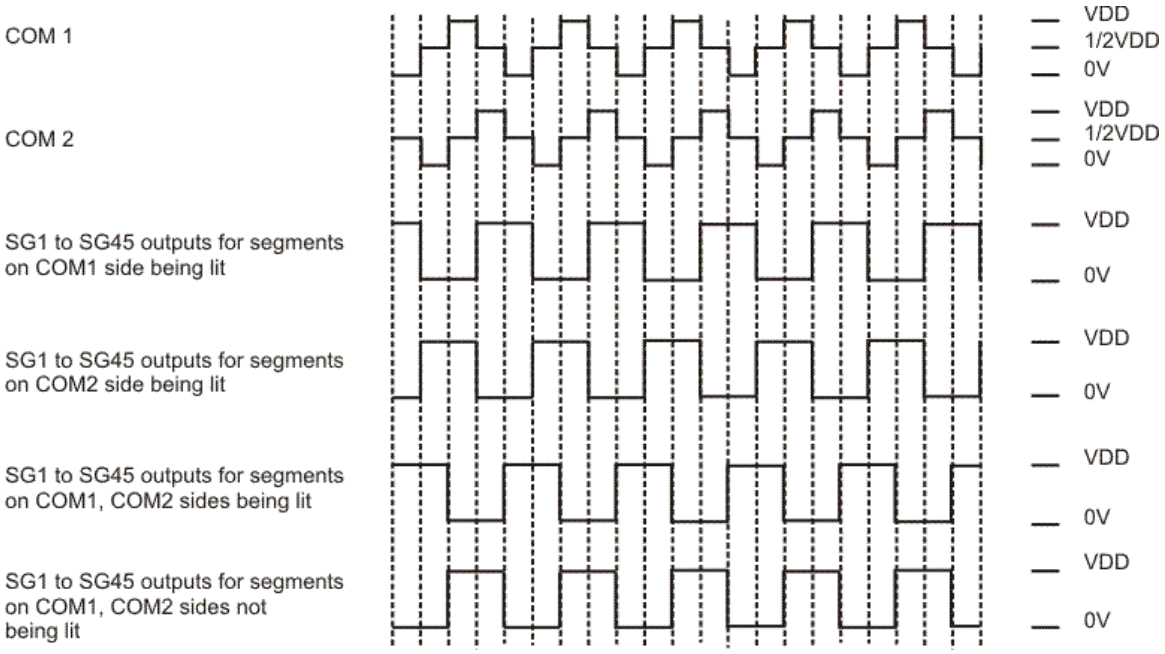
Note: *1=These diodes are required to reliably recognize events in which three or more of the keys on the KS6 line are pressed at the same time.



MULTIPLE KEY PRESSES

Without the insertion of additional diodes, the PT6552 supports key scan for double key presses in general, triple key presses of keys on the lines for input pins KI1 to KI5, and multiple key pressed of keys on the lines for the output pins KS1 to KS6. However, if multiple key presses in excess of these limits occur, the PT6552 may recognize keys that were not pressed as having been pressed. Therefore, series diodes must be connected to each key.

½ DUTY – ½ BIAS LCD DRIVE SCHEME



NTERNAL BLOCK STATES DURING THE RESET PERIOD (WHEN /RES IS LOW)

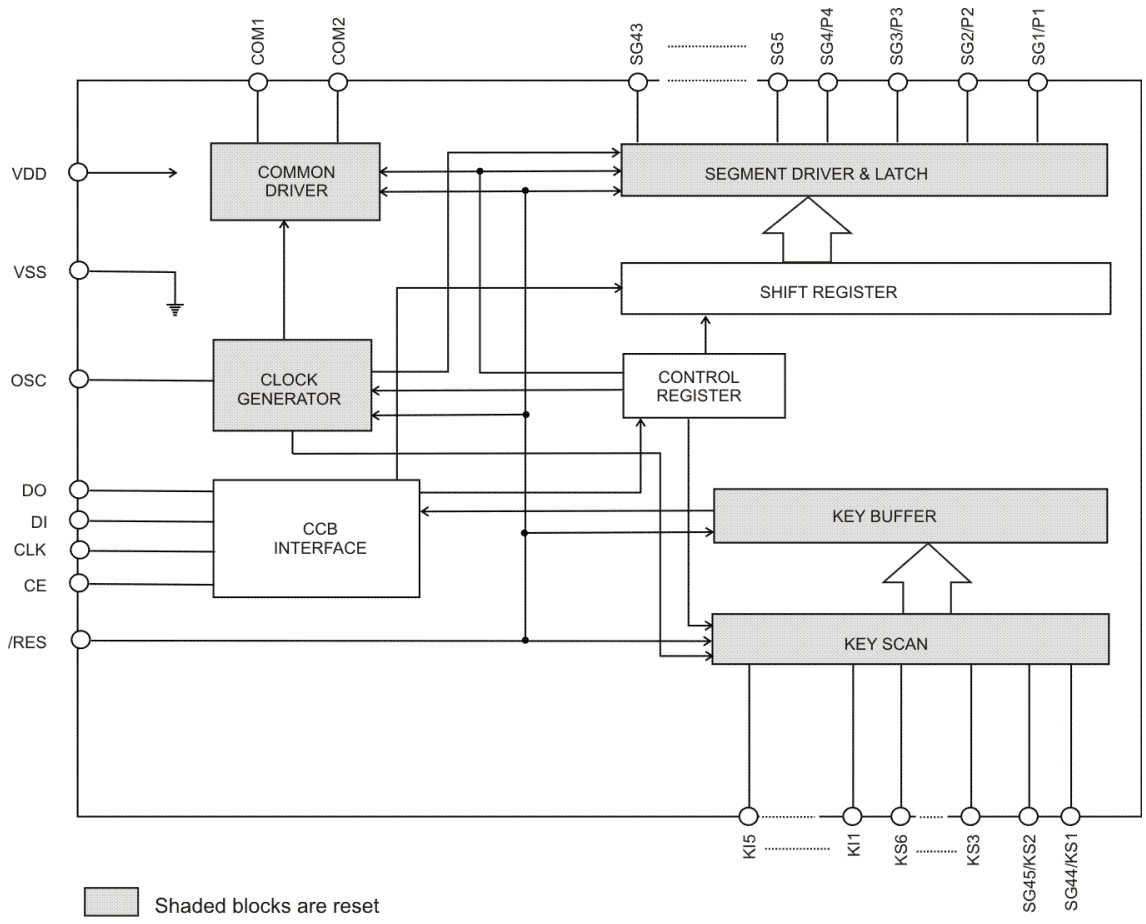
CLOCK GENERATOR
Reset is applied and the basic clock stops. However, the state of the OSC pin (the normal or sleep state) is determined after the control data S0 and S1 has been sent.

COMMON DRIVER, SEGMENT DRIVER & LATCH
Reset is applied and the display is turned off. However, display data can be input to the LATCH.

KEY SCAN
Reset is applied and at the same time as the internal states are set to their initial states, the key scan operation is disabled.

KEY BUFFER
Reset is applied and all the key data is set to the low level.

CCB INTERFACE, CONTROL REGISTER, SHIFT REGISTER
To allow serial data transfers, reset is not applied to these circuits.



OUTPUT PIN STATES DURING THE RESET PERIOD (WHEN /RES IS LOW)

Output Pin	State During Reset
SG1/P1 to SG4/P4	L *1
SG5 to SG43	L
COM1, COM2	L
KS1/SG44, KS2/SG45	L *1
KS3 to KS5	X *2
KS6	H
DO	H *3

X: don't care

Notes:
*1: These output pins are forcibly set to the segment output mode and held low.
*2: Immediately following power on, these output pins are undefined until the control data S0 and S1 has been sent.
*3: Since this output pin is an open-drain output, a pull-up resistor of between 1k and 10KΩ is required. This pin is held high during the reset period even if key data is read.

NOTE ON CONTROLLER DISPLAY DATA TRANSFER

The PT6552 transfers the display data (D1 to D90) in two operations. To assure visual display quality, all the display data should be sent within a 30ms or shorter period.

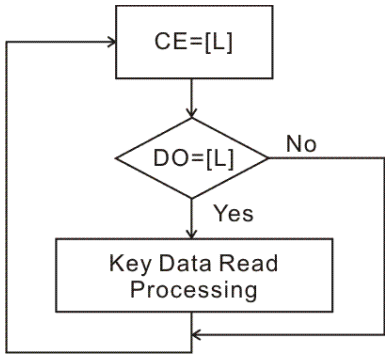
NOTE ON CONTROLLER KEY DATA READ TECHNIQUES

When determining key on/off and reading key data, the controller must confirm the state of D0 output when CE is low for each period t7. When DO is low, the controller recognizes that a key has been pressed and reads the key data. During this operation t7 must obey the following condition:

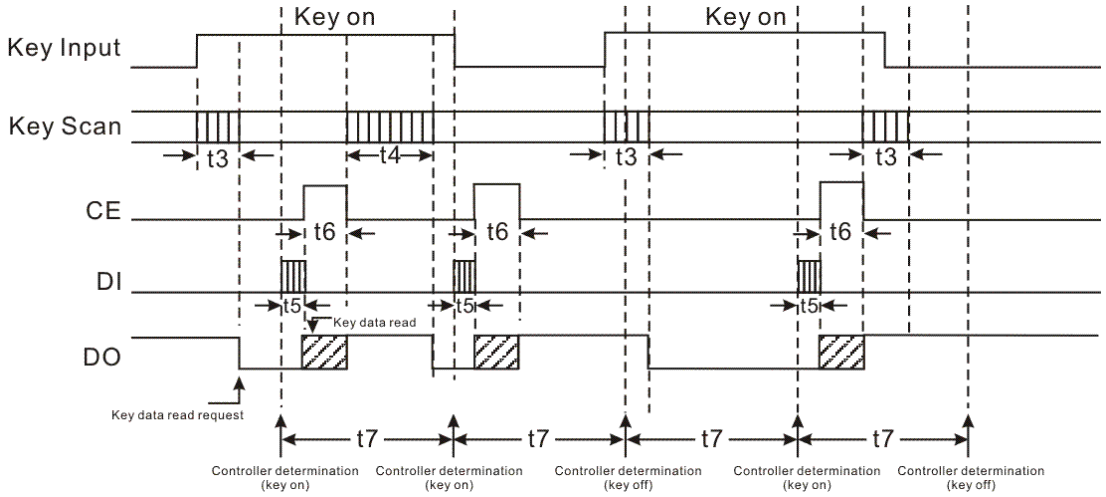
t7 > t5 + t6 + t4 If key data is read when DO is high, the key data (KD1 to KD30) and the sleep acknowledge data (SA) will be invalid.

1. CONTROLLER KEY DATA READING UNDER TIMER CONTROL

FLOWCHART



TIMING CHART

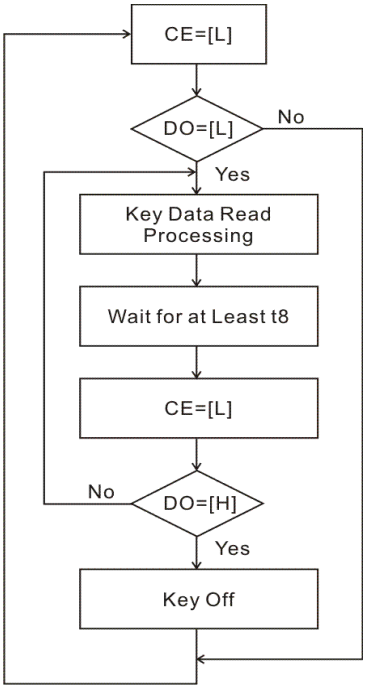


T=1/fosc
t3: Key scan execution time (800T [s]) when the key scan data for two key scans agrees.
t4: Key scan execution time (1600T [s]) when the key scan data for two key scans does not agree and a key scan is executed again.
t5: Key address (43H) transfer time.
t6: Key data read time.

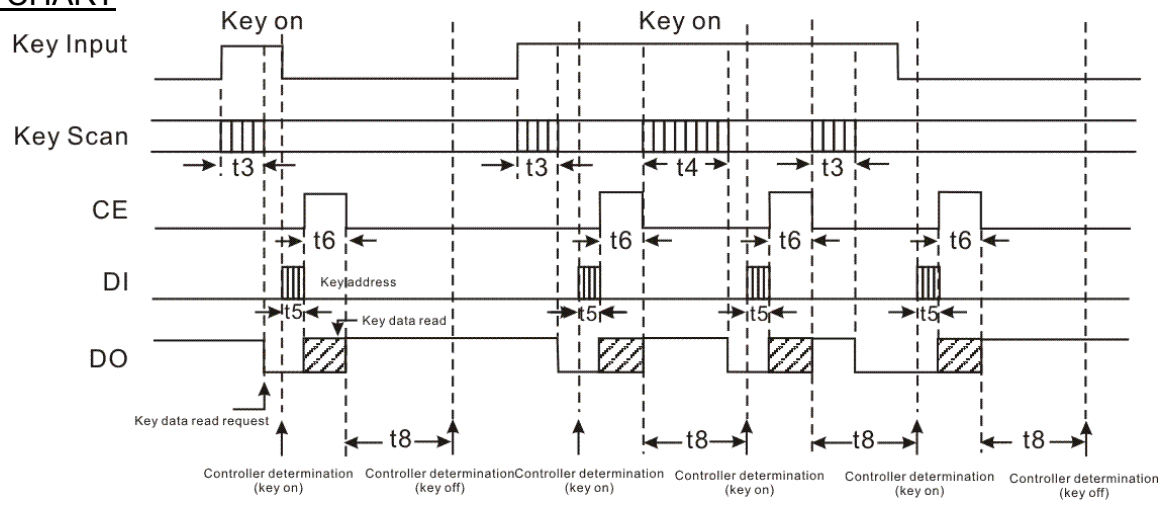
2. CONTROLLER KEY DATA READING UNDER INTERRUPT CONTROL

When determining key on/of and reading key data, the controller must confirm the state of DO output when CE is low. When DO is low, the controller recognizes that a key has been pressed and reads the key data. After the time t8, the next key on/off determination and reading key data must be confirmed by the state of DO output when CE is low. During this operation t8 must obey the following condition:
t8 > t4.
If key data is read when DO is high, the key data (KD1 to KD30) and the sleep acknowledge data (SA) be invalid.

FLOWCHART



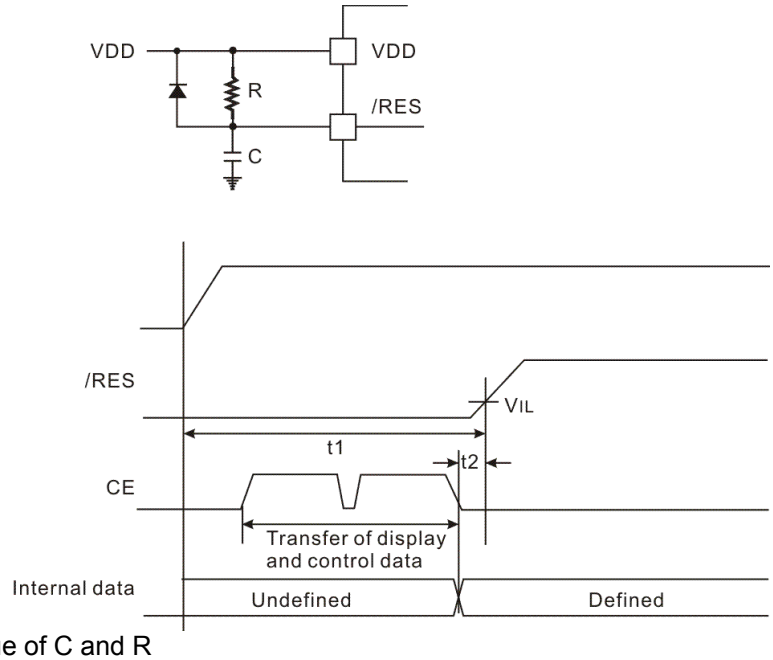
TIMING CHART



T=1/fosc
t3: Key scan execution time (800T [s]) when the key scan data for two key scans agrees.
t4: Key scan execution time (1600T [s]) when the key scan data for two key scans does not agree and a key scan is executed again.
t5: Key address (43H) transfer time.
t6: Key data read time.

/RES AND THE DISPLAY CONTROLLER

Since the LSI internal data (D1 to D90 and the control data) is undefined when power is first applied, the output pins SG1/P1 to SG4/P4, SG5 to SG43, COM1, COM2, KS1/SG44 and KS2/SG45 should be held low by setting the /RES pin low at the same time as power is applied. Then, meaningless displays at power on can be prevented by transferring data from the controller and setting /RES high when that transfer has completes.



t1: Determined by the value of C and R
t2: 10μs min

Figure 1

ABSOLUTE MAXIMUM RATINGS

(VSS=0V, Ta=25℃)

Parameter	Symbol	Condition	Rating	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	-0.3 ~ +7.0	V
Input voltage	V_{IN}	OSC, CE, CLK, DI, /RES, KI1 to KI5	-0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT}	OSC, DO, SG1 to SG45, COM1, COM2, KS1 to KS6, P1 to P4	-0.3 to V_{DD}+0.3	V
Output current	I_{OUT1}	SG1 to SG45	100	μA
	I_{OUT2}	COM1, COM2, KS1 to KS6	1	mA
	I_{OUT3}	P1 to P4	5	mA
Allowable power dissipation	Pd max	Ta=85℃	200	mW
Operating temperature	Topr		-40 to +85	℃
Storage temperature	Tstg		-65 to +150	℃

ALLOWABLE OPERATING RANGES

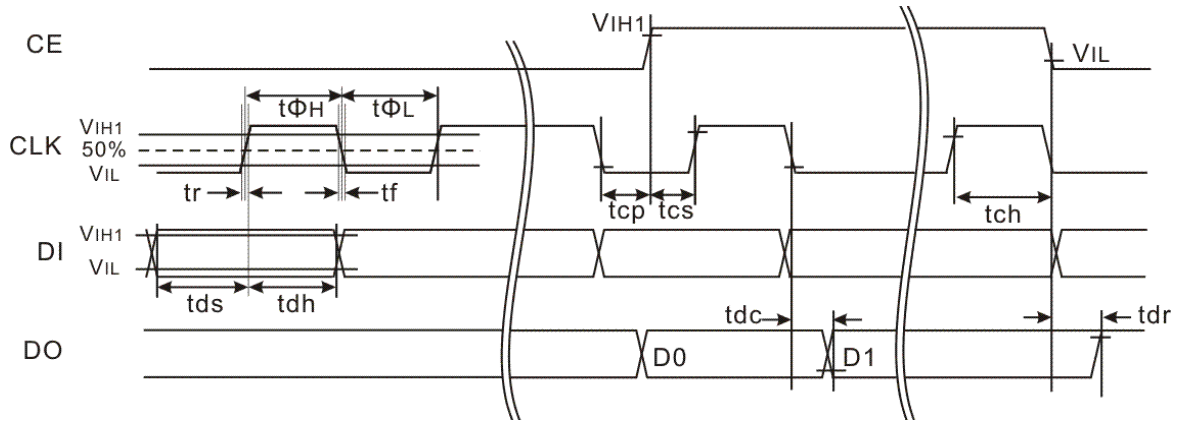
(Ta=-40 to +85℃, VSS=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	V_{DD}	4.5		6.0	V
Input high-level voltage	V_{IH1}	CE, CLK, DI, /RES	0.8V_{DD}		V_{DD}	V
	V_{IH2}	KI1 to KI5	0.6V_{DD}		V_{DD}	V
Input low-level voltage	V_{IL}	CE, CLK, DI, /RES, KI1 to KI5	0		0.2V_{DD}	V
Recommended external resistance	R_{OSC}	OSC		62		KΩ
Recommended external capacitance	C_{OSC}	OSC		680		pF
Guaranteed oscillator range	fosc	OSC	25	50	100	KHz
Data setup time	t_{ds}	CLK, DI: Figure 2	160			ns
Data hold time	t_{dh}	CLK, DI: Figure 2	160			ns
CE wait time	tcp	CE, CLK: Figure 2	160			ns
CE setup time	tcs	CE, CLK: Figure 2	160			ns
CE hold time	tch	CE, CLK: Figure 2	160			ns
High-level clock pulse width	$t_{\varnothing H}$	CLK: Figure 2	160			ns
Low-level clock pulse width	$t_{\varnothing L}$	CLK: Figure 2	160			ns
Rise time	t_r	CE, CLK, DI: Figure 2		160		ns
Fall time	t_f	CE, CLK, DI: Figure 2		160		ns
DO output delay time	t_{dc}	DO, R_{PU}=47KΩ, C_L=10pF*: Figure 2			1.5	μs
DO rise time	t_{dr}	DO, R_{PU}=47KΩ, C_L=10pF*: Figure 2			1.5	μs
/RES switching time	t_2	Figure 1	10			μs

ELECTRICAL CHARACTERISTICS IN THE ALLOWABLE OPERATING RANGES

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Hysteresis	V_H	CE, CLK, CI, /RES, KI1 to KI5		$0.1V_{DD}$		V
Input high-level current	I_{IH}	CE, CLK, DI, /RES: $V_I=V_{DD}$			5.0	μA
Input low-level current	I_{IL}	CE, CLK, DI, /RES: V_I=0V	-5.0			μA
Input floating voltage	V_{IF}	KI1 to KI5			$0.05V_{DD}$	V
Pull-down resistance	R_{PD}	KI1 to KI5:V_{DD}=5.0V	50	100	250	KΩ
Output off leakage current	I_{OFFH}	DO:V_O=6.0V			6.0	μA
Output high-level voltage	V_{OH1}	KS1 to KS6:I_O=-1mA	V_{DD}-1.0			V
	V_{OH2}	P1 to P4:I_O=-1mA	V_{DD}-1.0			V
	V_{OH3}	SG1 to SG45: I_O=-10μA	V_{DD}-1.0			V
	V_{OH4}	COM1, COM2: I_O=-100μA	V_{DD}-0.6			V
Output low-level voltage	V_{OL1}	KS1 to KS6:I_O=50μA	0.4	1.0	3.0	V
	V_{OL2}	P1 to P4:I_O=1mA			1.0	V
	V_{OL3}	SG1 to SG45:I_O=10μA			1.0	V
	V_{OL4}	COM1, COM2: I_O=-100μA			0.6	V
	V_{OL5}	DO:I_O=1mA		0.1	0.5	V
Output middle-level voltage	V_{MID1}	COM1, COM2: V_{DD}=6.0V, I_O=±100μA	2.4	3.0	3.6	V
	V_{MID2}	COM1, COM2: V_{DD}=4.5V, I_O=±100μA	1.65	2.25	2.85	V
Current drain	I_{DD1}	Sleep Mode, Ta=25℃			5	μA
	I_{DD2}	V_{DD}=6.0V, Output open, Ta=25℃, fosc=50KHz		1.4	2.5	mA

WHEN STOPPED WITH CL AT THE LOW LEVEL



WHEN STOPPED WITH CL AT THE HIGH LEVEL

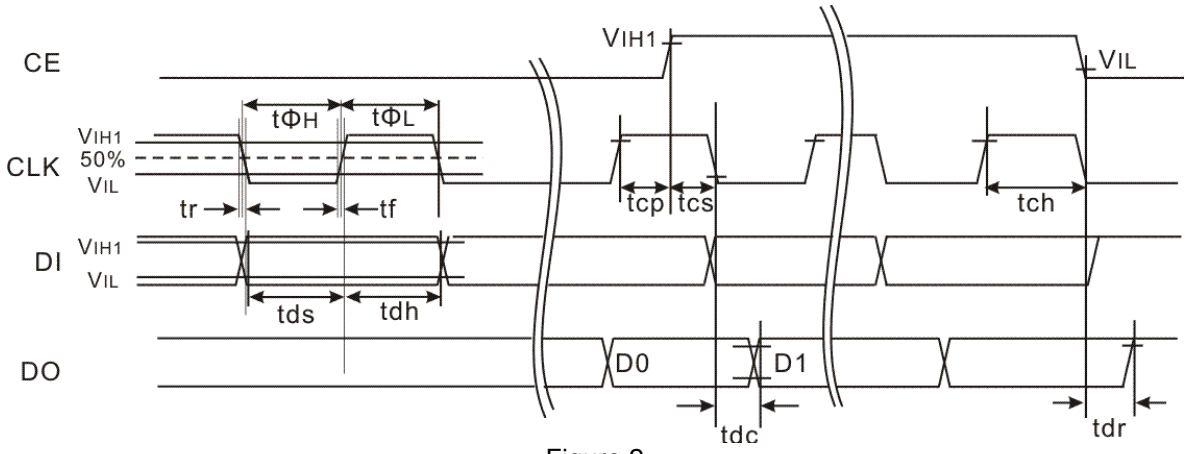
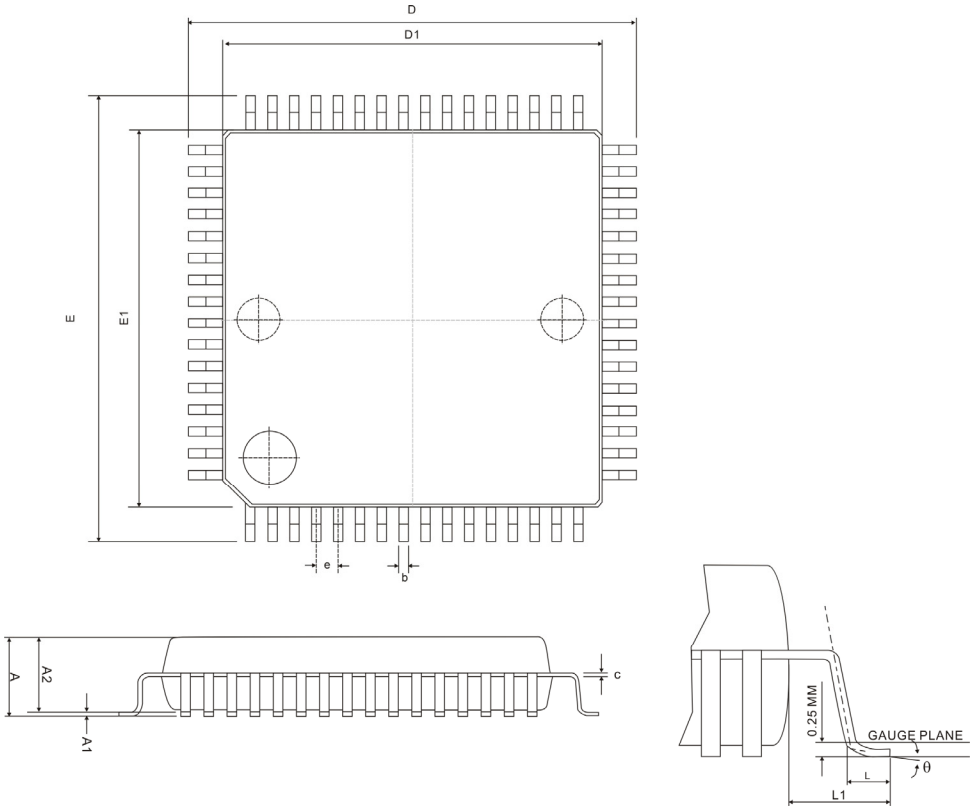


Figure 2

PACKAGE INFORMATION

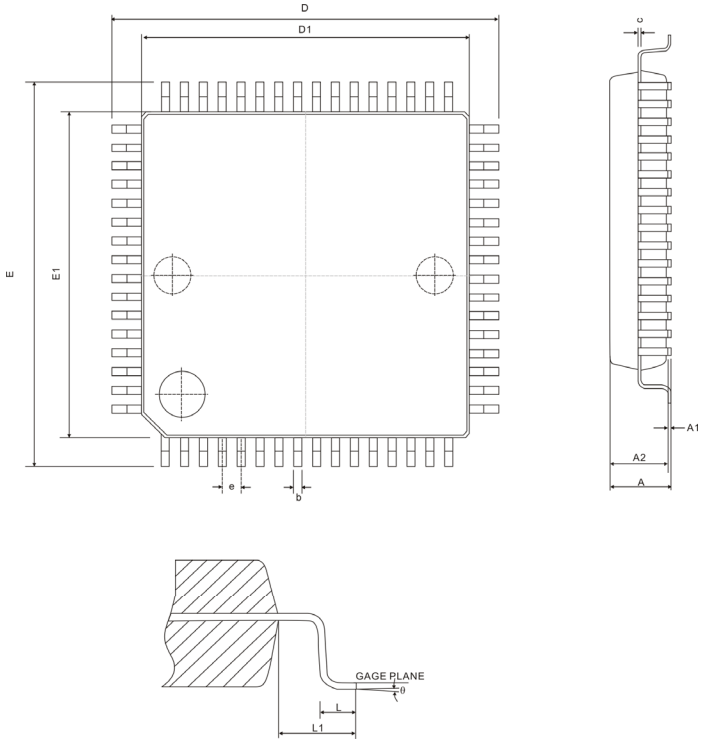
64 PINS, QFP



Symbol	Min.	Nom.	Max.
A	-	-	3.15
A1	0.00	-	0.25
A2	1.90	-	2.90
b	0.29	0.35	0.41
c	0.11	-	0.23
D		17.20 BSC	
D1		14.00 BSC	
E		17.20 BSC	
E1		14.00 BSC	
e		0.80 BSC	
L	0.65	-	1.05
L1		1.60 REF	
θ	0°	-	8°

Notes:
1. Refer to JEDEC MC-022BE
2. Unit: mm

64 PINS, LQFP



Symbol	Min.	Nom.	Max.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	-	0.20
D	12.00 BSC		
D1	10.00 BSC		
E	12.00 BSC		
E1	10.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

Notes:
1. All dimensions are in millimeter.
2. Refer to JEDEC MS-026BCD

IMPORTANT NOTICE

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