



**RoHS\***  
COMPLIANT

PRODUCT SUMMARY		
V <sub>DS</sub> (V)	r <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A) <sup>b</sup>
30	0.0065 at V <sub>GS</sub> = 10 V	84 <sup>b</sup>
	0.0095 at V <sub>GS</sub> = 4.5 V	59 <sup>b</sup>

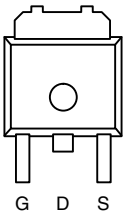
**FEATURES**

- TrenchFET® Power MOSFET
- 175 °C Junction Temperature
- Optimized for Low-Side Synchronous Rectifier Operation
- 100 % R<sub>g</sub> Tested

**APPLICATIONS**

- DC/DC Converters
- Synchronous Rectifiers

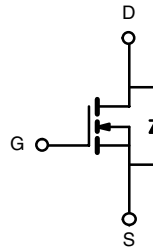
TO-252



Top View

Drain Connected to Tab

Ordering Information:  
SUD50N03-06P  
SUD50N03-06P-E3 (Lead (Pb)-free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V <sub>DS</sub>	30	V
Gate-Source Voltage		V <sub>GS</sub>	±20	
Continuous Drain Current <sup>a</sup>	T <sub>C</sub> = 25 °C	I <sub>D</sub>	84 <sup>b</sup>	A
	T <sub>C</sub> = 100 °C		59 <sup>b</sup>	
Pulsed Drain Current		I <sub>DM</sub>	100	
Continuous Source Current (Diode Conduction) <sup>a</sup>		I <sub>S</sub>	25	
Single Pulse Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	45	mJ
Avalanche Energy		E <sub>AS</sub>	101.25	
Maximum Power Dissipation	T <sub>C</sub> = 25 °C	P <sub>D</sub>	88	W
	T <sub>A</sub> = 25 °C		8.3 <sup>a</sup>	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	-55 to 175	°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>a</sup>	t ≤ 10 sec	R <sub>thJA</sub>	15	18	°C/W
	Steady State		40	50	
Maximum Junction-to-Case		R <sub>thJC</sub>	1.4	1.7	

Notes

- a. Surface Mounted on FR4 Board, t ≤ 10 sec.  
b. Based on maximum allowable Junction Temperature, package limitation current is 50 A.

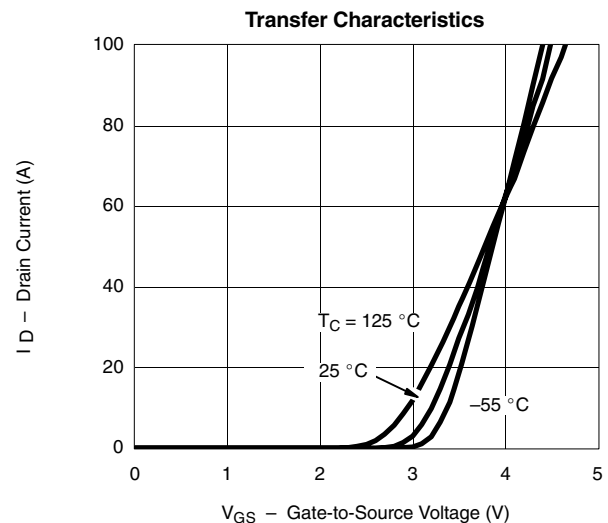
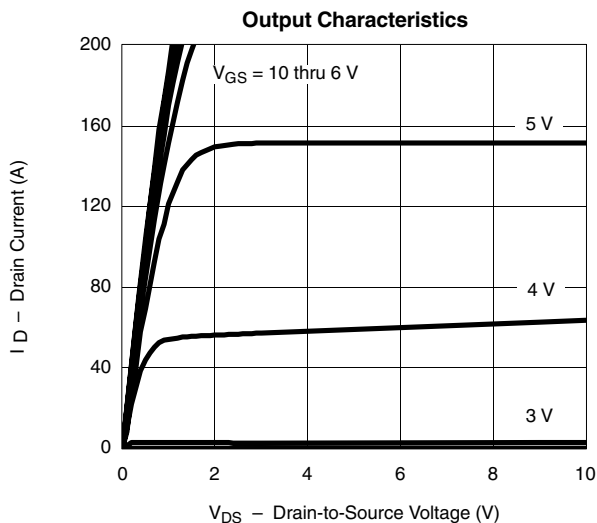
\* Pb containing terminations are not RoHS compliant, exemptions may apply

SPECIFICATIONS (T <sub>J</sub> = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ <sup>a</sup>	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	30			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.0		3.0	
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C			50	
On-State Drain Current <sup>b</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = 5 V, V <sub>GS</sub> = 10 V	50			A
Drain-Source On-State Resistance <sup>b</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A		0.0053	0.0065	Ω
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A, T <sub>J</sub> = 125 °C			0.0105	
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 20 A		0.0078	0.0095	
Forward Transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 20 A	20			S
<b>Dynamic<sup>a</sup></b>						
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1 MHz		3100		pF
Output Capacitance	C <sub>oss</sub>			565		
Reverse Transfer Capacitance	C <sub>rss</sub>			255		
Gate Resistance	R <sub>g</sub>		1	1.9	3.1	Ω
Total Gate Charge <sup>c</sup>	Q <sub>g</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 50 A		21	30	nC
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>			10		
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			7.5		
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = 15 V, R <sub>L</sub> = 0.3 Ω I <sub>D</sub> ≅ 50 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 2.5 Ω		12	20	ns
Rise Time <sup>c</sup>	t <sub>r</sub>			12	20	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			30	45	
Fall Time <sup>c</sup>	t <sub>f</sub>			10	15	
<b>Source-Drain Diode Ratings and Characteristic (T<sub>C</sub> = 25 °C)</b>						
Pulsed Current	I <sub>SM</sub>				100	A
Diode Forward Voltage <sup>b</sup>	V <sub>SD</sub>	I <sub>F</sub> = 100 A, V <sub>GS</sub> = 0 V		1.2	1.5	V
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 50 A, di/dt = 100 A/μs		35	70	ns

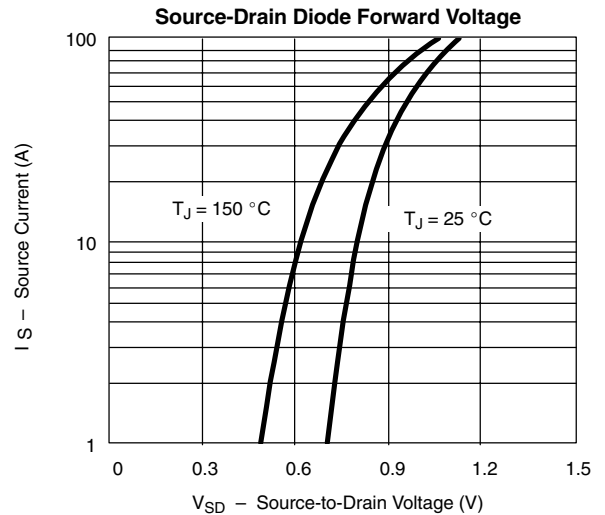
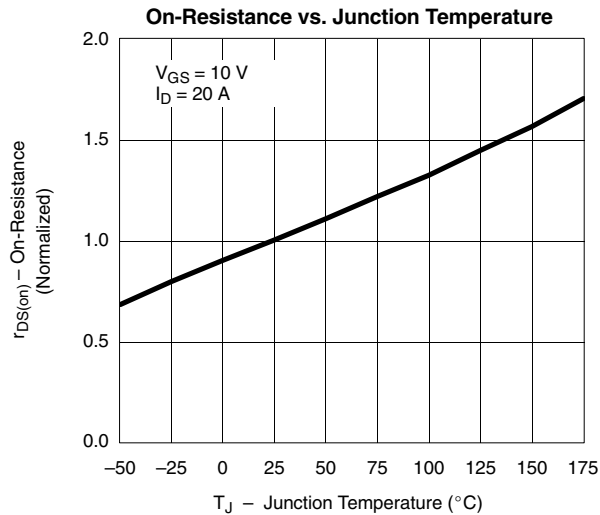
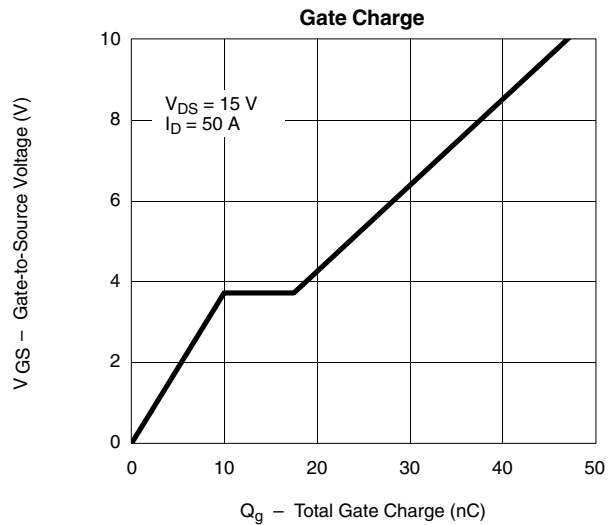
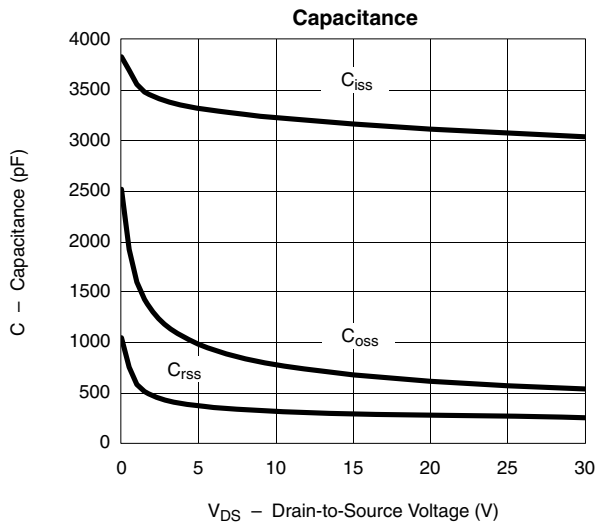
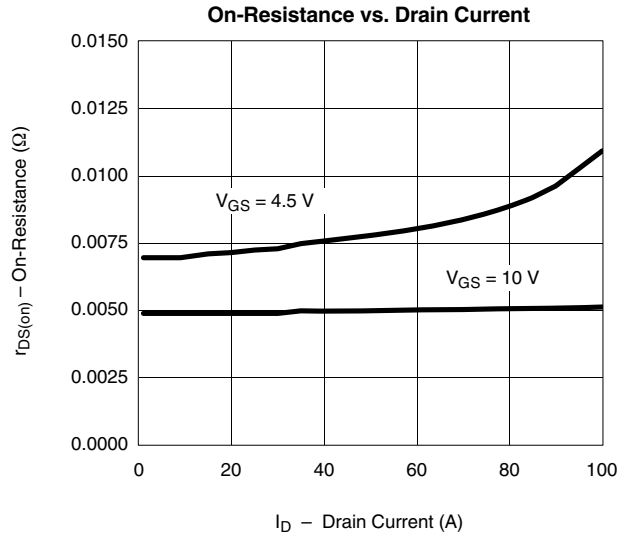
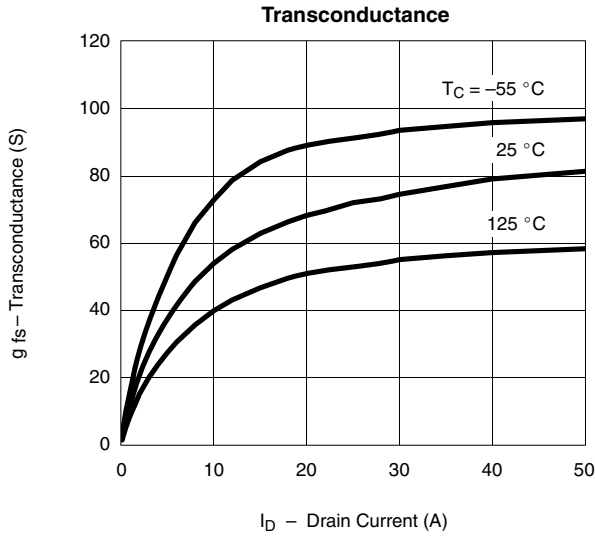
Notes

- Guaranteed by design, not subject to production testing.
- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- Independent of operating temperature.

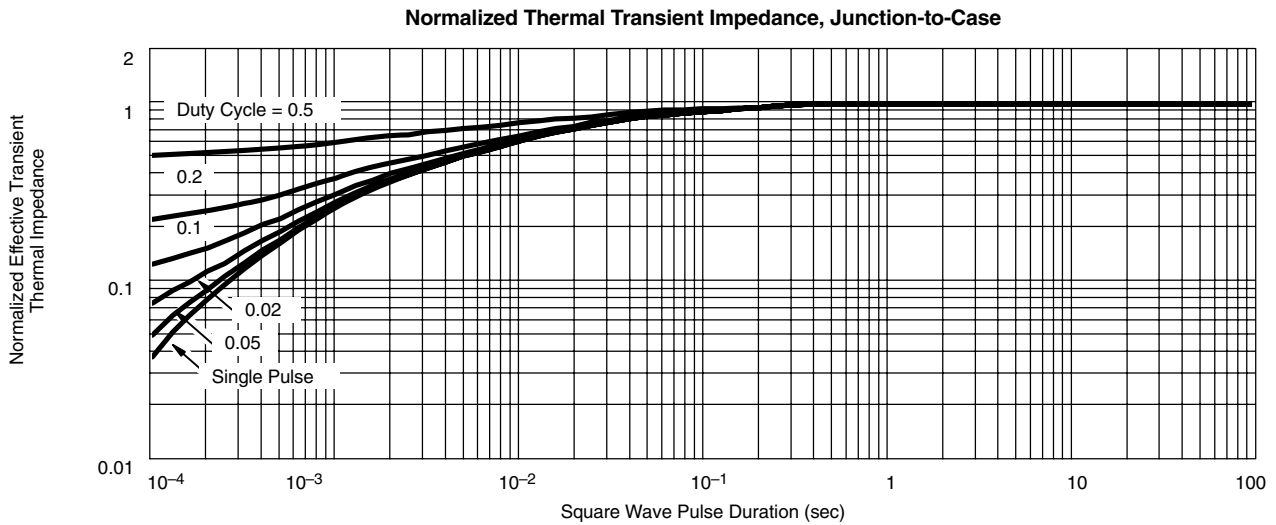
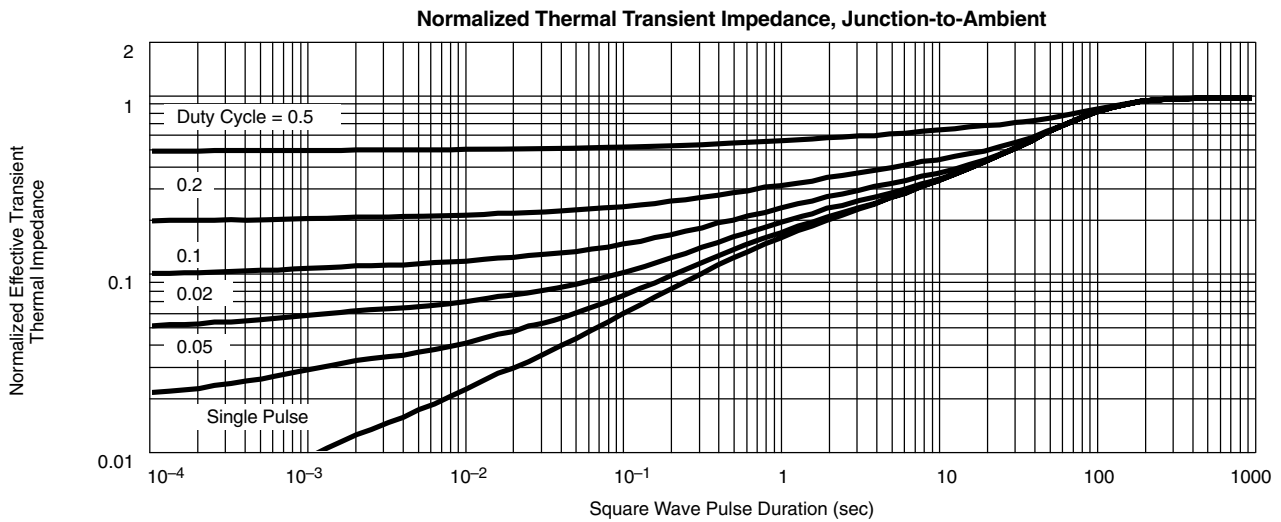
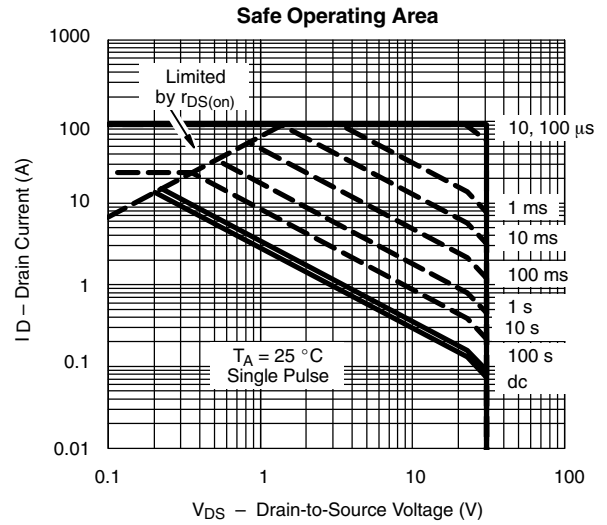
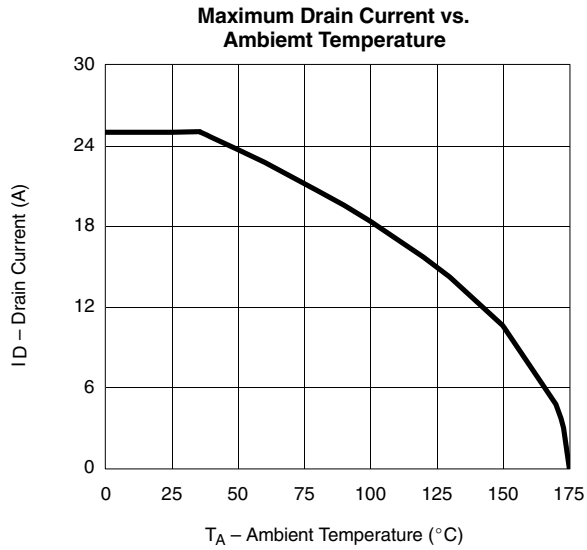
**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)**



**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)**



**THERMAL RATINGS**



## Disclaimer

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