3.3V CMOS 36-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS AND BUS-HOLD

IDT74ALVCH32501

FEATURES:

- **0.5 MICRON CMOS Technology**
- **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
- **ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)**
- **Vcc = 3.3V ± 0.3V, Normal Range**
- **Vcc = 2.7V to 3.6V, Extended Range**
- **Vcc = 2.5V ± 0.2V**
- **CMOS power levels (0.4µ W typ. static)**
- **Rail-to-Rail output swing for increased noise margin**
- **Available in 114-ball LFBGA package**

DRIVE FEATURES:

- **High Output Drivers: ±24mA**
- **Suitable for Heavy Loads**

APPLICATIONS:

- **3.3V high speed systems**
- **3.3V and lower voltage computing systems**

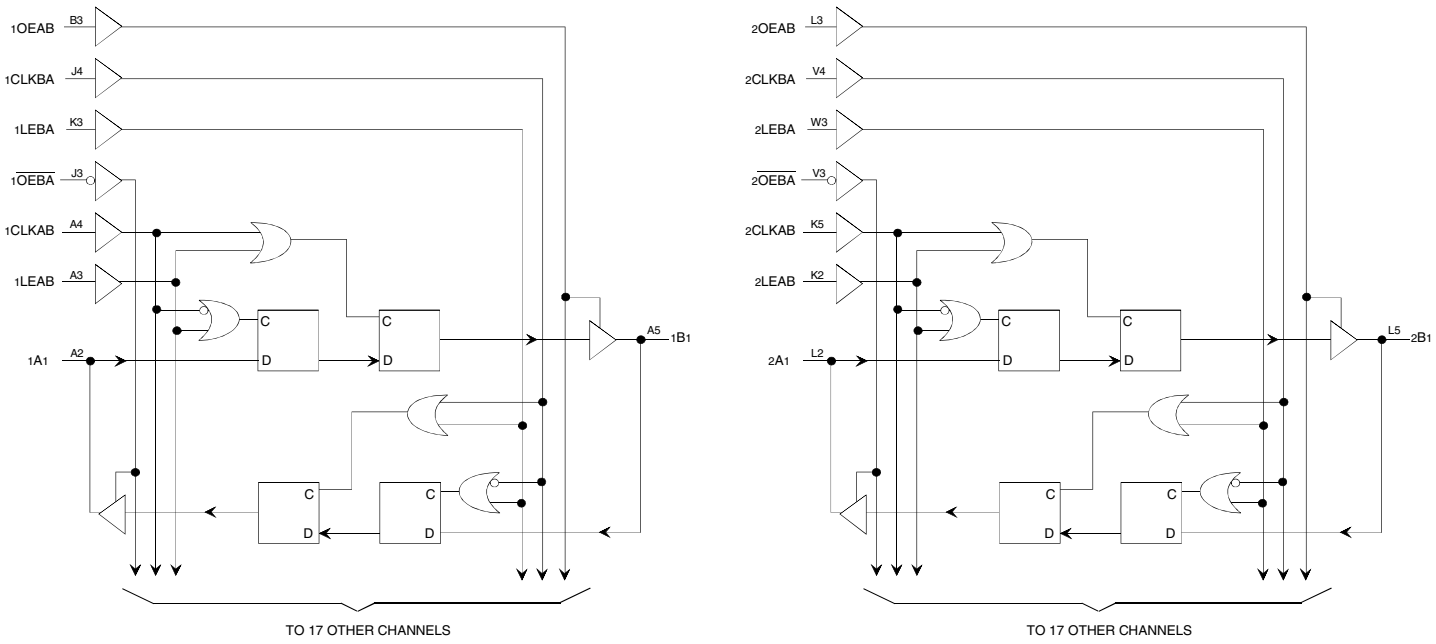
DESCRIPTION:

This 36-bit universal bus transceiver is built using advanced dual metal CMOS technology. The ALVCH32501 combines D-type latches and Dtype flip-flops to allow data flow in transparent latched and clocked modes. Data flow in each direction is controlled by output-enable (OEAB and $\overline{OEBA}$), latch enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a HIGH or low logic level. If LEAB is low, the A bus data is stored in the latch/ flip-flop on the low-to-high transition of CLKAB. OEAB performs the output enable function on the B port. Data flow from B port to A port is similar but requires using $\overline{OEBA}$, LEBA and CLKBA. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

This ALVCH32501 has been designed with a ±24mA output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The ALVCH32501 has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

FUNCTIONAL BLOCK DIAGRAM

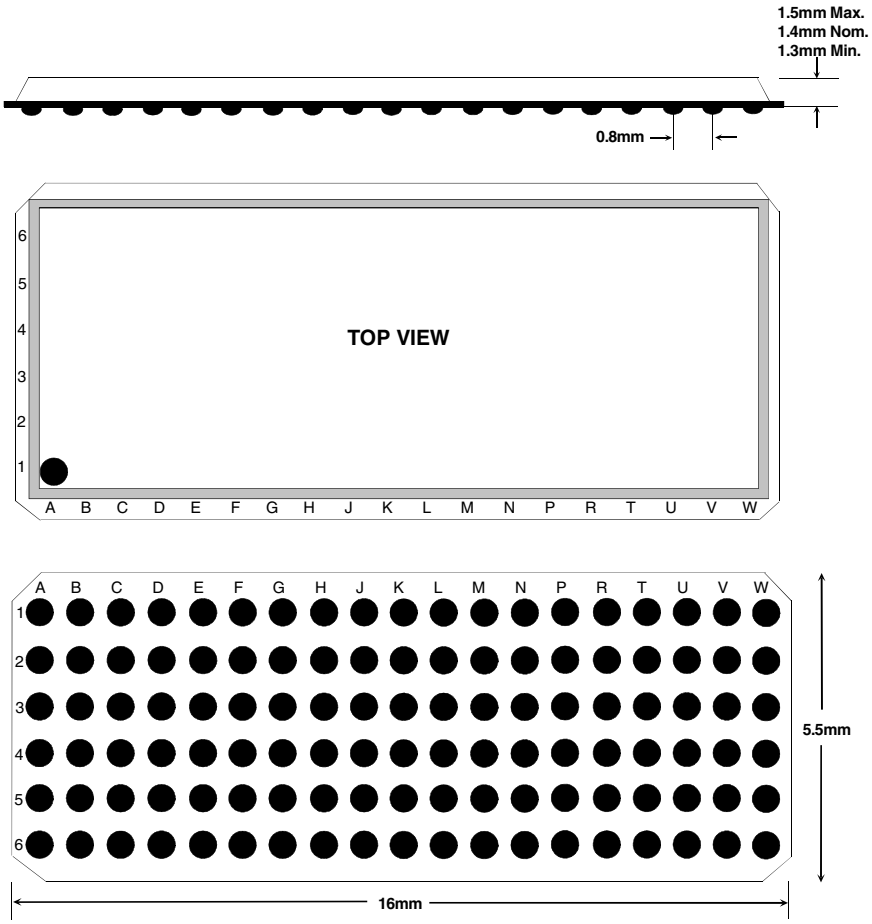


PIN CONFIGURATION

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W
6	1B2	1B4	1B6	1B8	1B10	1B12	1B14	1B15	1B17	NC	2B2	2B4	2B6	2B8	2B10	2B12	2B14	2B15	2B17
5	1B1	1B3	1B5	1B7	1B9	1B11	1B13	1B16	1B18	2CLKAB	2B1	2B3	2B5	2B7	2B9	2B11	2B13	2B16	2B18
4	1CLKAB	GND	GND	VCC	GND	GND	VCC	GND	1CLKBA	GND	GND	GND	VCC	GND	GND	VCC	GND	2CLKBA	GND
3	1LEAB	1OEAB	GND	VCC	GND	GND	VCC	GND	$1\overline{OEBA}$	1LEBA	2OEAB	GND	VCC	GND	GND	VCC	GND	$2\overline{OEBA}$	2LEBA
2	1A1	1A3	1A5	1A7	1A9	1A11	1A13	1A16	1A18	2LEAB	2A1	2A3	2A5	2A7	2A9	2A11	2A13	2A16	2A18
1	1A2	1A4	1A6	1A8	1A10	1A12	1A14	1A15	1A17	NC	2A2	2A4	2A6	2A8	2A10	2A12	2A14	2A15	2A17

LFBGA
TOPVIEW

114 BALL LFBGA PACKAGE ATTRIBUTES



ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +4.6	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}+0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current	–50 to +50	mA
I_{IK}	Continuous Clamp Current, V_I < 0 or V_I > V_{CC}	±50	mA
I_{OK}	Continuous Clamp Current, V_O < 0	–50	mA
I_{CC} I_{SS}	Continuous Current through each V_{CC} or GND	±100	mA

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC} terminals.
3. All terminals except V_{CC}.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	9	pF
$C_{I/O}$	I/O Port Capacitance	V_{IN} = 0V	7	9	pF

NOTE:
1. As applicable to the device type.

PIN DESCRIPTION

Pin Names	Description
OEAB	A-to-B Output Enable Input
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
xAx	A-to-B Data Inputs or B-to-A 3-State Outputs(1)
xBx	B-to-A Data Inputs or A-to-B 3-State Outputs(1)

NOTE:
1. These pins have "Bus-Hold". All other pins are standard inputs, outputs, or I/Os.

FUNCTION TABLE (EACH FLIP-FLOP)(1,2)

Inputs				Outputs
OEAB	LEAB	CLKAB	xAx	xBx
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	L	X	B(3)
H	L	H	X	B(4)

NOTES:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance
   ↑ = LOW-to-HIGH Transition
2. A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, and CLKBA.
3. Output level before the indicated steady-state conditions were established.
4. Output level before the indicated steady-state conditions were established, provided that CLKAB was HIGH before LEAB went LOW.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = –40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ.(1)	Max.	Unit
V_{IH}	Input HIGH Voltage Level	V_{CC} = 2.3V to 2.7V		1.7	—	—	V
		V_{CC} = 2.7V to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	V_{CC} = 2.3V to 2.7V		—	—	0.7	V
		V_{CC} = 2.7V to 3.6V		—	—	0.8	
I_{IH}	Input HIGH Current	V_{CC} = 3.6V	V_I = V_{CC}	—	—	±5	µA
I_{IL}	Input LOW Current	V_{CC} = 3.6V	V_I = GND	—	—	±5	µA
I_{OZH}	High Impedance Output Current	V_{CC} = 3.6V	V_O = V_{CC}	—	—	±10	µA
I_{OZL}	(3-State Output pins)		V_O = GND	—	—	±10	
V_{IK}	Clamp Diode Voltage	V_{CC} = 2.3V, I_{IN} = –18mA		—	–0.7	–1.2	V
V_H	Input Hysteresis	V_{CC} = 3.3V		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = 3.6V V_{IN} = GND or V_{CC}		—	0.1	40	µA
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at V_{CC} - 0.6V, other inputs at V_{CC} or GND		—	—	750	µA

NOTE:
1. Typical values are at V_{CC} = 3.3V, +25°C ambient.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter(1)	Test Conditions		Min.	Typ.(2)	Max.	Unit
I_{BHH}	Bus-Hold Input Sustain Current	V_{CC} = 3V	V_I = 2V	–75	—	—	µA
I_{BHL}			V_I = 0.8V	75	—	—	
I_{BHH}	Bus-Hold Input Sustain Current	V_{CC} = 2.3V	V_I = 1.7V	–45	—	—	µA
I_{BHL}			V_I = 0.7V	45	—	—	
I_{BHHO}	Bus-Hold Input Overdrive Current	V_{CC} = 3.6V	V_I = 0 to 3.6V	—	—	±500	µA
I_{BHLO}							

NOTES:
1. Pins with Bus-Hold are identified in the pin description.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 2.3V to 3.6V	I_{OH} = – 0.1mA	V_{CC} – 0.2	—	V
		V_{CC} = 2.3V	I_{OH} = – 6mA	2	—	
		V_{CC} = 2.3V	I_{OH} = – 12mA	1.7	—	
		V_{CC} = 2.7V		2.2	—	
		V_{CC} = 3V		2.4	—	
		V_{CC} = 3V	I_{OH} = – 24mA	2	—	
V_{OL}	Output LOW Voltage	V_{CC} = 2.3V to 3.6V	I_{OL} = 0.1mA	—	0.2	V
		V_{CC} = 2.3V	I_{OL} = 6mA	—	0.4	
			I_{OL} = 12mA	—	0.7	
		V_{CC} = 2.7V	I_{OL} = 12mA	—	0.4	
		V_{CC} = 3V	I_{OL} = 24mA	—	0.55	

NOTE:
1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = – 40°C to + 85°C.

OPERATING CHARACTERISTICS, T_A = 25°C

Symbol	Parameter	Test Conditions	V_{CC} = 2.5V ± 0.2V	V_{CC} = 3.3V ± 0.3V	Unit
			Typical	Typical	
C_{PD}	Power Dissipation Capacitance Outputs enabled	C_L = 0pF, f = 10Mhz	88	108	pF
C_{PD}	Power Dissipation Capacitance Outputs disabled		12	12	

SWITCHING CHARACTERISTICS(1)

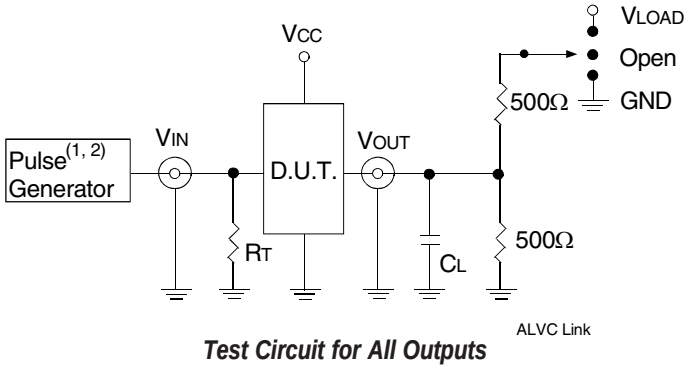
Symbol	Parameter		V_{CC} = 2.5V ± 0.2V		V_{CC} = 2.7V		V_{CC} = 3.3V ± 0.3V		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay xCLK to xQx		1	5.3	—	4.9	1	4.2	ns
t_{PLH} t_{PHL}	Propagation Delay xAx to xBx or xBx to xAx		1	4.8	—	4.5	1	3.9	ns
t_{PLH} t_{PHL}	Propagation Delay LE to xAx or xBx		1.1	5.7	—	5.3	1.3	4.6	ns
t_{PLH} t_{PHL}	Propagation Delay CLK to Ax or Bx		1.2	6.1	—	5.6	1.4	4.9	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ to xAx		1.3	6.3	—	6	1.1	5	ns
t_{PZH} t_{PZL}	Output Enable Time OEAB to xBx		1	5.8	—	5.3	1	4.6	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}$ to xAx		1.3	5.3	—	4.6	1.3	4.2	ns
t_{PHZ} t_{PLZ}	Output Disable Time OEAB to xBx		1.5	6.2	—	5.7	1.4	5	ns
t_{SU}	Set-up Time, data before CLK↑		2.2	—	2.1	—	1.7	—	ns
t_H	Hold Time, data after CLK↑		0.6	—	0.6	—	0.7	—	ns
t_{SU}	Set-up Time, data before LE↓	CLK HIGH	1.9	—	1.6	—	1.5	—	ns
		CLK LOW	1.3	—	1.1	—	1	—	
t_H	Hold Time, data after LE↓, CLK HIGH or LOW		1.4	—	1.7	—	1.4	—	ns
t_W	Pulse Width, LE HIGH		3.3	—	3.3	—	3.3	—	ns
t_W	Pulse Width, CLK HIGH or LOW		3.3	—	3.3	—	3.3	—	ns
$t_{SK(o)}$	Output Skew(2)		—	—	—	—	—	500	ps

NOTES:
1. See TEST CIRCUITS AND WAVEFORMS. T_A = – 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	$V_{CC}^{(1)}$=3.3V±0.3V	$V_{CC}^{(1)}$=2.7V	$V_{CC}^{(2)}$=2.5V±0.2V	Unit
V_{LOAD}	6	6	2 x Vcc	V
V_{IH}	2.7	2.7	Vcc	V
V_T	1.5	1.5	Vcc / 2	V
V_{LZ}	300	300	150	mV
V_{HZ}	300	300	150	mV
C_L	50	50	30	pF



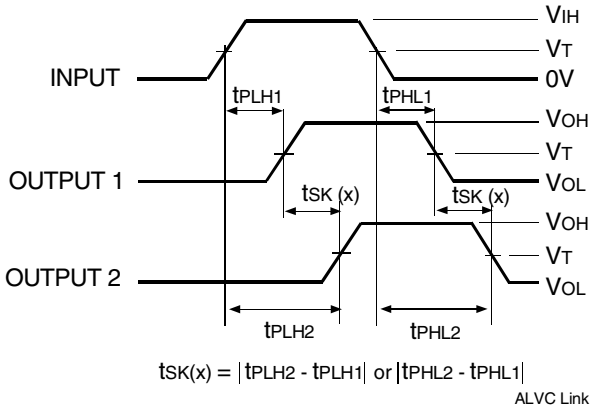
Test Circuit for All Outputs

DEFINITIONS:
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:
1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2ns; t_R ≤ 2ns.

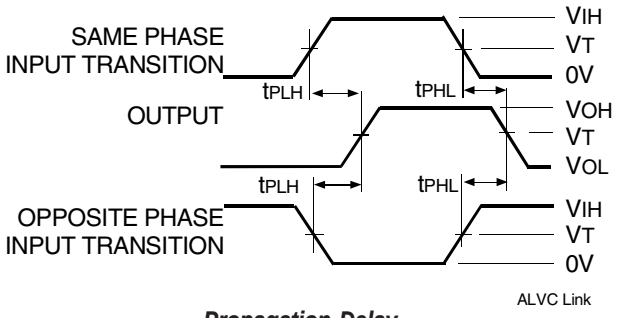
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V_{LOAD}
Disable High Enable High	GND
All Other Tests	Open

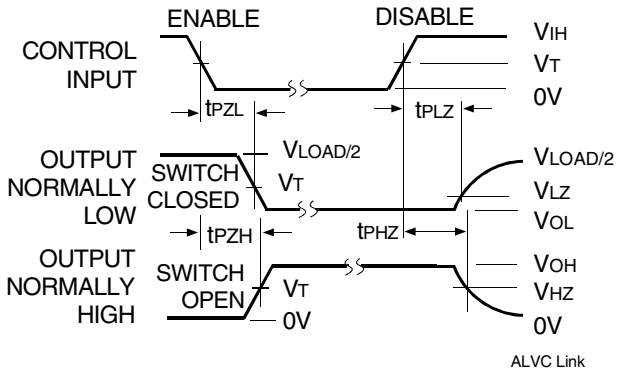


Output Skew - $t_{SK}(x)$

NOTES:
1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

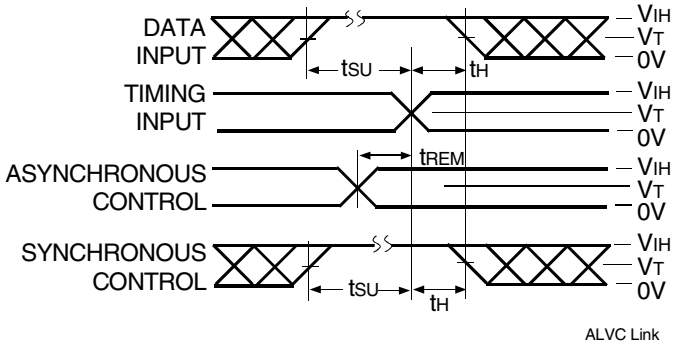


Propagation Delay

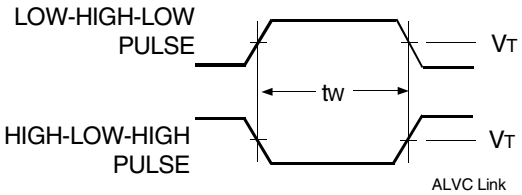


Enable and Disable Times

NOTE:
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

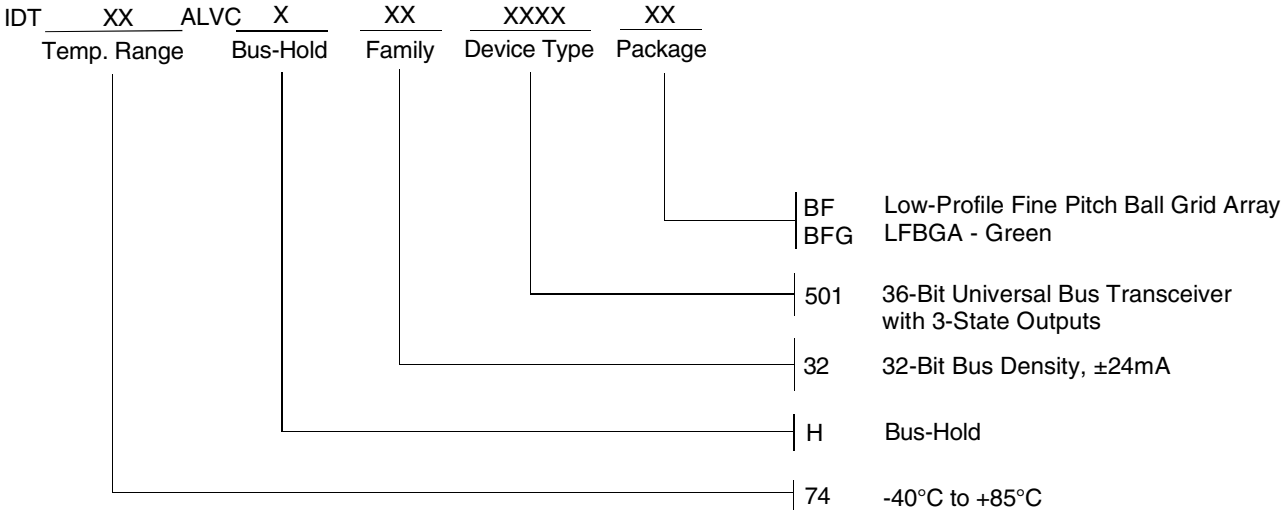


Set-up, Hold, and Release Times



Pulse Width

ORDERING INFORMATION



CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com

for Tech Support:
logichelp@idt.com
(408) 654-6459