# International IƏR Rectifier

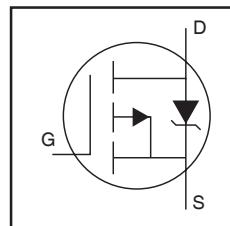**IRF4905SPbF**
**IRF4905LPbF**

HEXFET® Power MOSFET

## Features

- Advanced Process Technology
- Ultra Low On-Resistance
- 150°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Some Parameters Are Differrent from IRF4905S
- Lead-Free



$V_{DSS} = -55V$

$R_{DS(on)} = 20m\Omega$

$I_D = -42A$

## Description

Features of this design  are a 150°C junction operating temperature, fast switching speed and improved repetitive avalanche rating . These features combine to make this design an extremely efficient and reliable device for use in  a wide variety of other applications.



D²Pak
IRF4905SPbF

TO-262
IRF4905LPbF

| G | D | S |
|---|---|---|
| Gate | Drain | Source |

## Absolute Maximum Ratings

| | Parameter | Max. | Units |
|---|---|---|---|
| $I_D$ @ $T_C$ = 25°C | Continuous Drain Current, $V_{GS}$ @ 10V (Silicon Limited) | -70 | A |
| $I_D$ @ $T_C$ = 100°C | Continuous Drain Current, $V_{GS}$ @ 10V (Silicon Limited) | -44 | |
| $I_D$ @ $T_C$ = 25°C | Continuous Drain Current, $V_{GS}$ @ 10V (Package Limited) | -42 | |
| $I_{DM}$ | Pulsed Drain Current ① | -280 | |
| $P_D$ @$T_C$ = 25°C | Power Dissipation | 170 | W |
| | Linear Derating Factor | 1.3 | W/°C |
| $V_{GS}$ | Gate-to-Source Voltage | ± 20 | V |
| $E_{AS}$ (Thermally limited) | Single Pulse Avalanche Energy② | 140 | mJ |
| $E_{AS}$ (Tested ) | Single Pulse Avalanche Energy Tested Value ⑥ | 790 | |
| $I_{AR}$ | Avalanche Current ① | See Fig.12a, 12b, 15, 16 | A |
| $E_{AR}$ | Repetitive Avalanche Energy ⑤ | | mJ |
| $T_J$ | Operating Junction and | -55  to + 150 | °C |
| $T_{STG}$ | Storage Temperature Range | | |
| | Soldering Temperature, for 10 seconds | 300 (1.6mm from case ) | |
| | Mounting Torque, 6-32 or M3 screw ⑦ | 10 lbf•in (1.1N•m) | |

## Thermal Resistance

| | Parameter | Typ. | Max. | Units |
|---|---|---|---|---|
| $R_{\theta JC}$ | Junction-to-Case ⑧ | — | 0.75 | |
| $R_{\theta JA}$ | Junction-to-Ambient (PCB Mount, steady state) ⑦⑧ | — | 40 | |

8/5/05

# IRF4905S/L

## Electrical Characteristics @ $T_J$ = 25°C (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | -55 | —— | —— | V | $V_{GS}$ = 0V, $I_D$ = -250µA |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | —— | -0.054 | —— | V/°C | Reference to 25°C, $I_D$ = -1mA |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | —— | —— | 20 | mΩ | $V_{GS}$ = -10V, $I_D$ = -42A ③ |
| $V_{GS(th)}$ | Gate Threshold Voltage | -2.0 | —— | -4.0 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = -250µA |
| gfs | Forward Transconductance | 19 | —— | —— | S | $V_{DS}$ = -25V, $I_D$ = -42A |
| $I_{DSS}$ | Drain-to-Source Leakage Current | —— | —— | -25 | µA | $V_{DS}$ = -55V, $V_{GS}$ = 0V |
| | | —— | —— | -200 | | $V_{DS}$ = -44V, $V_{GS}$ = 0V, $T_J$ = 125°C |
| $I_{GSS}$ | Gate-to-Source Forward Leakage | —— | —— | 100 | nA | $V_{GS}$ = -20V |
| | Gate-to-Source Reverse Leakage | —— | —— | -100 | | $V_{GS}$ = 20V |
| $Q_g$ | Total Gate Charge | —— | 120 | 180 | | $I_D$ = -42A |
| $Q_{gs}$ | Gate-to-Source Charge | —— | 32 | —— | nC | $V_{DS}$ = -44V |
| $Q_{gd}$ | Gate-to-Drain ("Miller") Charge | —— | 53 | —— | | $V_{GS}$ = -10V ③ |
| $t_{d(on)}$ | Turn-On Delay Time | —— | 20 | —— | | $V_{DD}$ = -28V |
| $t_r$ | Rise Time | —— | 99 | —— | | $I_D$ = -42A |
| $t_{d(off)}$ | Turn-Off Delay Time | —— | 51 | —— | ns | $R_G$ = 2.6 Ω |
| $t_f$ | Fall Time | —— | 64 | —— | | $V_{GS}$ = -10V ③ |
| $L_S$ | Internal Source Inductance | —— | 7.5 | —— | nH | Between lead, and center of die contact |
| $C_{iss}$ | Input Capacitance | —— | 3500 | —— | | $V_{GS}$ = 0V |
| $C_{oss}$ | Output Capacitance | —— | 1250 | —— | | $V_{DS}$ = -25V |
| $C_{rss}$ | Reverse Transfer Capacitance | —— | 450 | —— | pF | $f$ = 1.0MHz |
| $C_{oss}$ | Output Capacitance | —— | 4620 | —— | | $V_{GS}$ = 0V, $V_{DS}$ = -1.0V, $f$ = 1.0MHz |
| $C_{oss}$ | Output Capacitance | —— | 940 | —— | | $V_{GS}$ = 0V, $V_{DS}$ = -44V, $f$ = 1.0MHz |
| $C_{oss}$ eff. | Effective Output Capacitance | —— | 1530 | —— | | $V_{GS}$ = 0V, $V_{DS}$ = 0V to -44V ④ |

## Source-Drain Ratings and Characteristics

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $I_S$ | Continuous Source Current (Body Diode) | —— | —— | -42 | A | MOSFET symbol showing the |
| $I_{SM}$ | Pulsed Source Current (Body Diode) ① | —— | —— | -280 | | integral reverse p-n junction diode. |
| $V_{SD}$ | Diode Forward Voltage | —— | —— | -1.3 | V | $T_J$ = 25°C, $I_S$ = -42A, $V_{GS}$ = 0V ③ |
| $t_{rr}$ | Reverse Recovery Time | —— | 61 | 92 | ns | $T_J$ = 25°C, $I_F$ = -42A, $V_{DD}$ = -28V |
| $Q_{rr}$ | Reverse Recovery Charge | —— | 150 | 220 | nC | di/dt = -100A/µs ③ |
| $t_{on}$ | Forward Turn-On Time | Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD) | | | | |
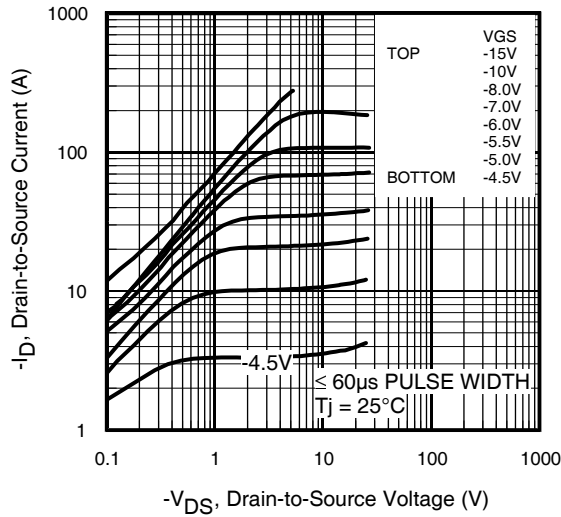
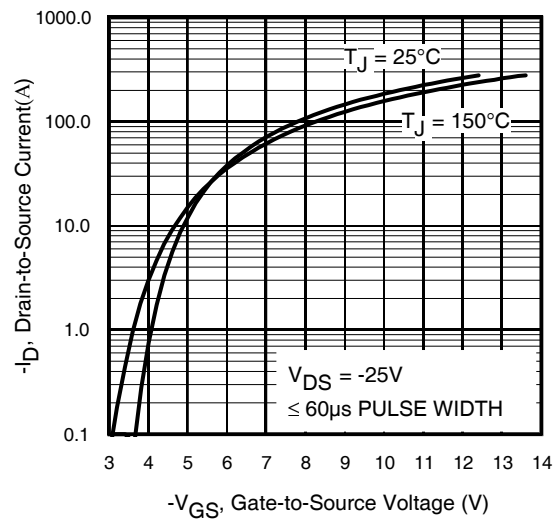**Fig 1.** Typical Output Characteristics
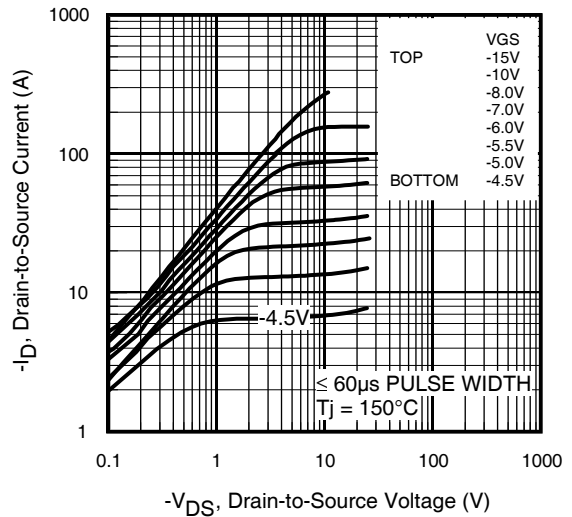
**Fig 2.** Typical Output Characteristics

**Fig 3.** Typical Transfer Characteristics
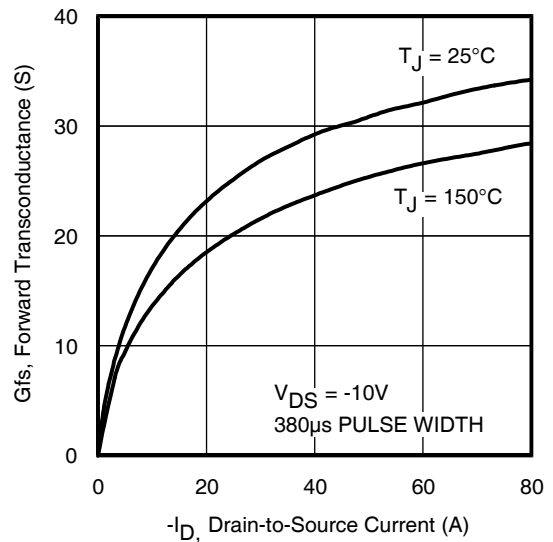
**Fig 4.** Typical Forward Transconductance Vs. Drain Current
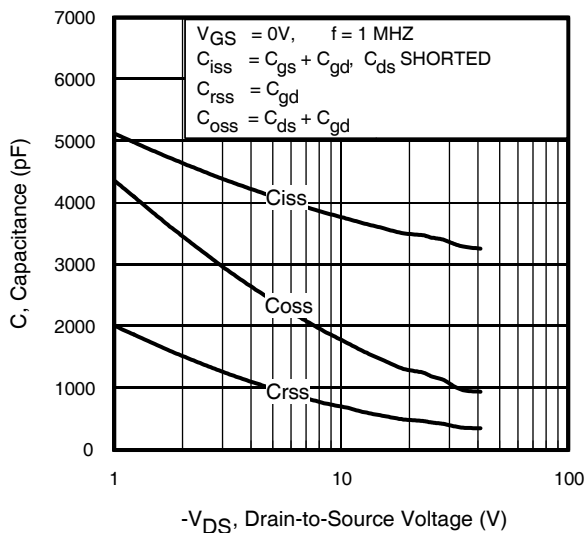
Fig 5. Typical Capacitance Vs.
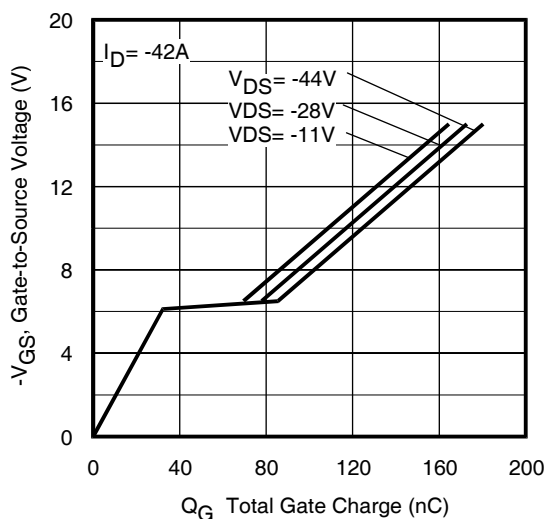Drain-to-Source Voltage



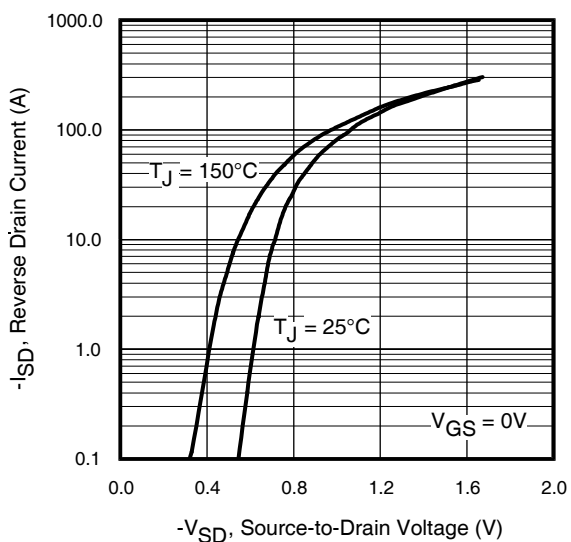Fig 6. Typical Gate Charge Vs.
Gate-to-Source Voltage
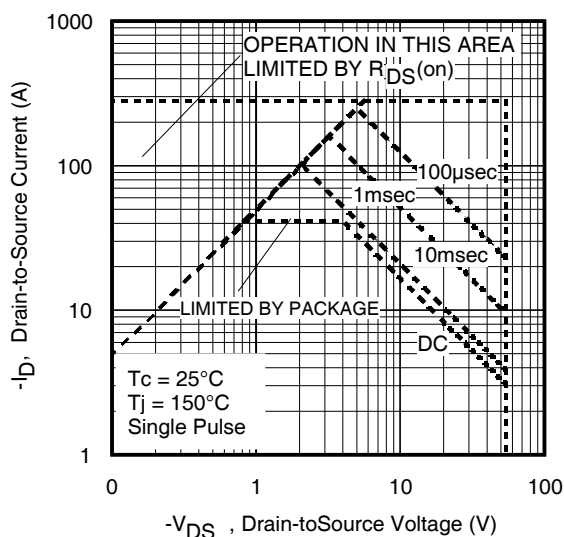


Fig 7. Typical Source-Drain Diode
Forward Voltage



Fig 8. Maximum Safe Operating Area
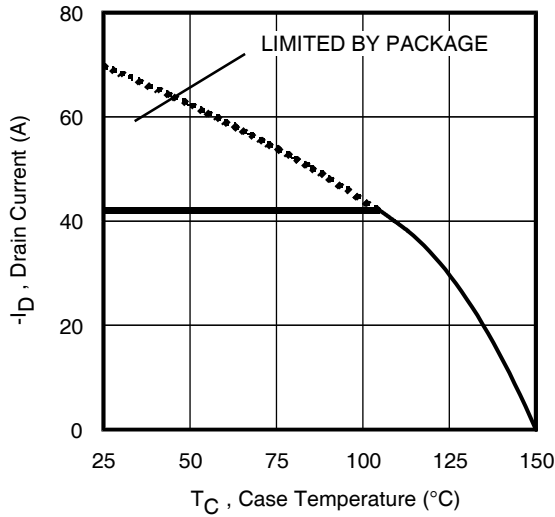
**Fig 9.** Maximum Drain Current Vs. Case Temperature

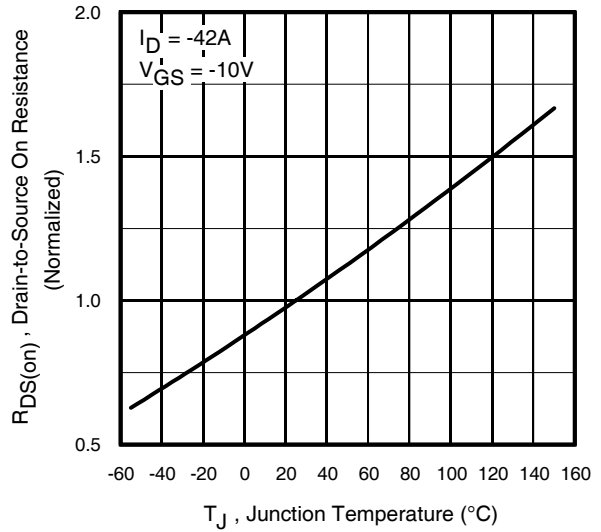

**Fig 10.** Normalized On-Resistance Vs. Temperature
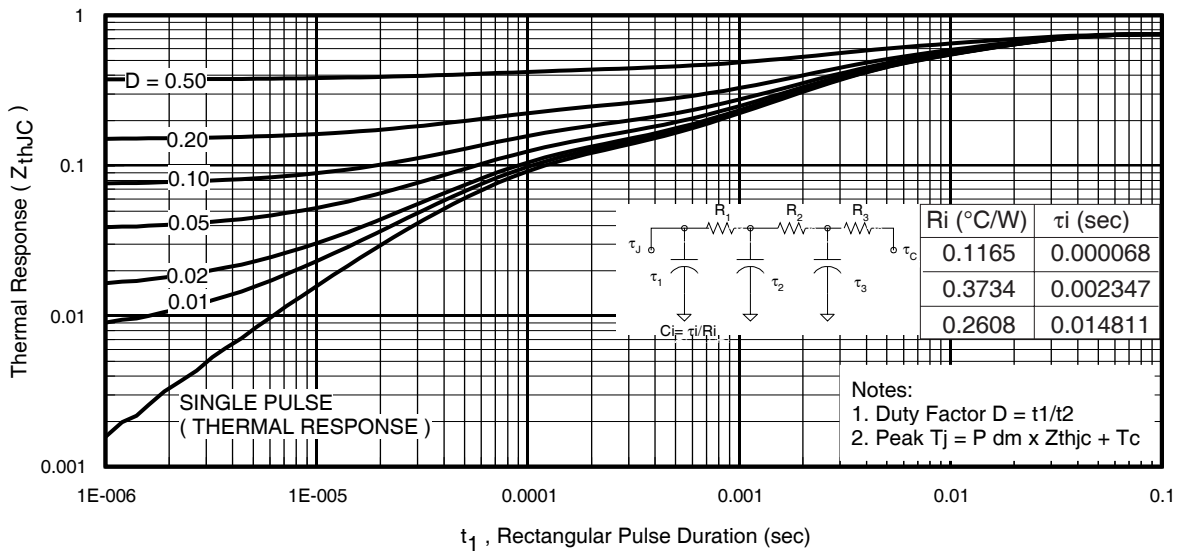


**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

# IRF4905S/L
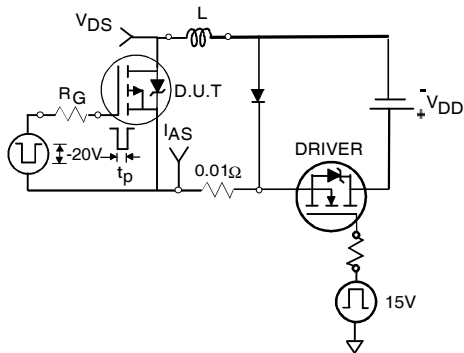
**Fig 12a.** Unclamped Inductive Test Circuit
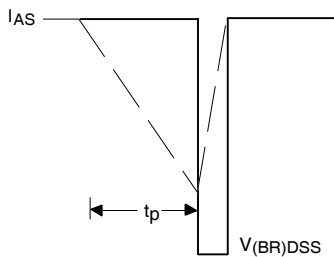


**Fig 12b.** Unclamped Inductive Waveforms



**Fig 13a.** Basic Gate Charge Waveform
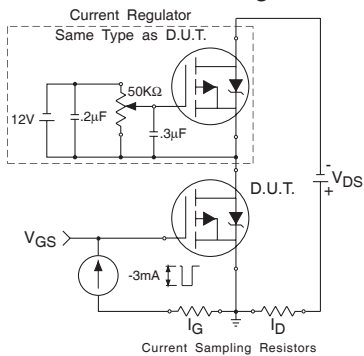


**Fig 13b.** Gate Charge Test Circuit



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

$I_D$
TOP        -17A
           -30A
BOTTOM  -42A



$I_D = -250\mu A$
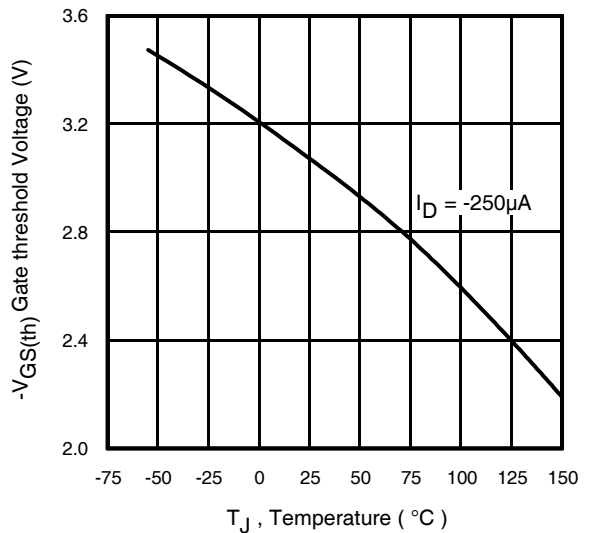
**Fig 14.** Threshold Voltage Vs. Temperature

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IRF4905S/L



Allowed avalanche Current vs avalanche pulsewidth, tav assuming ΔTj = 25°C due to avalanche losses. Note: In no case should Tj be allowed to exceed Tjmax
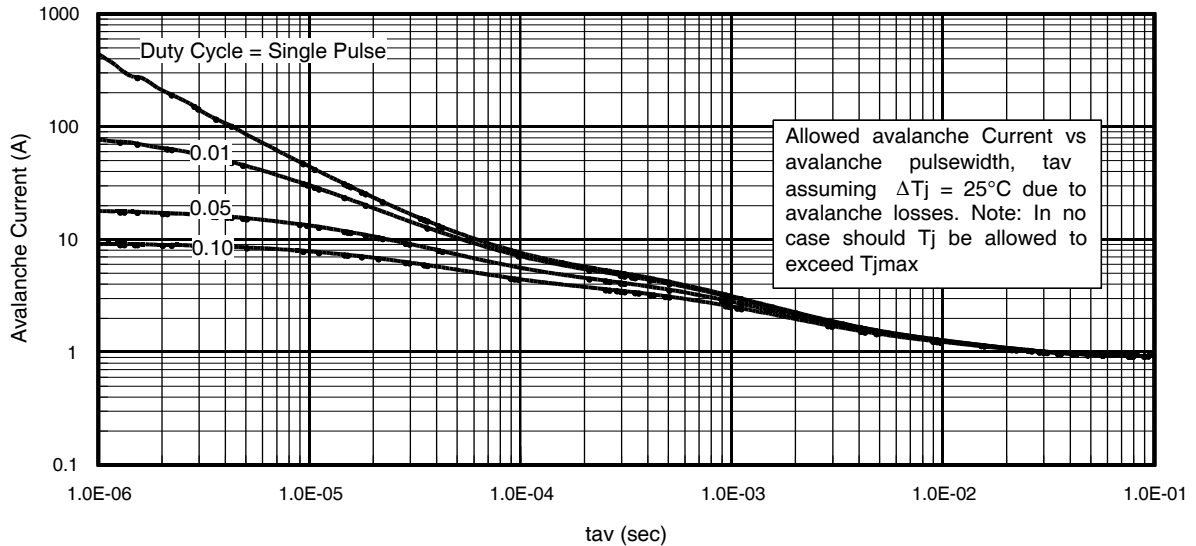
**Fig 15.** Typical Avalanche Current Vs.Pulsewidth



TOP       Single Pulse
BOTTOM   1% Duty Cycle
$I_D$ = -42A
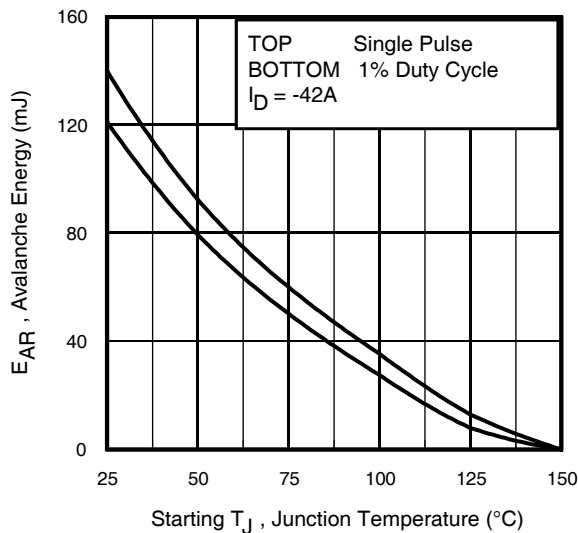
**Fig 16.** Maximum Avalanche Energy Vs. Temperature

**Notes on Repetitive Avalanche Curves , Figures 15, 16:**
**(For further info, see AN-1005 at www.irf.com)**
1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of $T_{jmax}$. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as $T_{jmax}$ is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. $I_{av}$ = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed $T_{jmax}$ (assumed as 25°C in Figure 15, 16).
   $t_{av}$ = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D (ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS (AR)} = P_{D (ave)} \cdot t_{av}$$

# IRF4905S/L

**Circuit Layout Considerations**
- Low Stray Inductance
- Ground Plane
- Low Leakage Inductance Current Transformer

- dv/dt controlled by $R_G$
- Driver same type as D.U.T.
- $I_{SD}$ controlled by Duty Factor "D"
- D.U.T. - Device Under Test

** Reverse Polarity of D.U.T for P-Channel
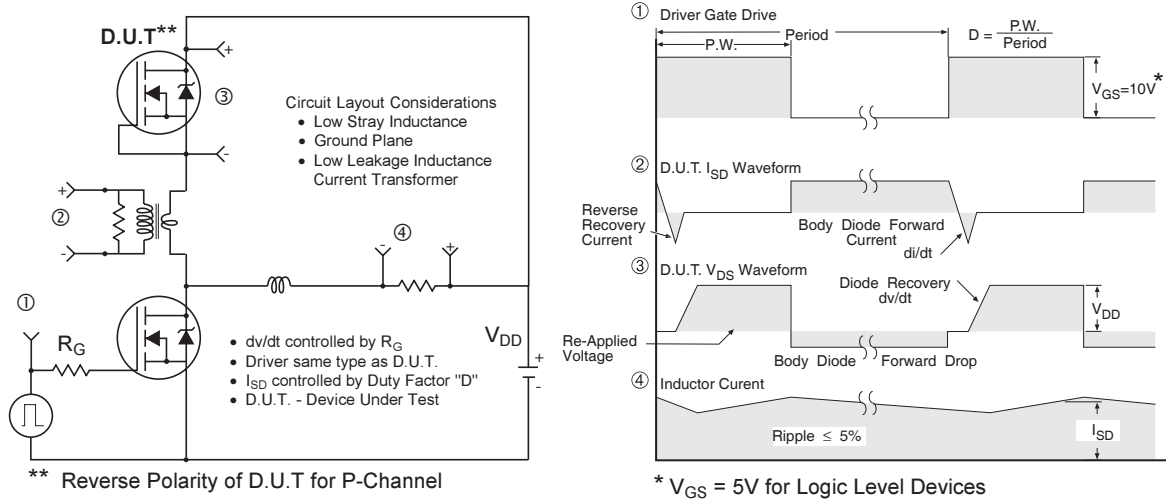
* $V_{GS}$ = 5V for Logic Level Devices

**Fig 17.** Peak Diode Recovery dv/dt Test Circuit for P-Channel HEXFET® Power MOSFETs
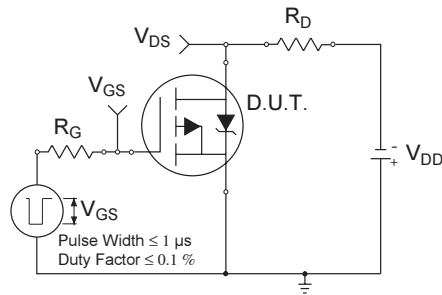


**Fig 18a.** Switching Time Test Circuit

Pulse Width ≤ 1 µs
Duty Factor ≤ 0.1 %
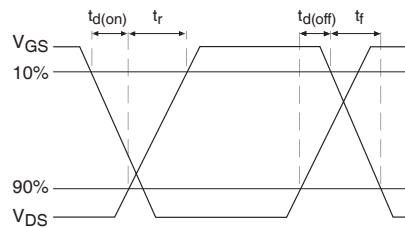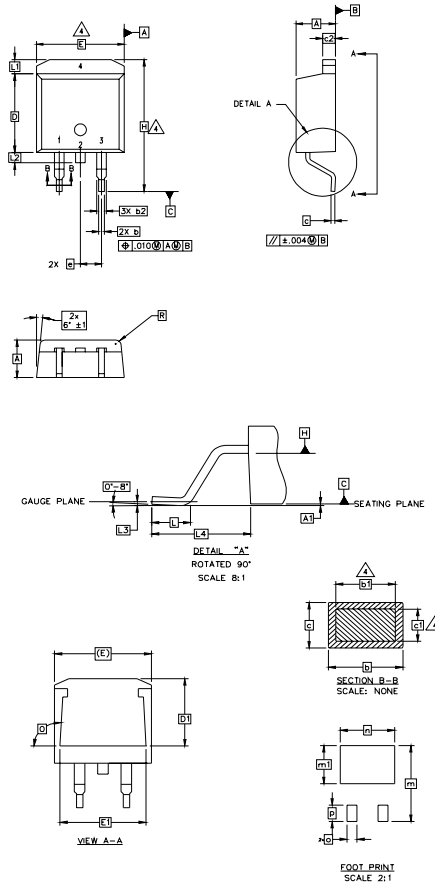


**Fig 18b.** Switching Time Waveforms

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## D²Pak Package Outline (Dimensions are shown in millimeters (inches))



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994

2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.

4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.

5. CONTROLLING DIMENSION: INCH.

| SYMBOL | DIMENSIONS | | | | NOTES |
| | MILLIMETERS | | INCHES | | |
| | MIN. | MAX. | MIN. | MAX. | |
|---|---|---|---|---|---|
| A | 4.06 | 4.83 | .160 | .190 | |
| A1 | 0.00 | 0.254 | .000 | .010 | |
| b | 0.51 | 0.99 | .020 | .039 | |
| b1 | 0.51 | 0.89 | .020 | .035 | 4 |
| b2 | 1.14 | 1.78 | .045 | .070 | |
| c | 0.38 | 0.74 | .015 | .029 | |
| c1 | 0.38 | 0.58 | .015 | .023 | 4 |
| c2 | 1.14 | 1.65 | .045 | .065 | |
| D | 8.51 | 9.65 | .335 | .380 | 3 |
| D1 | 6.86 | | .270 | | |
| E | 9.65 | 10.67 | .380 | .420 | 3 |
| E1 | 6.22 | | .245 | | |
| e | 2.54 BSC | | .100 BSC | | |
| H | 14.61 | 15.88 | .575 | .625 | |
| L | 1.78 | 2.79 | .070 | .110 | |
| L1 | | 1.65 | | .065 | |
| L2 | 1.27 | 1.78 | .050 | .070 | |
| L3 | 0.25 BSC | | .010 BSC | | |
| L4 | 4.78 | 5.28 | .188 | .208 | |
| m | 17.78 | | .700 | | |
| m1 | 8.89 | | .350 | | |
| n | 11.43 | | .450 | | |
| o | 2.08 | | .082 | | |
| p | 3.81 | | .150 | | |
| R | 0.51 | 0.71 | .020 | .028 | |
| θ | 90° | 93° | 90° | 93° | |

LEAD ASSIGNMENTS

HEXFET

1.— GATE
2, 4.— DRAIN
3.— SOURCE

IGBTs, CoPACK

1.— GATE
2, 4.— COLLECTOR
3.— EMITTER

DIODES

1.— ANODE *
2, 4.— CATHODE
3.— ANODE

* PART DEPENDENT.

## D²Pak Part Marking Information



EXAMPLE: THIS IS AN IRF530S WITH LOT CODE 8024 ASSEMBLED ON WW 02, 2000 IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line position indicates "Lead-Free"

OR

INTERNATIONAL RECTIFIER LOGO — F530S — PART NUMBER
80 — 002L — DATE CODE YEAR 0 = 2000 WEEK 02 LINE L
24
ASSEMBLY LOT CODE

INTERNATIONAL RECTIFIER LOGO — F530S — PART NUMBER
80 — P002A — DATE CODE P = DESIGNATES LEAD-FREE PRODUCT (OPTIONAL) YEAR 0 = 2000 WEEK 02 A = ASSEMBLY SITE CODE
24
ASSEMBLY LOT CODE
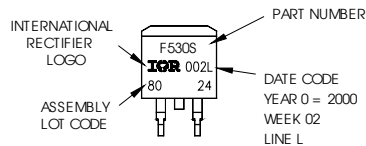
# IRF4905S/L

## TO-262 Package Outline (Dimensions are shown in millimeters (inches))



SECTION B-B
SCALE: NONE

| S Y M B O L | DIMENSIONS | | | | N O T E S |
|---|---|---|---|---|---|
| | MILLIMETERS | | INCHES | | |
| | MIN. | MAX. | MIN. | MAX. | |
| A | 4.06 | 4.83 | .160 | .190 | |
| A1 | 2.03 | 2.92 | .080 | .115 | |
| b | 0.51 | 0.99 | .020 | .039 | |
| b1 | 0.51 | 0.89 | .020 | .035 | 4 |
| b2 | 1.14 | 1.40 | .045 | .055 | |
| c | 0.38 | 0.63 | .015 | .025 | 4 |
| c1 | 1.14 | 1.40 | .045 | .055 | |
| c2 | 0.43 | .063 | .017 | .029 | |
| D | 8.51 | 9.65 | .335 | .380 | 3 |
| D1 | 5.33 | | .210 | | |
| E | 9.65 | 10.67 | .380 | .420 | 3 |
| E1 | 6.22 | | .245 | | |
| e | 2.54 BSC | | .100 BSC | | |
| L | 13.46 | 14.09 | .530 | .555 | |
| L1 | 3.56 | 3.71 | .140 | .146 | |
| L2 | | 1.65 | | .065 | |

LEAD ASSIGNMENTS

HEXFET
1.- GATE
2.- DRAIN
3.- SOURCE
4.- DRAIN

IGBT
1- GATE
2- COLLECTOR
3- EMITTER
4- COLLECTOR

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5. CONTROLLING DIMENSION: INCH.

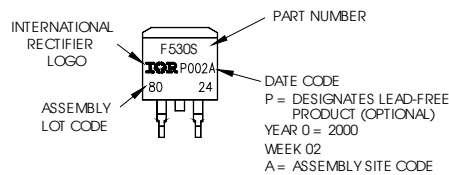## TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

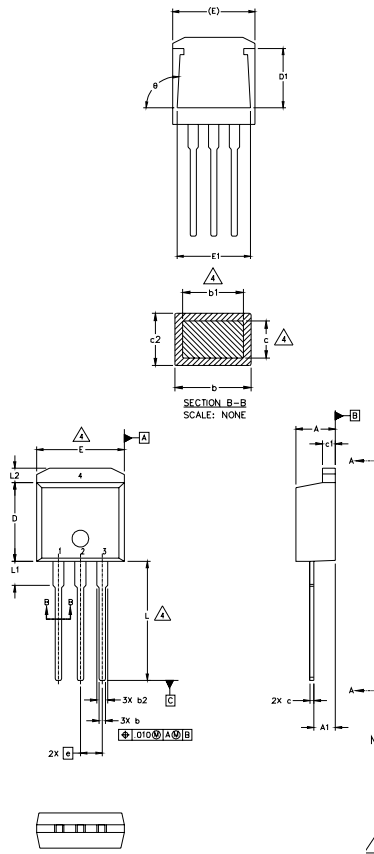Note: "P" in assembly line position indicates "Lead-Free"



INTERNATIONAL RECTIFIER LOGO
PART NUMBER
ASSEMBLY LOT CODE
DATE CODE
YEAR 7 = 1997
WEEK 19
LINE C

OR



INTERNATIONAL RECTIFIER LOGO
PART NUMBER
ASSEMBLY LOT CODE
DATE CODE
P = DESIGNATES LEAD-FREE PRODUCT (OPTIONAL)
YEAR 7 = 1997
WEEK 19
A = ASSEMBLY SITE CODE
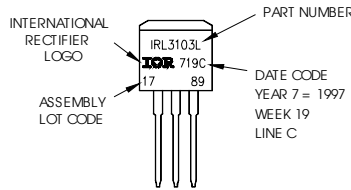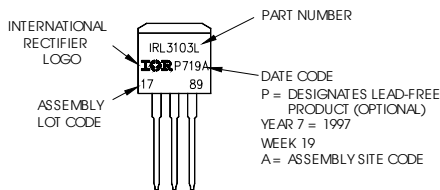
# D²Pak Tape & Reel Information

TRR

FEED DIRECTION

TRL

FEED DIRECTION

1.60 (.063)
1.50 (.059)

4.10 (.161)
3.90 (.153)

Ø 1.60 (.063)
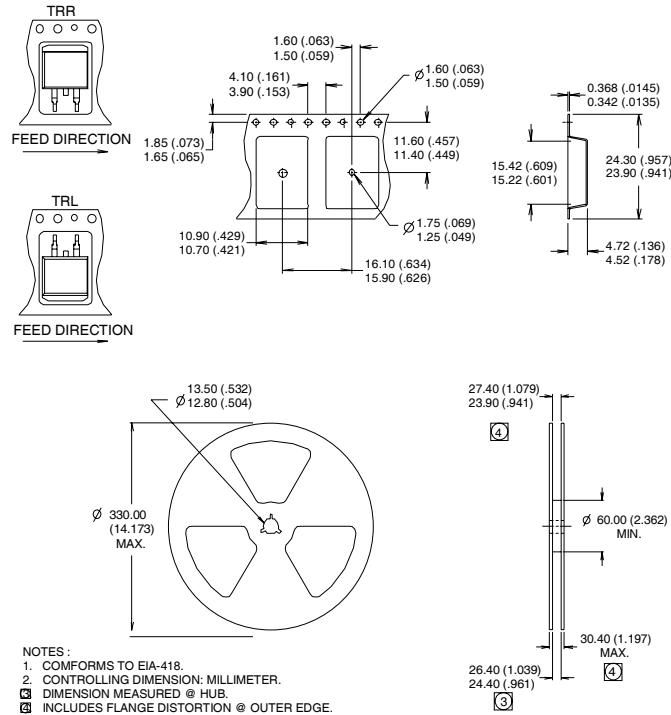1.50 (.059)

1.85 (.073)
1.65 (.065)

11.60 (.457)
11.40 (.449)

0.368 (.0145)
0.342 (.0135)

15.42 (.609)
15.22 (.601)

24.30 (.957)
23.90 (.941)

10.90 (.429)
10.70 (.421)

Ø 1.75 (.069)
1.25 (.049)

16.10 (.634)
15.90 (.626)

4.72 (.136)
4.52 (.178)

13.50 (.532)
Ø 12.80 (.504)

27.40 (1.079)
23.90 (.941)

4

Ø 330.00
(14.173)
MAX.

Ø 60.00 (2.362)
MIN.

30.40 (1.197)
MAX.

4

26.40 (1.039)
24.40 (.961)

3

NOTES :
1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
3 DIMENSION MEASURED @ HUB.
4 INCLUDES FLANGE DISTORTION @ OUTER EDGE.

**Notes:**

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).

② Limited by $T_{Jmax}$, starting $T_J = 25°C$, L = 0.16mH $R_G = 25\Omega$, $I_{AS}$ = -42A, $V_{GS}$ =-10V. Part not recommended for use above this value.

③ Pulse width ≤ 1.0ms; duty cycle ≤ 2%.

④ $C_{oss}$ eff. is a fixed capacitance that gives the same charging time as $C_{oss}$ while $V_{DS}$ is rising from 0 to 80% $V_{DSS}$ .

⑤ Limited by $T_{Jmax}$ , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.

⑥ This value determined from sample failure population. 100% tested to this value in production.

⑦ This is applied to D²Pak, when mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

⑧ $R_\theta$ is measured at $T_J$ approximately 90°C

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

International IƏR Rectifier

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