

NLSF308

Quad Gate 2-Input AND

The NLSF308 is an advanced high speed CMOS 2-input AND gate fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

- High Speed: $t_{PD} = 4.3$ ns (Typ) at $V_{CC} = 5.0$ V
- Low Power Dissipation: $I_{CC} = 2.0$ μ A (Max) at $T_A = 25^\circ$ C
- High Noise Immunity: $V_{NIH} = V_{NIL} = 28\%$ V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2.0 V to 5.5 V Operating Range
- Low Noise: $V_{OLP} = 0.8$ V (Max)
- Function Compatible with Other Standard Logic Families
- QFN-16 Package
- Latchup Performance Exceeds 300 mA
- ESD Performance: Human Body Model; > 2000 V;
Machine Model; > 200 V
- Chip Complexity: 24 FETs or 6 Equivalent Gates



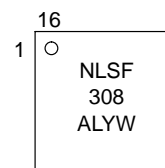
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MARKING DIAGRAM



**QFN-16
MN SUFFIX
CASE 485G**



(Top View)

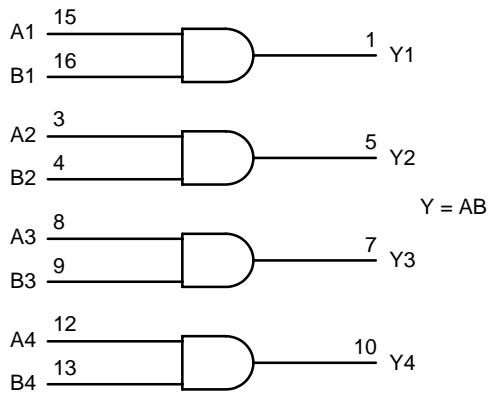
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

| Device | Package | Shipping† |
|-------------|-------------|------------------|
| NLSF308MN | QFN-16, 3x3 | 123 Units/Rail |
| NLSF308MNR2 | QFN-16, 3x3 | 3000/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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FUNCTION TABLE

| Inputs | | Output |
|--------|---|--------|
| A | B | Y |
| L | L | L |
| L | H | L |
| H | L | L |
| H | H | H |

Figure 1. LOGIC DIAGRAM

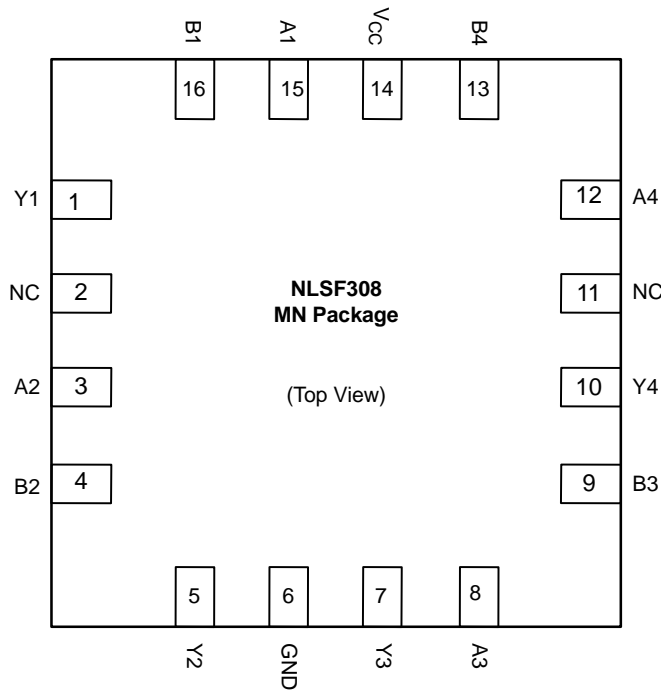


Figure 2. Pin Assignment (QFN-16)

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MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
|------------------|---|-------------------------------|------|
| V _{CC} | DC Supply Voltage | -0.5 to + 7.0 | V |
| V _{in} | DC Input Voltage | -0.5 to + 7.0 | V |
| V _{out} | DC Output Voltage | -0.5 to V _{CC} + 0.5 | V |
| I _{IK} | Input Diode Current | -20 | mA |
| I _{OK} | Output Diode Current | ±20 | mA |
| I _{out} | DC Output Current, per Pin | ±25 | mA |
| I _{CC} | DC Supply Current, V _{CC} and GND Pins | ±50 | mA |
| P _D | Power Dissipation in Still Air | 450 | mW |
| T _{stg} | Storage Temperature | -65 to + 150 | °C |

Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If stress limits are exceeded device functional operation is not implied, damage may occur and reliability may be affected. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|---------------------------------|--|--------|-----------------|------|
| V _{CC} | DC Supply Voltage | 2.0 | 5.5 | V |
| V _{in} | DC Input Voltage | 0 | 5.5 | V |
| V _{out} | DC Output Voltage | 0 | V _{CC} | V |
| T _A | Operating Temperature | -40 | + 85 | °C |
| t _r , t _f | Input Rise and Fall Time V _{CC} = 3.3 V ±0.3 V V _{CC} = 5.0 V ±0.5 V | 0 0 | 100 20 | ns/V |

DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Conditions | V _{CC} V | T _A = 25°C | | | T _A = - 40 to 85°C | | Unit |
|-----------------|-----------------------------------|---|----------------------|-------------------------------|-------------------|-------------------------------|-------------------------------|-------------------------------|------|
| | | | | Min | Typ | Max | Min | Max | |
| V _{IH} | Minimum High-Level Input Voltage | | 2.0 3.0 to 5.5 | 1.50 V _{CC} x 0.7 | | | 1.50 V _{CC} x 0.7 | | V |
| V _{IL} | Maximum Low-Level Input Voltage | | 2.0 3.0 to 5.5 | | | 0.50 V _{CC} x 0.3 | | 0.50 V _{CC} x 0.3 | V |
| V _{OH} | Minimum High-Level Output Voltage | V _{in} = V _{IH} or V _{IL} I _{OH} = -50 μA | 2.0 3.0 4.5 | 1.9 2.9 4.4 | 2.0 3.0 4.5 | | 1.9 2.9 4.4 | | V |
| | | V _{in} = V _{IH} or V _{IL} I _{OH} = -4 mA, I _{OH} = -8 mA | 3.0 4.5 | 2.58 3.94 | | | 2.48 3.80 | | |
| V _{OL} | Maximum Low-Level Output Voltage | V _{in} = V _{IH} or V _{IL} I _{OL} = 50 μA | 2.0 3.0 4.5 | | 0.0 0.0 0.0 | 0.1 0.1 0.1 | | 0.1 0.1 0.1 | V |
| | | V _{in} = V _{IH} or V _{IL} I _{OL} = 4 mA I _{OL} = 8 mA | 3.0 4.5 | | | 0.36 0.36 | | 0.44 0.44 | |
| I _{in} | Maximum Input Leakage Current | V _{in} = 5.5 V or GND | 0 to 5.5 | | | ± 0.1 | | ± 1.0 | μA |
| I _{CC} | Maximum Quiescent Supply Current | V _{in} = V _{CC} or GND | 5.5 | | | 2.0 | | 20.0 | μA |

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AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

| Symbol | Parameter | Test Conditions | $T_A = 25^\circ\text{C}$ | | | $T_A = -40$ to 85°C | | Unit |
|--------------------------|--|---|--------------------------|------------|-------------|-----------------------------------|--------------|------|
| | | | Min | Typ | Max | Min | Max | |
| t_{PLH} , t_{PHL} | Maximum Propagation Delay, A or B to Y | $V_{CC} = 3.3 \pm 0.3$ V, $C_L = 15$ pF, $C_L = 50$ pF | | 6.2 8.7 | 8.8 12.3 | 1.0 1.0 | 10.5 14.0 | ns |
| | | | | 4.3 5.8 | 5.9 7.9 | 1.0 1.0 | 7.0 9.0 | |
| C_{in} | Maximum Input Capacitance | | 4 | 10 | | 10 | pF | |
| C_{PD} | Power Dissipation Capacitance (Note 1) | Typical @ 25°C , $V_{CC} = 5.0$ V | | | | | pF | |
| | | 18 | | | | | | |

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}/4$ (per gate). C_{PD} is used to determine the no-load dynamic power consumption; $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns, $C_L = 50$ pF, $V_{CC} = 5.0$ V)

| Symbol | Characteristic | $T_A = 25^\circ\text{C}$ | | Unit |
|-----------|--|--------------------------|------|------|
| | | Typ | Max | |
| V_{OLP} | Quiet Output Maximum Dynamic V_{OL} | 0.3 | 0.8 | V |
| V_{OLV} | Quiet Output Minimum Dynamic V_{OL} | -0.3 | -0.8 | V |
| V_{IHD} | Minimum High Level Dynamic Input Voltage | | 3.5 | V |
| V_{ILD} | Maximum Low Level Dynamic Input Voltage | | 1.5 | V |

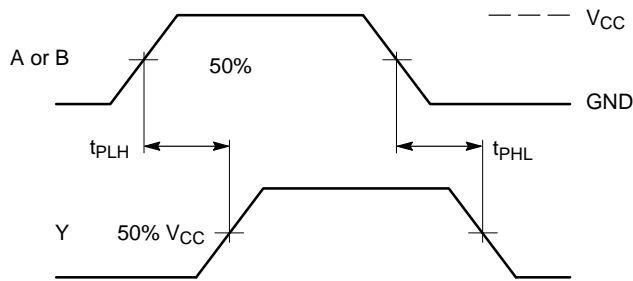
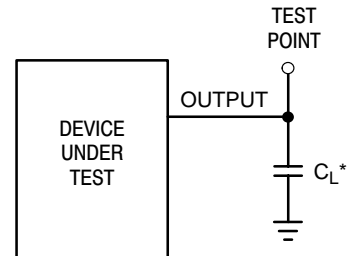


Figure 3. Switching Waveforms



*Includes all probe and jig capacitance

Figure 4. Test Circuit

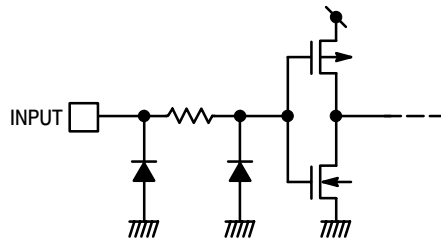
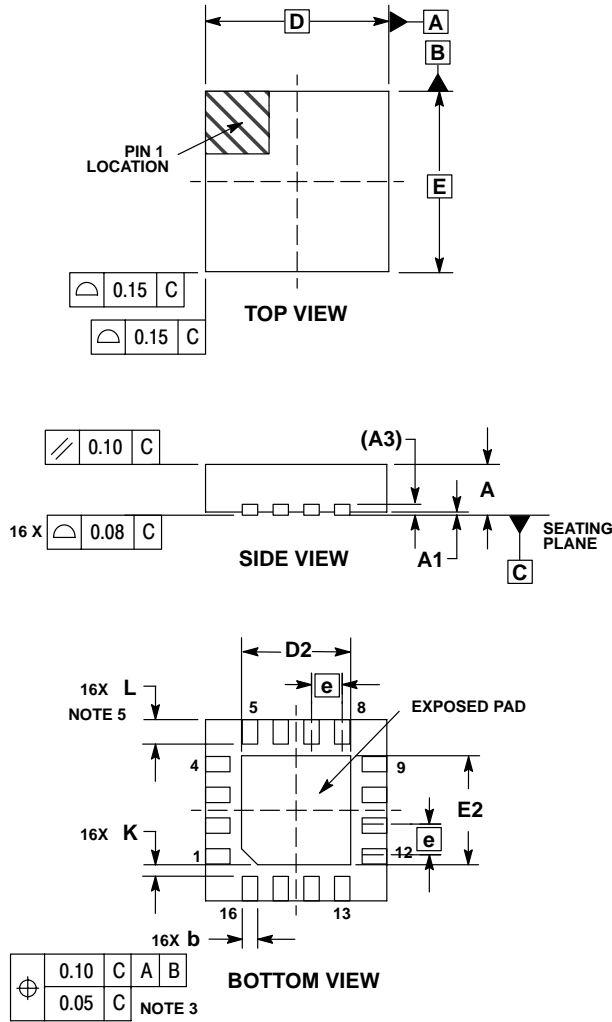


Figure 5. Input Equivalent Circuit

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PACKAGE DIMENSIONS

QFN-16
MN SUFFIX
CASE 485G-01
ISSUE B

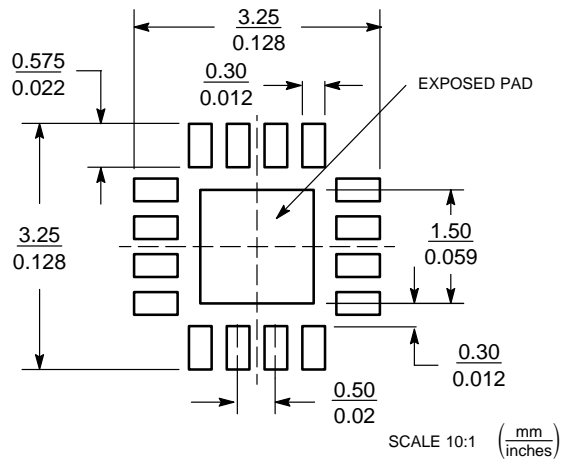


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. L_{max} CONDITION CAN NOT VIOLATE 0.2 MM MINIMUM SPACING BETWEEN LEAD TIP AND FLAG


| MILLIMETERS | | |
|-------------|------|------|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 | REF |
| b | 0.18 | 0.30 |
| D | 3.00 | BSC |
| D2 | 1.65 | 1.85 |
| E | 3.00 | BSC |
| E2 | 1.65 | 1.85 |
| e | 0.50 | BSC |
| K | 0.20 | --- |
| L | 0.30 | 0.50 |

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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