



32K x 8 Static RAM

Features

- High speed  
— 12 ns
- Fast t<sub>DOE</sub>
- CMOS for optimum speed/power
- Low active power  
— 880 mW
- Low standby power  
— 165 mW
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features
- TTL-compatible inputs and outputs
- Automatic power-down when deselected

Functional Description

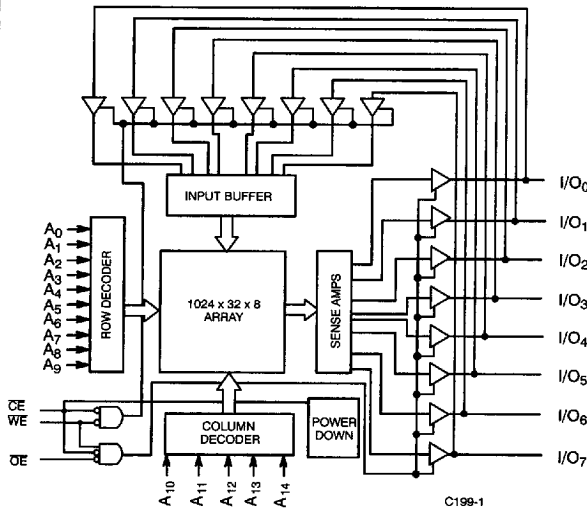
The CY7C199 is a high-performance CMOS static RAM organized as 32,768 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ( $\overline{CE}$ ) and active LOW output enable ( $\overline{OE}$ ) and three-state drivers. This device has an automatic power-down feature, reducing the power consumption by 81% when deselected. The CY7C199 is in the standard 300-mil-wide DIP, SOJ, and LCC packages.

An active LOW write enable signal ( $\overline{WE}$ ) controls the writing/reading operation of the memory. When  $\overline{CE}$  and  $\overline{WE}$  inputs are both LOW, data on the eight data input/

output pins (I/O<sub>0</sub> through I/O<sub>7</sub>) is written into the memory location addressed by the address present on the address pins (A<sub>0</sub> through A<sub>14</sub>). Reading the device is accomplished by selecting the device and enabling the outputs,  $\overline{CE}$  and  $\overline{OE}$  active LOW, while  $\overline{WE}$  remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

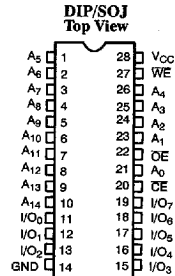
The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable ( $\overline{WE}$ ) is HIGH. A die coat is used to ensure alpha immunity.

Logic Block Diagram

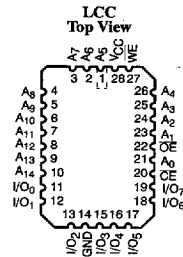


C199-1

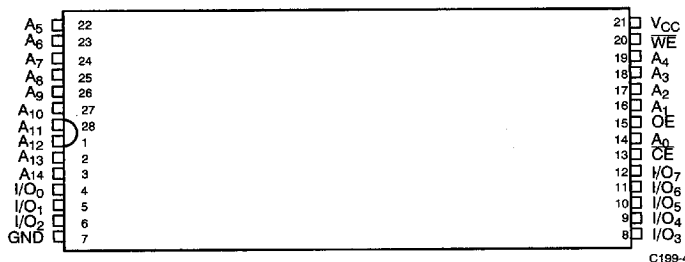
Pin Configurations



C199-2



C199-3

**Pin Configurations (continued)**
**TSOP  
Top View**

**Selection Guide**

	7C199-10	7C199-12	7C199-15	7C199-20	7C199-25	7C199-35	7C199-45
Maximum Access Time (ns)	10	12	15	20	25	35	45
Maximum Operating Current (mA)	Com <sup>1</sup>	160	160	155	150	150	140
	L		130	110	100	100	100
	Mil			180	170	150	150
	L			150	130	130	130
Maximum Standby Current (mA)	30	30	30	30	30	25	25
	L		20	20	15	15	15

Shaded area contains preliminary information.

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage to Ground Potential (Pin 28 to Pin 14)	-0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State <sup>[1]</sup>	-0.5V to V <sub>CC</sub> + 0.5V
DC Input Voltage <sup>[1]</sup>	-0.5V to V <sub>CC</sub> + 0.5V

Output Current into Outputs (LOW)	20 mA
Static Discharge Voltage (per MIL-STD-883, Method 3015)	>2001V
Latch-Up Current	>200 mA

**Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	5V ± 10%
Military <sup>[2]</sup>	-55°C to +125°C	5V ± 10%

**Electrical Characteristics Over the Operating Range<sup>[3]</sup>**

Parameter	Description	Test Conditions	7C199-10		7C199-12		7C199-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> + 0.3V	2.2	V <sub>CC</sub> + 0.3V	2.2	V <sub>CC</sub> + 0.3V	V
V <sub>IL</sub>	Input LOW Voltage		-0.5	0.8	-0.5	0.8	-0.5	0.8	V
I <sub>Ix</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-5	+5	-5	+5	-5	+5	μA

Shaded area contains preliminary information.

**Notes:**

- V<sub>IL</sub> (min.) = -2.0V for pulse durations of less than 20 ns.
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.

**Electrical Characteristics** Over the Operating Range<sup>[3]</sup> (continued)

Parameter	Description	Test Conditions	7C199-10		7C199-12		7C199-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled	-5	+5	-5	+5	-5	+5	μA
I <sub>OS</sub>	Output Short Circuit Current <sup>[4]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND		-300		-300		-300	mA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	Com'1	160		160		155	mA
			L			130		110	
			Mil					180	
			L					150	
I <sub>SB1</sub>	Automatic CE Power-Down Current—TTL Inputs	Max. V <sub>CC</sub> , CE ≥ V <sub>IH</sub> , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>		30		30		30	mA
			L			20		20	
I <sub>SB2</sub>	Automatic CE Power-Down Current—CMOS Inputs	Max. V <sub>CC</sub> , CE ≥ V <sub>CC</sub> - 0.3V V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V, f = 0	Com'1	10		10		10	mA
			L			500		500	
			Mil					15	
			L					5	

Shaded area contains preliminary information.

**Electrical Characteristics** Over the Operating Range<sup>[3]</sup> (continued)

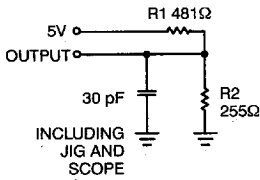
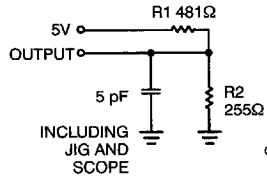
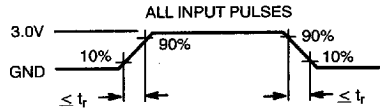
Parameter	Description	Test Conditions	7C199-20		7C199-25		7C199-35, 45		Unit	
			Min.	Max.	Min.	Max.	Min.	Max.		
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		2.4		2.4		V	
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4		0.4	V	
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> + 0.3V	2.2	V <sub>CC</sub> + 0.3V	2.2	V <sub>CC</sub> + 0.3V	V	
V <sub>IL</sub>	Input LOW Voltage		-0.5	0.8	-3.0	0.8	-3.0	0.8	V	
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-5	+5	-5	+5	-5	+5	μA	
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	-5	+5	-5	+5	-5	+5	μA	
I <sub>OS</sub>	Output Short Circuit Current <sup>[4]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND		-300		-300		-300	mA	
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	Com'1	150		150		140	mA	
			L		100		100			100
			Mil		170		150			150
			L		130		130			130
I <sub>SB1</sub>	Automatic CE Power-Down Current—TTL Inputs	Max. V <sub>CC</sub> , CE ≥ V <sub>IH</sub> , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>		30		30		25	mA	
			L		15		15			15
I <sub>SB2</sub>	Automatic CE Power-Down Current—CMOS Inputs	Max. V <sub>CC</sub> , CE ≥ V <sub>CC</sub> - 0.3V V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V, f = 0	Com'1	15		15		15	mA	
			L		500		500			500
			Mil		15		15			15
			L		5		5			5

**Note:**

4. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

**Capacitance<sup>[5]</sup>**

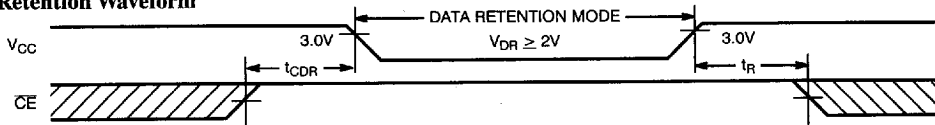
Parameter	Description	Test Conditions	Max.	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = 5.0\text{V}$	8	pF
$C_{OUT}$	Output Capacitance		8	pF

**AC Test Loads and Waveforms<sup>[6]</sup>**

**(a) Normal Load**

**(b) High-Z Load**

**C199-6**

Equivalent to: THÉVENIN EQUIVALENT  
 $167\Omega$   
 OUTPUT  $\longleftrightarrow$  1.73V

**Data Retention Characteristics (Over the Operating Range)**

Parameter	Description	Conditions <sup>[7]</sup>	Min.	Max.	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		2.0		V
$I_{CCDR}$	Data Retention Current	Com'1	$V_{CC} = V_{DR} = 2.0\text{V}$ , $CE \geq V_{CC} - 0.3\text{V}$ , $V_{IN} \geq V_{CC} - 0.3\text{V}$ or $V_{IN} \leq 0.3\text{V}$	10	$\mu\text{A}$
		Mil		100	
$t_{CDR}^{[5]}$	Chip Deselect to Data Retention Time		0		ns
$t_R^{[5]}$	Operation Recovery Time		$t_{RC}$		ns

**Data Retention Waveform**

**C199-7**
**Notes:**

- Tested initially and after any design or process changes that may affect these parameters.
- $t_r \leq 3\text{ ns}$  for the -12 and -15 speeds.  $t_r \leq 5\text{ ns}$  for the -20 and slower speeds.
- No input may exceed  $V_{CC} + 0.5\text{V}$ .

**Switching Characteristics Over the Operating Range<sup>[3, 8]</sup>**

Parameter	Description	7C199-10		7C199-12		7C199-15		7C199-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>										
t <sub>RC</sub>	Read Cycle Time	10		12		15		20		ns
t <sub>AA</sub>	Address to Data Valid		10		12		15		20	ns
t <sub>OHA</sub>	Data Hold from Address Change	3		3		3		3		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid		10		12		15		20	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		5		5		7		9	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z <sup>[9]</sup>	0		0		0		0		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[9, 10]</sup>		5		5		7		9	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low Z <sup>[9]</sup>	3		3		3		3		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High Z <sup>[9, 10]</sup>		5		5		7		9	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to Power-Down		10		12		15		20	ns
<b>WRITE CYCLE<sup>[11, 12]</sup></b>										
t <sub>WC</sub>	Write Cycle Time	10		12		15		20		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	7		9		10		15		ns
t <sub>AW</sub>	Address Set-Up to Write End	7		9		10		15		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		0		0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	7		8		9		15		ns
t <sub>SD</sub>	Data Set-Up to Write End	5		8		9		10		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		0		0		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[10]</sup>		5		7		7		10	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z <sup>[9]</sup>	3		3		3		3		ns

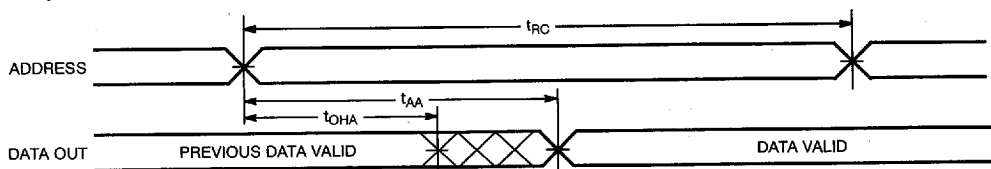
Shaded area contains preliminary information.

**Notes:**

- Test conditions assume signal transition time of 3 ns or less for -12 and -15 speeds and 5 ns or less for -20 and slower speeds, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30-pF load capacitance.
- At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.
- t<sub>HZOE</sub>, t<sub>HZCE</sub>, and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- The minimum write cycle time for write cycle #3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of t<sub>HZWE</sub> and t<sub>SD</sub>.

**Switching Characteristics Over the Operating Range<sup>[3, 8]</sup> (continued)**

Parameter	Description	7C199-25		7C199-35		7C199-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>								
$t_{RC}$	Read Cycle Time	25		35		45		ns
$t_{AA}$	Address to Data Valid		25		35		45	ns
$t_{OHA}$	Data Hold from Address Change	3		3		3		ns
$t_{ACE}$	$\overline{CE}$ LOW to Data Valid		25		35		45	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		10		16		16	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z <sup>[9]</sup>	3		3		3		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[9, 10]</sup>		11		15		15	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low Z <sup>[9]</sup>	3		3		3		ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High Z <sup>[9, 10]</sup>		11		15		15	ns
$t_{PU}$	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
$t_{PD}$	$\overline{CE}$ HIGH to Power-Down		20		20		25	ns
<b>WRITE CYCLE<sup>[11, 12]</sup></b>								
$t_{WC}$	Write Cycle Time	25		35		45		ns
$t_{SCE}$	$\overline{CE}$ LOW to Write End	18		22		22		ns
$t_{AW}$	Address Set-Up to Write End	20		30		40		ns
$t_{HA}$	Address Hold from Write End	0		0		0		ns
$t_{SA}$	Address Set-Up to Write Start	0		0		0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	18		22		22		ns
$t_{SD}$	Data Set-Up to Write End	10		15		15		ns
$t_{HD}$	Data Hold from Write End	0		0		0		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[10]</sup>		11		15		15	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z <sup>[9]</sup>	3		3		3		ns

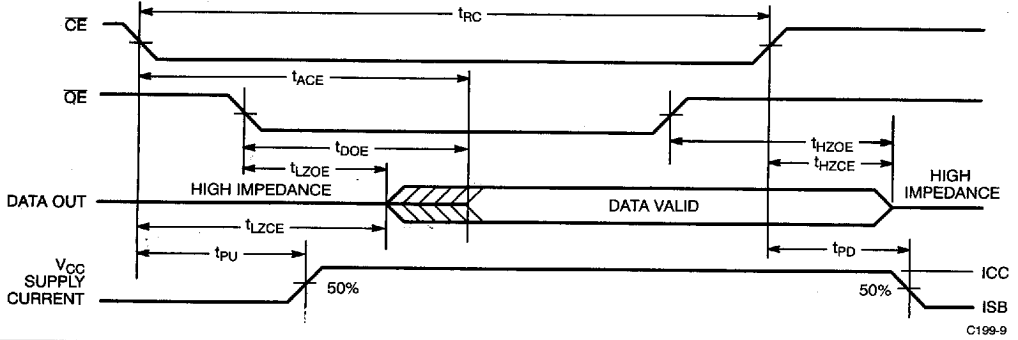
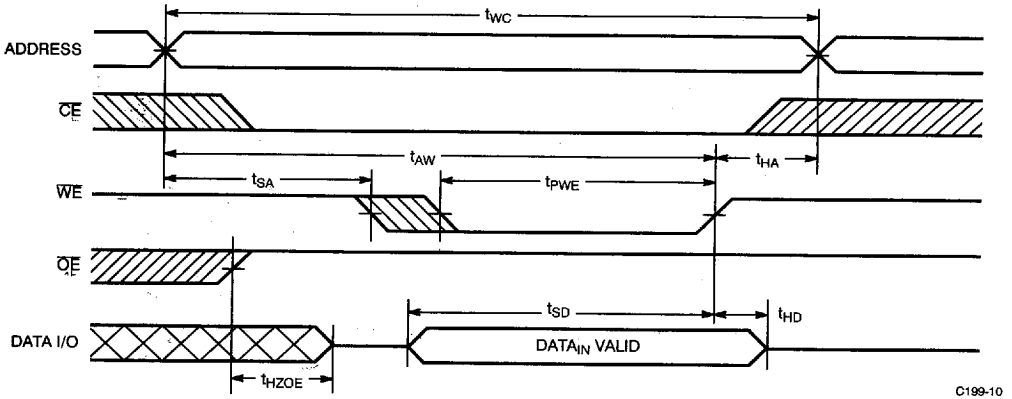
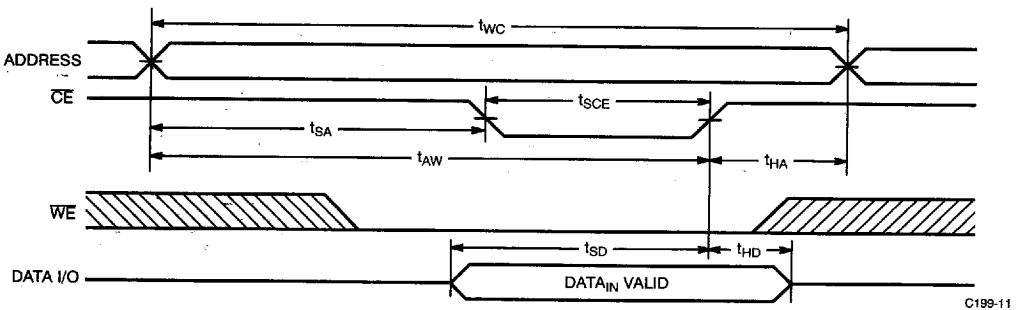
**Switching Waveforms**
**Read Cycle No. 1<sup>[13, 14]</sup>**


C199-8

**Notes:**

 13. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$  =  $V_{IL}$ .

 14.  $\overline{WE}$  is HIGH for read cycle.

**Switching Waveforms (continued)**
**Read Cycle No. 2<sup>[14, 15]</sup>**

**Write Cycle No. 1 (WE Controlled)<sup>[11, 16, 17]</sup>**

**Write Cycle No. 2 (CE Controlled)<sup>[11, 16, 17]</sup>**

**Notes:**

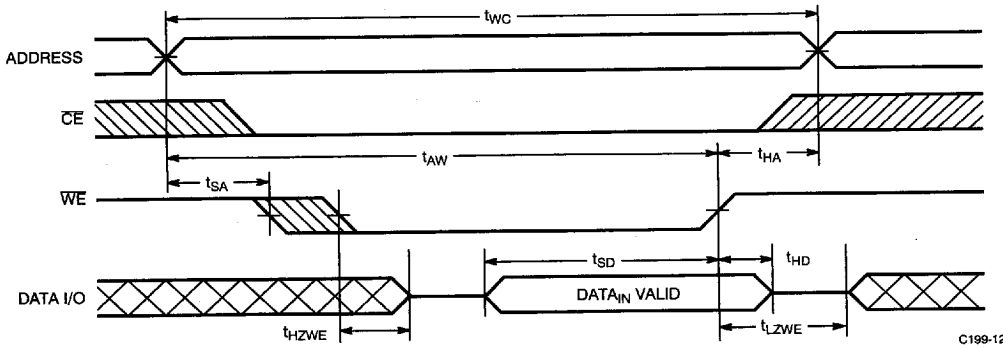
15. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.  
 16. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .

17. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.



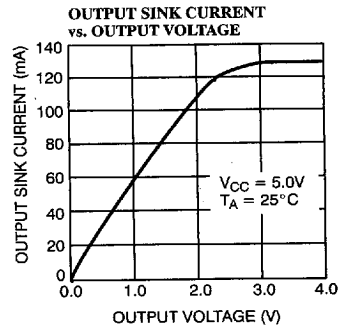
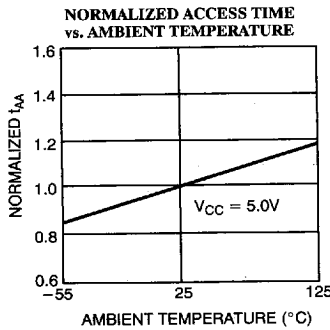
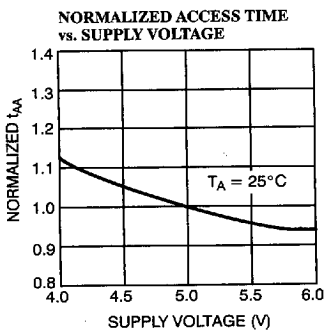
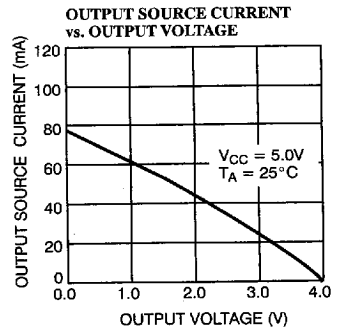
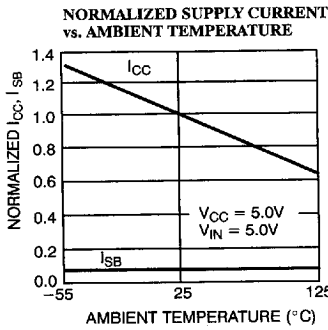
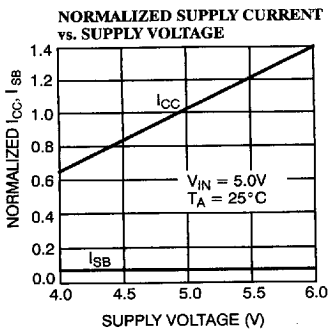
Switching Waveforms (continued)

Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)[12, 17]

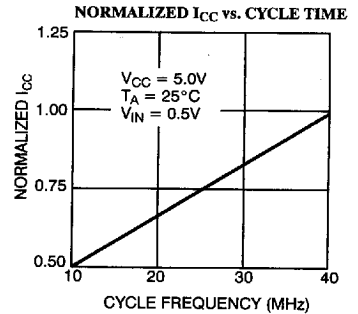
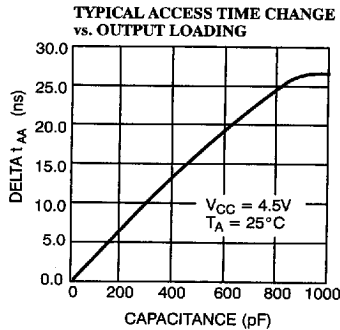
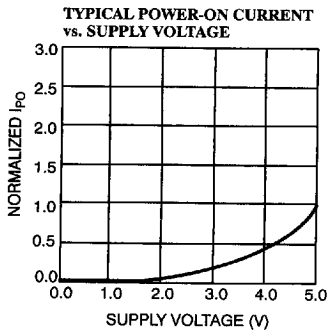


C199-12

Typical DC and AC Characteristics





**Typical DC and AC Characteristics (continued)**

**Truth Table**

CE	WE	OE	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
L	H	L	Data Out	Read	Active ( $I_{CC}$ )
L	L	X	Data In	Write	Active ( $I_{CC}$ )
L	H	H	High Z	Deselect, Output Disabled	Active ( $I_{CC}$ )

**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range	
10	CY7C199-10VC	V21	28-Lead Molded SOJ	Commercial	
12	CY7C199-12PC	P21	28-Lead (300-Mil) Molded DIP	Commercial	
	CY7C199L-12PC	P21	28-Lead (300-Mil) Molded DIP		
	CY7C199-12VC	V21	28-Lead Molded SOJ		
	CY7C199L-12VC	V21	28-Lead Molded SOJ		
	CY7C199-12ZC	Z28	28-Lead Thin Small Outline Package		
15	CY7C199L-12ZC	Z28	28-Lead Thin Small Outline Package	Commercial	
	CY7C199-15PC	P21	28-Lead (300-Mil) Molded DIP		
	CY7C199L-15PC	P21	28-Lead (300-Mil) Molded DIP		
	CY7C199-15VC	V21	28-Lead Molded SOJ		
	CY7C199L-15VC	V21	28-Lead Molded SOJ		
	CY7C199-15ZC	Z28	28-Lead Thin Small Outline Package		
	CY7C199L-15ZC	Z28	28-Lead Thin Small Outline Package		
	CY7C199-15DMB	D22	28-Lead (300-Mil) CerDIP		Military
	CY7C199L-15DMB	D22	28-Lead (300-Mil) CerDIP		
	CY7C199-15LMB	L54	28-Pin Rectangular Leadless Chip Carrier		
CY7C199L-15LMB	L54	28-Pin Rectangular Leadless Chip Carrier			
20	CY7C199-20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial	
	CY7C199L-20PC	P21	28-Lead (300-Mil) Molded DIP		
	CY7C199-20VC	V21	28-Lead Molded SOJ		
	CY7C199L-20VC	V21	28-Lead Molded SOJ		
	CY7C199-20ZC	Z28	28-Lead Thin Small Outline Package		
	CY7C199L-20ZC	Z28	28-Lead Thin Small Outline Package		

**Ordering Information** (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7C199-20DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C199L-20DMB	D22	28-Lead (300-Mil) CerDIP	
	CY7C199-20LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
	CY7C199L-20LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
25	CY7C199-25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C199L-25PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C199-25VC	V21	28-Lead Molded SOJ	
	CY7C199L-25VC	V21	28-Lead Molded SOJ	
	CY7C199-25ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199L-25ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199-25DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C199L-25DMB	D22	28-Lead (300-Mil) CerDIP	
	CY7C199-25LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
	CY7C199L-25LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
35	CY7C199-35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C199L-35PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C199-35VC	V21	28-Lead Molded SOJ	
	CY7C199L-35VC	V21	28-Lead Molded SOJ	
	CY7C199-35ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199L-35ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199-35DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C199L-35DMB	D22	28-Lead (300-Mil) CerDIP	
	CY7C199-35LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
	CY7C199L-35LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
45	CY7C199-45DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C199L-45DMB	D22	28-Lead (300-Mil) CerDIP	
	CY7C199-45LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
	CY7C199L-45LMB	L54	28-Pin Rectangular Leadless Chip Carrier	

Shaded area contains preliminary information.

**MILITARY SPECIFICATIONS**  
**Group A Subgroup Testing**
**DC Characteristics**

Parameter	Subgroups
V <sub>OH</sub>	1, 2, 3
V <sub>OL</sub>	1, 2, 3
V <sub>IH</sub>	1, 2, 3
V <sub>IL Max.</sub>	1, 2, 3
I <sub>Ix</sub>	1, 2, 3
I <sub>OZ</sub>	1, 2, 3
I <sub>CC</sub>	1, 2, 3
I <sub>SB1</sub>	1, 2, 3
I <sub>SB2</sub>	1, 2, 3

**Switching Characteristics**

Parameter	Subgroups
<b>READ CYCLE</b>	
t <sub>RC</sub>	7, 8, 9, 10, 11
t <sub>AA</sub>	7, 8, 9, 10, 11
t <sub>OHA</sub>	7, 8, 9, 10, 11
t <sub>ACE</sub>	7, 8, 9, 10, 11
t <sub>DOE</sub>	7, 8, 9, 10, 11
<b>WRITE CYCLE</b>	
t <sub>WC</sub>	7, 8, 9, 10, 11
t <sub>SCE</sub>	7, 8, 9, 10, 11
t <sub>AW</sub>	7, 8, 9, 10, 11
t <sub>HA</sub>	7, 8, 9, 10, 11
t <sub>SA</sub>	7, 8, 9, 10, 11
t <sub>PWE</sub>	7, 8, 9, 10, 11
t <sub>SD</sub>	7, 8, 9, 10, 11
t <sub>HD</sub>	7, 8, 9, 10, 11

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