CY7C1020D

512K (32K x 16) Static RAM

Features

- Pin- and function-compatible with CY7C1020B
- High speed
  - — t_{AA} = 10 ns
- Low active power
  - — I_{CC} = 80 mA @ 10ns
- Low complementary metal oxide semiconductor (CMOS) standby power
  - — I_{SB2} = 3 mA
- 2.0 V data retention
- Automatic power-down when deselected
- CMOS for optimum speed/power
- Independent control of upper and lower bits
- Available in Pb-free 44-pin 400-Mil wide Molded SOJ and 44-pin thin small outline package (TSOP) II packages

Functional Description [1]

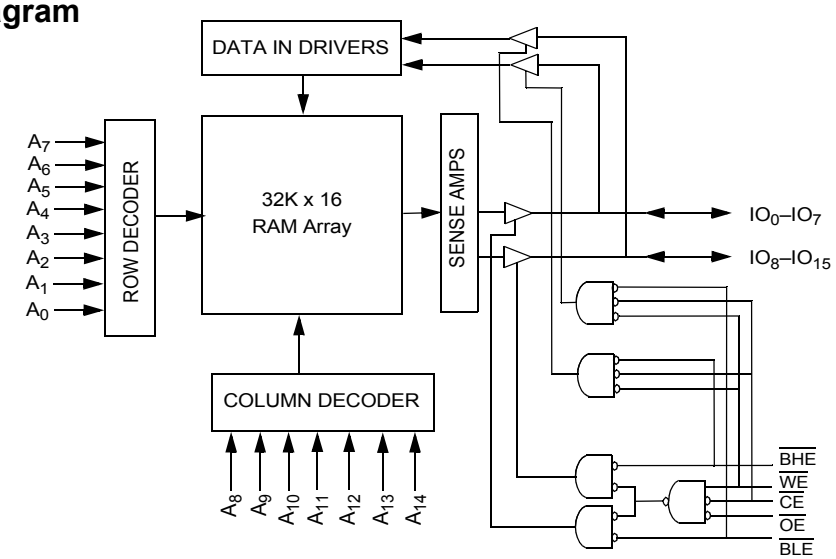
The CY7C1020D is a high-performance CMOS static RAM organized as 32,768 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected.The input and output pins (IO_0 through IO_{15}) are placed in a high-impedance state when:

- Deselected ($\overline{CE}$ HIGH)
- Outputs are disabled ($\overline{OE}$ HIGH)
- $\overline{BHE}$ and $\overline{BLE}$ are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH)
- When the write operation is active ($\overline{CE}$ LOW, and $\overline{WE}$ LOW)

Write to the device by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from IO pins (IO_0 through IO_7), is written into the location specified on the address pins (A_0 through A_{14}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from IO pins (IO_8 through IO_{15}) is written into the location specified on the address pins (A_0 through A_{14}).

Reading from the device by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appears on IO_0 to IO_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on IO_8 to IO_{15}. See the "Truth Table" on page 9 for a complete description of read and write modes.

Logic Block Diagram

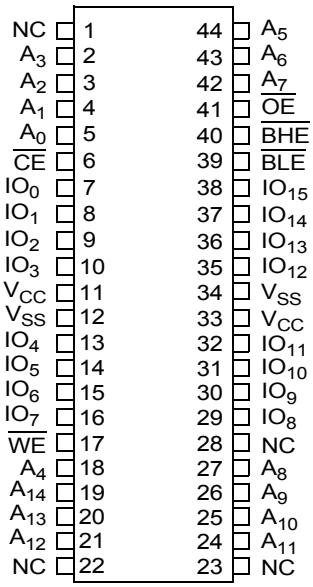


Note
1. For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at www.cypress.com.

Contents

Pin Configurations[2]

SOJ/TSOP II
Top View



Selection Guide

	–10 (Industrial)	Unit
Maximum access time	10	ns
Maximum operating current	80	mA
Maximum CMOS standby current	3	mA

Note
2. NC pins are not connected on the die.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage on V_{CC} to Relative GND [3] ..–0.5 V to +6.0 V

DC voltage applied to outputs in High Z State [3] ..... –0.5 V to V_{CC} + 0.5 V

DC input voltage [3] ..... –0.5 V to V_{CC} + 0.5 V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage..... >2001 V (per MIL-STD-883, Method 3015)

Latch-up current ..... >200mA

Operating Range

Range	Ambient Temperature	V_{CC}	Speed
Industrial	–40 °C to +85 °C	5 V ± 0.5 V	10 ns

Electrical Characteristics (Over the Operating Range)

Parameter	Description	Test Conditions		–10 (Industrial)		Unit
				Min	Max	
V_{OH}	Output HIGH voltage	I_{OH} = –4.0 mA		2.4	–	V
V_{OL}	Output LOW voltage	I_{OL} = 8.0 mA		–	0.4	V
V_{IH}	Input HIGH voltage	–		2.2	V_{CC} + 0.5V	V
V_{IL}	Input LOW voltage [3]	–		–0.5	0.8	V
I_{IX}	Input load current	GND ≤ V_I ≤ V_{CC}		–1	+1	µA
I_{OZ}	Output leakage current	GND ≤ V_I ≤ V_{CC}, output disabled		–1	+1	µA
I_{CC}	V_{CC} operating supply current	V_{CC} = Max, I_{OUT} = 0 mA, f = f_{max} = $1/t_{RC}$	100 MHz	–	80	mA
			83 MHz	–	72	mA
			66 MHz	–	58	mA
			40 MHz	–	37	mA
I_{SB1}	Automatic CE power-down current—TTL inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{IH} V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{max}		–	10	mA
I_{SB2}	Automatic CE Power-Down current—CMOS inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V, or V_{IN} ≤ 0.3V, f = 0		–	3	mA

Note
3. V_{IL} (min) = –2.0 V and V_{IH}(max) = V_{CC} + 1 V for pulse durations of less than 5 ns.

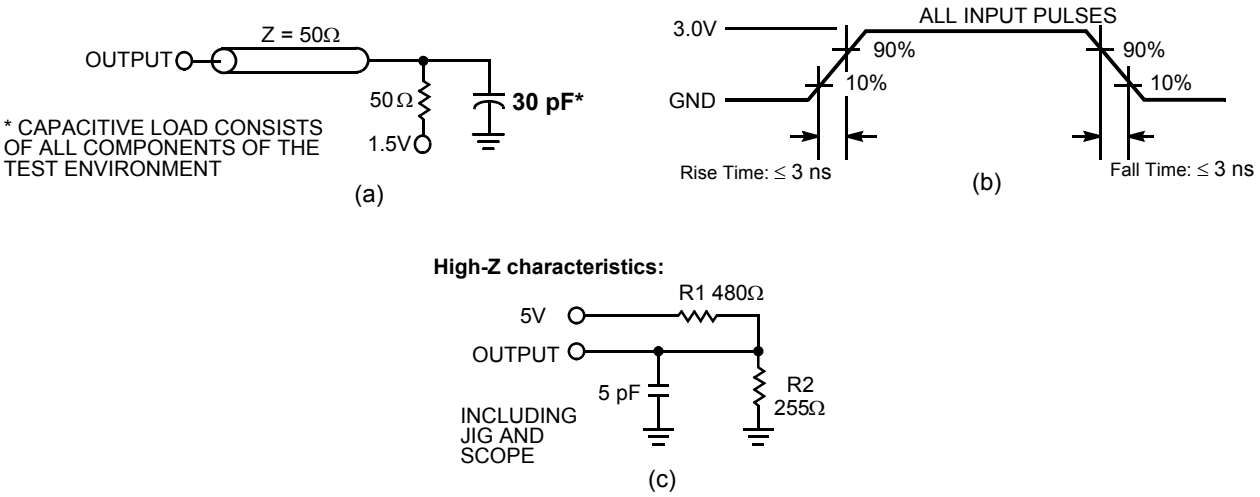
Capacitance [4]

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 5.0 V	8	pF
C_{OUT}	Output capacitance		8	pF

Thermal Resistance [4]

Parameter	Description	Test Conditions	SOJ	TSOP II	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	59.52	53.91	°C/W
Θ_{JC}	Thermal resistance (junction to case)		36.75	21.24	°C/W

AC Test Loads and Waveforms [5]



Notes
4. Tested initially and after any design or process changes that may affect these parameters.
5. AC characteristics (except High-Z) are tested using the load conditions shown in Figure (a). High-Z characteristics are tested for all speeds using the test load shown in Figure (c).

Switching Characteristics (Over the Operating Range) [6]

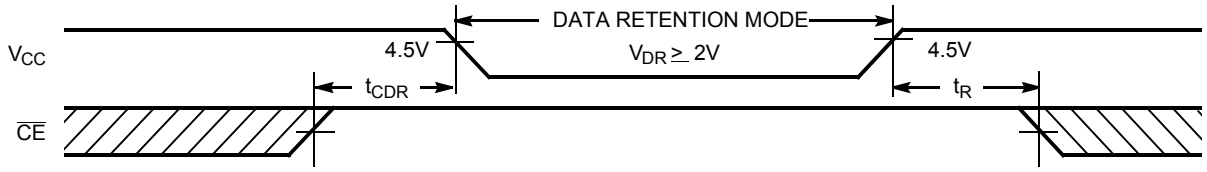
Parameter	Description	–10 (Industrial)		Unit
		Min	Max	
Read Cycle				
t_{power} [7]	V_{CC}(typical) to the first access	100	–	µs
t_{RC}	Read cycle time	10	–	ns
t_{AA}	Address to data valid	–	10	ns
t_{OHA}	Data hold from address change	3	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	10	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	5	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z [9]	0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z [8, 9]	–	5	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z [9]	3	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z [8, 9]	–	5	ns
t_{PU} [10]	$\overline{CE}$ LOW to power-up	0	–	ns
t_{PD} [10]	$\overline{CE}$ HIGH to power-down	–	10	ns
t_{DBE}	Byte enable to data valid		5	ns
t_{LZBE}	Byte enable to Low Z	0	–	ns
t_{HZBE}	Byte disable to High Z	–	5	ns
Write Cycle [11, 12]				
t_{WC}	Write cycle time	10	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	7	–	ns
t_{AW}	Address set-up to write end	7	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address set-up to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	7	–	ns
t_{SD}	Data set-up to write end	6	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [9]	3	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [8, 9]	–	5	ns
t_{BW}	Byte enable to end of write	7	–	ns

Notes
6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access can be performed.
8. t_{HZOE}, t_{HZBE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (c) of "AC Test Loads and Waveforms [5]" on page 5. Transition is measured when the outputs enter a high impedance state.
9. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
10. This parameter is guaranteed by design and is not tested.
11. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW, $\overline{WE}$ LOW and $\overline{BHE}/\overline{BLE}$ LOW. $\overline{CE}$, $\overline{WE}$ and $\overline{BHE}/\overline{BLE}$ must be LOW to initiate a write and the transition of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
12. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min	Max	Unit
V_{DR}	V_{CC} for data retention	–	2.0	–	V
I_{CCDR}	Data retention current	$V_{CC} = V_{DR} = 2.0$ V, $\overline{CE} \geq V_{CC} - 0.3$ V, $V_{IN} \geq V_{CC} - 0.3$ V or $V_{IN} \leq 0.3$ V	–	3	mA
t_{CDR} [13]	Chip deselect to data retention time	–	0	–	ns
t_R [14]	Operation recovery time	–	t_{RC}	–	ns

Data Retention Waveform



Switching Waveforms

Figure 1. Read Cycle No.1 (Address Transition Controlled) [15, 16]

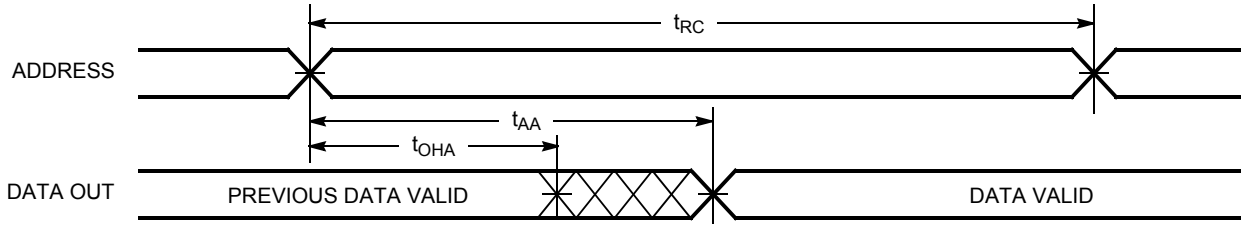
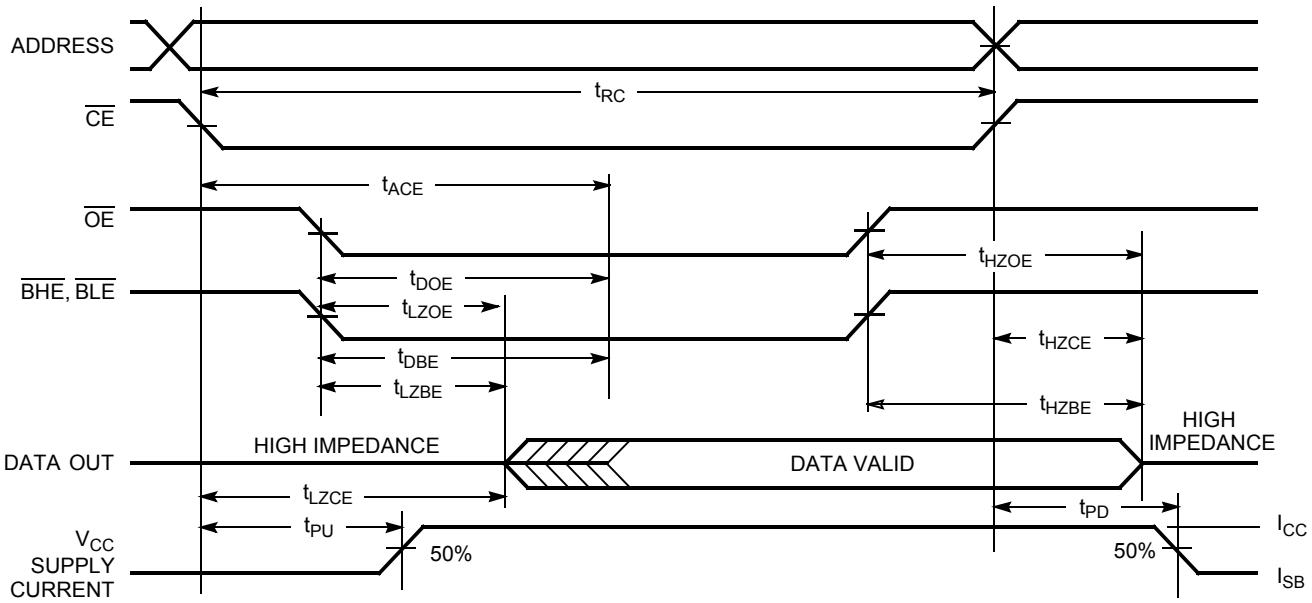


Figure 2. Read Cycle No.2 ($\overline{OE}$ Controlled) [16, 17]



Notes
13. Tested initially and after any design or process changes that may affect these parameters.
14. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 50$ µs or stable at $V_{CC(min)} \geq 50$ µs.
15. Device is continuously selected. OE, CE, BHE and/or BLE = V_{IL}.
16. WE is HIGH for read cycle.
17. Address valid prior to or coincident with CE transition LOW.

Switching Waveforms(continued)

Figure 3. Write Cycle No. 1 ($\overline{CE}$ Controlled) [18, 19]

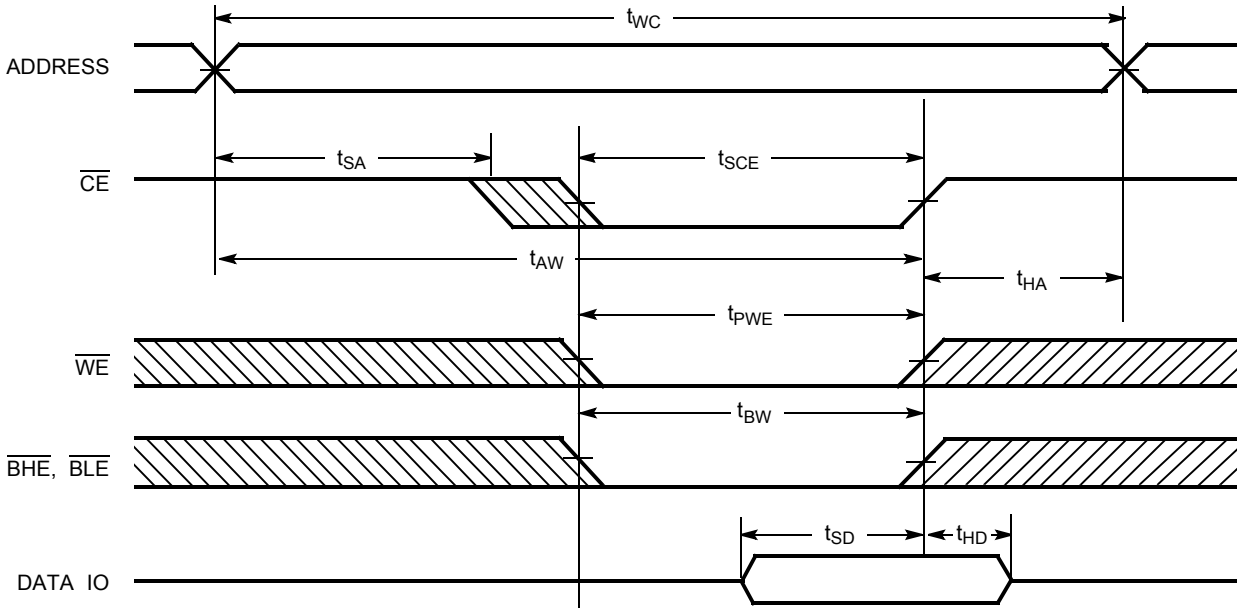
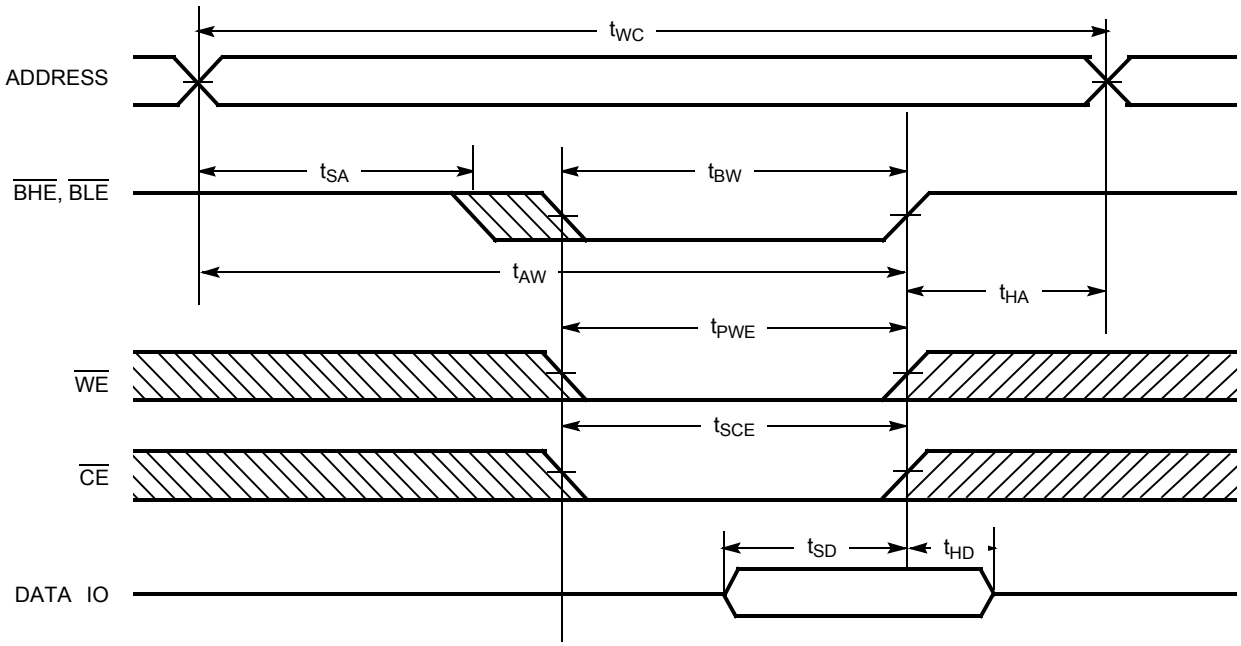


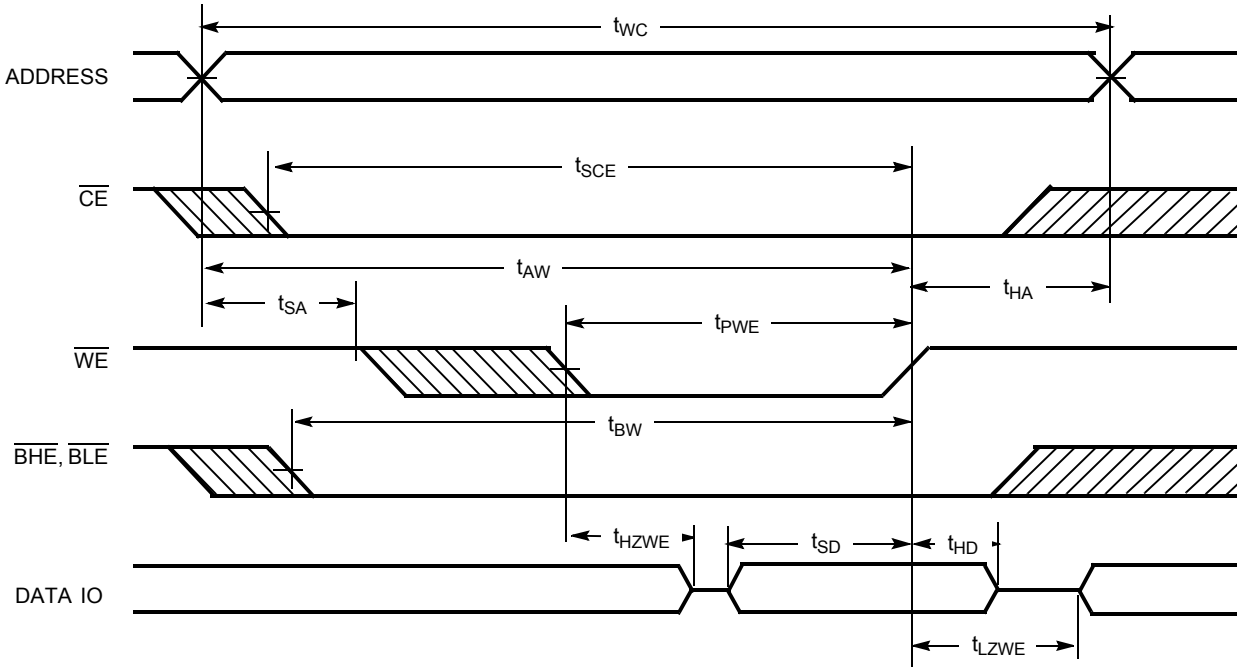
Figure 4. Write Cycle No. 2 ($\overline{BLE}$ or $\overline{BHE}$ Controlled) [18, 19]



Notes
18. Data IO is high impedance if $\overline{OE}$ or $\overline{BHE}$ and/or $\overline{BLE}$= V_{IH}.
19. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms(continued)

Figure 5. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [20, 21]



Truth Table

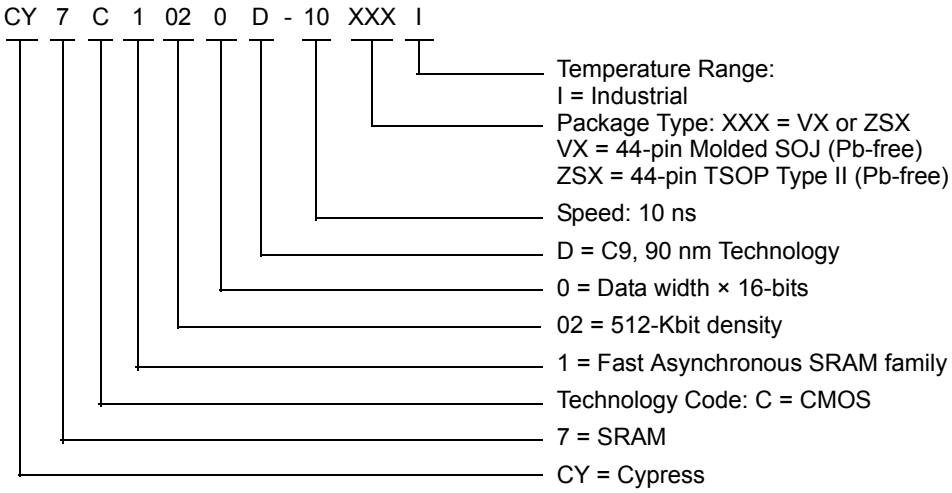
$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	IO_0–IO_7	IO_8–IO_{15}	Mode	Power
H	X	X	X	X	High Z	High Z	Power-down	Standby (I_{SB})
L	L	H	L	L	Data out	Data out	Read – All bits	Active (I_{CC})
			L	H	Data out	High Z	Read – Lower bits only	Active (I_{CC})
			H	L	High Z	Data out	Read – Upper bits only	Active (I_{CC})
L	X	L	L	L	Data in	Data in	Write – All bits	Active (I_{CC})
			L	H	Data in	High Z	Write – Lower bits only	Active (I_{CC})
			H	L	High Z	Data in	Write – Upper bits only	Active (I_{CC})
L	H	H	X	X	High Z	High Z	Selected, outputs disabled	Active (I_{CC})
L	X	X	H	H	High Z	High Z	selected, outputs disabled	Active (I_{CC})

Notes
20. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.
21. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1020D-10VXI	51-85082	44-pin (400-Mil) Molded SOJ (Pb-free)	Industrial
	CY7C1020D-10ZSXI	51-85087	44-pin TSOP Type II (Pb-free)	

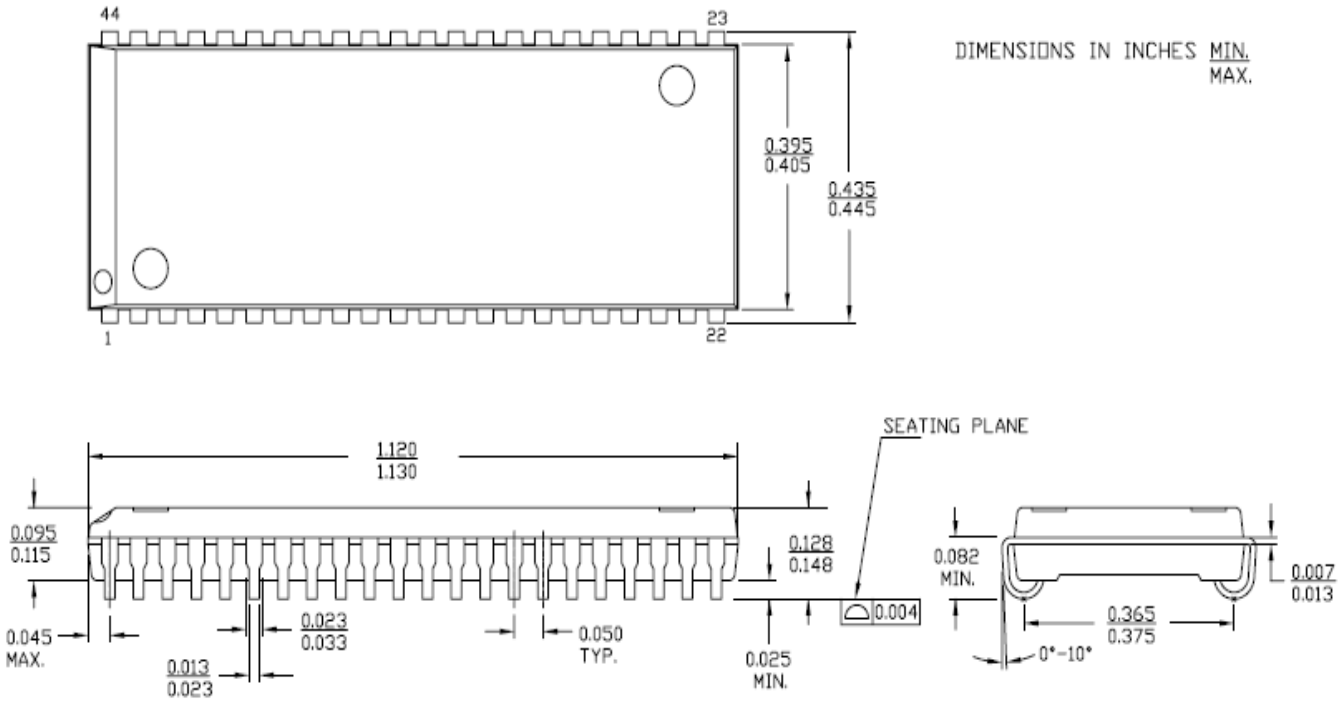
Ordering Code Definitions



Please contact your local Cypress sales representative for availability of these parts.

Package Diagrams

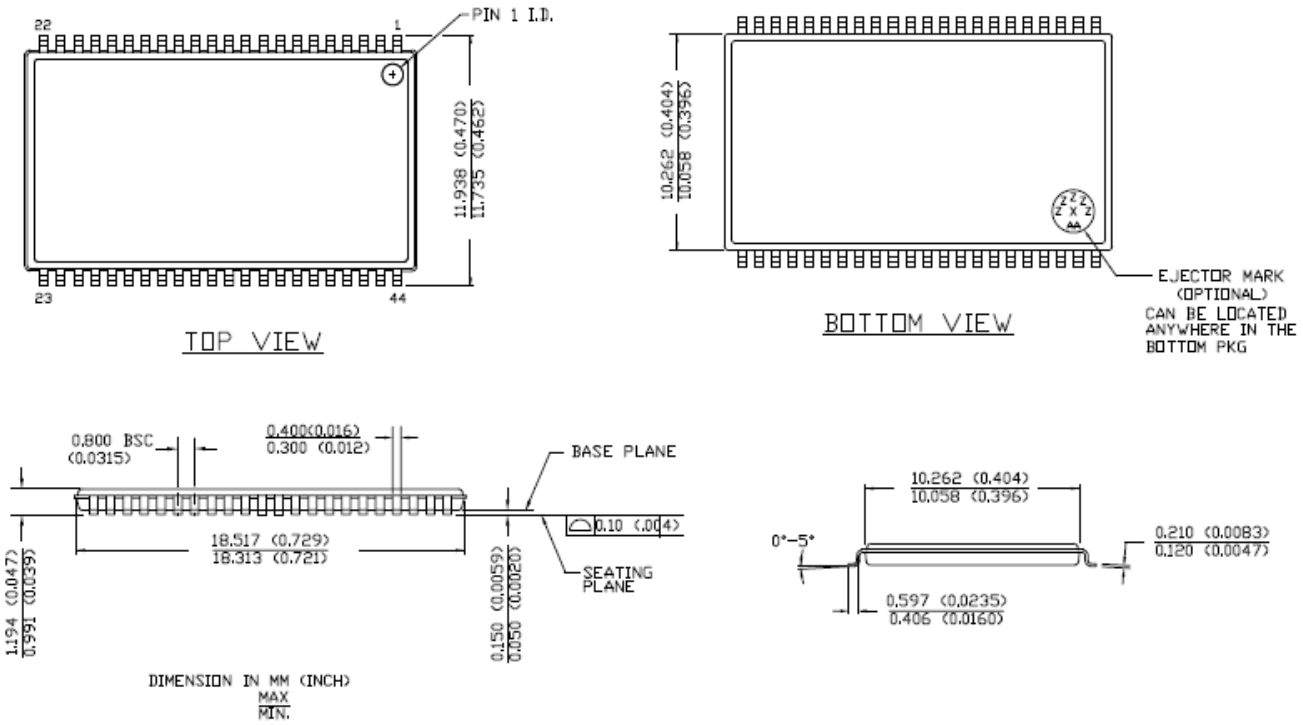
Figure 6. 44-pin (400-Mil) Molded SOJ, 51-85082



51-85082 *C

Package Diagrams(continued)

Figure 7. 44-Pin Thin Small Outline Package Type II, 51-85087



51-85087 *C

Acronyms

Acronym	Description
BGA	ball grid array
CMOS	complementary metal oxide semiconductor
FBGA	very fine ball gird array
I/O	input/output
TSOP	thin small outline package
SRAM	static random access memory
TTL	Transistor transistor logic

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
µA	microamperes
mA	milliampere
MHz	megahertz
ns	nanoseconds
pF	picofarads
V	volts
Ω	ohms
W	watts

Document History Page

Document Title: CY7C1020D, 512K (32K x 16) Static RAM Document #: 38-05463				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	201560	See ECN	SWI	Advance Data sheet for C9 IPP
*A	233695	See ECN	RKF	1) DC parameters modified as per EROS (Spec # 01-0216) 2) Pb-free Offering in the 'Ordering Information'
*B	263769	See ECN	RKF	1) Corrected pin #18 on SOJ/TSOPII Pinout (Page #1) from A_{15} to A_4 2) Changed IO_1 - IO_{16} to IO_0 - IO_{15} on the Pin-out diagram 3) Added T_{power} Spec in Switching Characteristics Table 4) Added Data Retention Characteristics Table and Waveforms 5) Shaded 'Ordering Information'
*C	307594	See ECN	RKF	Reduced Speed bins to –10, –12 and –15 ns
*D	560995	See ECN	VKN	Converted from Preliminary to Final Removed Commercial Operating range Removed 12 ns speed bin Added I_{CC} values for the frequencies 83MHz, 66MHz and 40MHz Updated Thermal Resistance table Updated Ordering Information Table Changed Overshoot spec from V_{CC}+2V to V_{CC}+1V in footnote #3
*E	802877	See ECN	VKN	Changed I_{CC} specs from 60 mA to 80 mA for 100MHz, 55 mA to 72 mA for 83MHz, 45 mA to 58 mA for 66MHz, 30 mA to 37 mA for 40MHz
*F	3109992	12/14/2010	AJU	Added Ordering Code Definitions. Updated Package Diagrams.
*G	3219056	04/07/2011	PRAS	Added TOC Added Acronyms and Units of Measure table. Updated Datasheet as per template.

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