National Semiconductor

PRELIMINARY

DM54AS113/DM74AS113 Dual J-K Negative-Edge-Triggered Flip-Flops with Preset

General Description

The DM54AS113 is a dual-edge-triggered flip-flops. Each flip-flop has individual J, K, clock, and preset inputs, and also complementary Q and $\overline{Q}$ outputs.

Information at input J or K is transferred to the Q output on the negative going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. When the clock input is at either the high or low level, the J, K input signal has no effect.

Asynchronous preset inputs will set Q output upon the application of low level signal.

The JK design allows operation as a toggle flip-flop by tying the J and K inputs high.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and LS TTL Counterpart.
- Improved AC Performance Over S113 at Approximately Half the Power.

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

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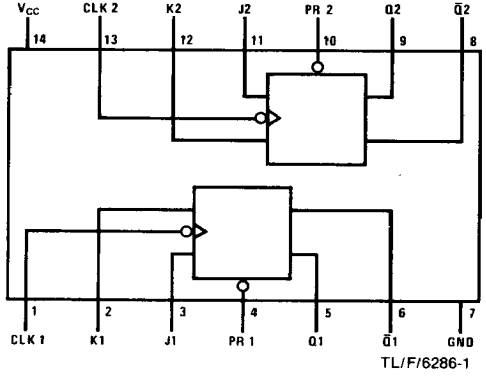
Connection Diagram

Dual-In-Line Package



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54AS113 (J) **74AS113 (J, N)**

Function Table

Inputs				Outputs	
PR	CK	J	K	Q	$\overline{Q}$
L	X	X	X	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	
H	↓	L	L	Q0	$\overline{Q}$0
H	↓	H	L	H	L
H	H	X	X	Q0	$\overline{Q}$0

L = Low State, H = High State, X = Don't Care
↓ = Negative Edge Transition, Q0 = Previous Condition of Q

Recommended Operating Conditions

Parameter		DM54AS113			DM74AS113			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−2			−2	mA
Low Level Output Current, I_{OL}				20			20	mA
Clock Frequency, fCLOCK		0			0			MHz
Pulse Width T_W	Clock High							ns
	Clock Low							ns
Pulse Width T_W, Preset								ns
Data Setup Time, T_{SU}	J or K							ns
	PRE inactive							
Data Hold Time, T_H								ns

The (↓) arrow indicates the negative edge of the Clock is used for reference.

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage		$V_{CC} = 4.5V$, $I_I = -18mA$			−1.2	V
V_{OH}	High Level Output Voltage		$I_{OH} = -2mA$ $V_{CC} = 4.5V$ to $5.5V$	$V_{CC} - 2$			V
V_{OL}	Low Level Output Voltage		$V_{CC} = 4.5V$ $V_{IH} = 2V$ $I_{OL} = 20mA$		0.35	0.5	V
I_I	Max High Input Current		$V_{CC} = 5.5V$, $V_{IH} = 7V$			0.1	mA
I_{IH}	High Level Input Current	Clock, J, K	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$			20	μA
		Preset				40	
I_{IL}	Low Level Input Current	Clock	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$		−5		mA
		J, K			−1		
		Preset			−5.5		
I_O	Output Drive Current	$V_{CC} = 5.5V$	$V_O = 2.25V$	−30		−112	mA
I_{CC}	Supply Current		$V_{CC} = 5.5V$		38		mA

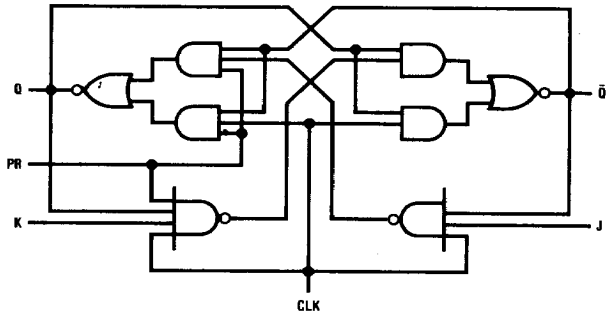
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54AS113			DM74AS113			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF		175			175		MHz
T_{PLH}	Preset	Q or $\overline{Q}$			3			3		ns
T_{PHL}					4			4		ns
T_{PLH}	Clock	Q or $\overline{Q}$			3			3		ns
T_{PHL}					4			4		ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



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