National Semiconductor

CD4512BM/CD4512BC 8-Channel Buffered Data Selector

General Description

The CD4512BM/CD4512BC buffered 8-channel data selector is a complementary MOS (CMOS) circuit constructed with N- and P-channel enhancement mode transistors. This data selector is primarily used as a digital signal multiplexer selecting 1 of 8 inputs and routing the signal to a TRI-STATE® output. A high level at the Inhibit input forces a low level at the output. A high level at the Output Enable ($\overline{OE}$) input forces the output into the TRI-STATE condition. Low levels at both the Inhibit and ($\overline{OE}$) inputs allow normal operation.

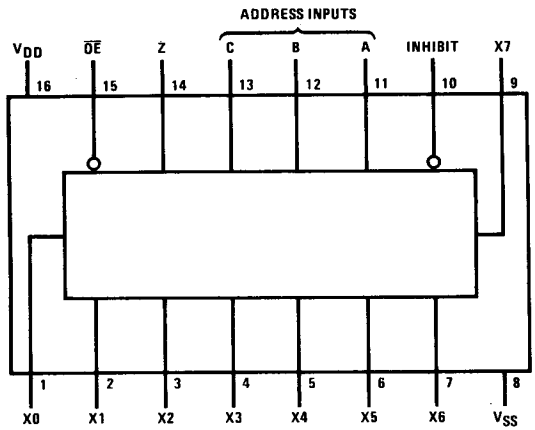
TRI-STATE is a trademark of National Semiconductor Corp.

Features

- Wide supply voltage range 3.0V-15V
- High noise immunity 0.45 V_{DD} (typ.)
- TRI-STATE output
- Low quiescent power dissipation 0.25 μW/package (typ.) @ $V_{CC} = 5.0V$
- Plug-in replacement for Motorola MC14512

Connection Diagram and Truth Table

Dual-In-Line Package



TOP VIEW

ADDRESS INPUTS			CONTROL INPUTS		OUTPUT
C	B	A	INHIBIT	$\overline{OE}$	Z
0	0	0	0	0	X0
0	0	1	0	0	X1
0	1	0	0	0	X2
0	1	1	0	0	X3
1	0	0	0	0	X4
1	0	1	0	0	X5
1	1	0	0	0	X6
1	1	1	0	0	X7
Ø	Ø	Ø	1	0	0
Ø	Ø	Ø	Ø	1	Hi-Z

Ø = Don't care
Hi-Z = TRI-STATE® condition
Xn = Data at input n

Absolute Maximum Ratings
(Notes 1 & 2)

V_{DD} Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} + 0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions
(Note 2)

V_{DD} DC Supply Voltage	3.0 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4512BM	−55°C to +125°C
CD4512BC	−40°C to +85°C

DC Electrical Characteristics CD4512BM (Note 2)

Parameter	Conditions	−55°C		25°C			125°C		Units
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_{DD} Quiescent Device Current	V_{DD} = 5.0 V		5.0		0.005	5.0		150	μA
	V_{DD} = 10 V		10		0.010	10		300	μA
	V_{DD} = 15 V		20		0.015	20		600	μA
V_{OL} Low Level Output Voltage	V_{DD} = 5.0 V		0.05		0	0.05		0.05	V
	V_{DD} = 10 V		0.05		0	0.05		0.05	V
	V_{DD} = 15 V		0.05		0	0.05		0.05	V
V_{OH} High Level Output Voltage	V_{DD} = 5.0 V	4.95		4.95	5.0		4.95		V
	V_{DD} = 10 V	9.95		9.95	10.0		9.95		V
	V_{DD} = 15 V	14.95		14.95	15.0		14.95		V
V_{IL} Low Level Input Voltage	V_{DD} = 5.0 V, V_O = 0.5 V		1.5		2.25	1.5		1.5	V
	V_{DD} = 10 V, V_O = 1.0 V		3.0		4.50	3.0		3.0	V
	V_{DD} = 15 V, V_O = 1.5 V		4.0		6.75	4.0		4.0	V
V_{IH} High Level Input Voltage	V_{DD} = 5.0 V, V_O = 4.5 V	3.5		3.5	2.75		3.5		V
	V_{DD} = 10 V, V_O = 9.0 V	7.0		7.0	5.50		7.0		V
	V_{DD} = 15 V, V_O = 13.5 V	11.0		11.0	8.25		11.0		V
I_{OL} Low Level Output Current	V_{DD} = 5.0 V, V_O = 0.4 V	0.64		0.51	0.78		0.36		mA
	V_{DD} = 10 V, V_O = 0.5 V	1.6		1.3	2.0		0.9		mA
	V_{DD} = 15 V, V_O = 1.5 V	4.2		3.4	7.8		2.4		mA
I_{OH} High Level Output Current	V_{DD} = 5.0 V, V_O = 4.6 V	−0.64		−0.51	−1.7		−0.36		mA
	V_{DD} = 10 V, V_O = 9.5 V	−1.6		−1.3	−1.9		−0.9		mA
	V_{DD} = 15 V, V_O = 13.5 V	−4.2		−3.4	−3.5		−2.4		mA
I_{IN} Input Current	V_{DD} = 15 V, V_{IN} = 0 V		−0.1		-10^{-5}	−0.1		−1.0	μA
	V_{DD} = 15 V, V_{IN} = 15 V		0.1		10^{-}	0.1		1.0	μA
I_{OZ} TRI-STATE® Output Current	V_{DD} = 15V, V_O = 0 V		±0.1		-10^{-5}	±0.1		±3.0	μA
	V_{DD} = 15 V, V_O = 15 V				10^{-5}				μA

DC Electrical Characteristics CD4512BC (Note 2)

Parameter	Conditions	−40°C		25°C			85°C		Units
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_{DD} Quiescent Device Current	V_{DD} = 5.0 V		20		0.005	20		150	μA
	V_{DD} = 10 V		40		0.010	40		300	μA
	V_{DD} = 15 V		80		0.015	80		600	μA
V_{OL} Low Level Output Voltage	V_{DD} = 5.0 V		0.05		0	0.05		0.05	V
	V_{DD} = 10 V		0.05		0	0.05		0.05	V
	V_{DD} = 15 V		0.05		0	0.05		0.05	V
V_{OH} High Level Output Voltage	V_{DD} = 5.0 V	4.95		4.95	5.0		4.95		V
	V_{DD} = 10 V	9.95		9.95	10.0		9.95		V
	V_{DD} = 15 V	14.95		14.95	15.0		14.95		V
V_{IL} Low Level Input Voltage	V_{DD} = 5.0 V, V_O = 0.5 V		1.5		2.25	1.5		1.5	V
	V_{DD} = 10 V, V_O = 1.0 V or 9.0 V		3.0		4.50	3.0		3.0	V
	V_{DD} = 15 V, V_O = 1.5 V or 13.5 V		4.0		6.75	4.0		4.0	V
V_{IH} High Level Input Voltage	V_{DD} = 5.0 V, V_O = 4.5 V	3.5		3.5	2.75		3.5		V
	V_{DD} = 10 V, V_O = 9.0 V	7.0		7.0	5.50		7.0		V
	V_{DD} = 15 V, V_O = 1.5 V or 13.5 V	11.0		11.0	8.25		11.0		V

DC Electrical Characteristics (cont'd) CD4512BC (Note 2)

Parameter	Conditions	−40°C		25°C			85°C		Units
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_{OL} Low Level Output Current	$V_{DD}=5.0V$, $V_O=0.4V$	0.52		0.44	0.78		0.36		mA
	$V_{DD}=10V$, $V_O=0.5V$	1.3		1.1	2.0		0.9		mA
	$V_{DD}=15V$, $V_O=1.5V$	3.6		3.4	7.8		2.4		mA
I_{OH} High Level Output Current	$V_{DD}=5.0V$, $V_O=2.5V$	−0.52		−0.44	−1.7		−0.36		mA
	$V_{DD}=10V$, $V_O=9.5V$	−1.3		−1.1	−0.9		−0.9		mA
	$V_{DD}=15V$, $V_O=113.5V$	−3.6		−3.4	−3.5		−2.4		mA
I_{IN} Input Current	$V_{DD}=15V$, $V_{IN}=0V$		−0.3		-10^{-5}	−0.3		−1.0	μA
	$V_{DD}=15V$, $V_{IN}=15V$		0.3		10^{-5}	0.3		1.0	μA
I_{OZ} TRI-STATE® Output Current	$V_{DD}=15V$, $V_O=0V$ or $15V$		±1.0		$\pm10^{-5}$	±1.0		±7.5	μA

AC Electrical Characteristics $T_A=25°C$, $t_r=t_f=20ns$, $C_L=15pF$

Parameter		Conditions	CD4512BM			CD4512BC			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PHL}	Propagation Delay High-to-Low Level	$V_{DD}=5.0V$		225	500		225	750	ns
		$V_{DD}=10V$		75	175		75	200	ns
		$V_{DD}=15V$		57	130		57	150	ns
t_{PLH}	Propagation Delay Low-to-High Level	$V_{DD}=5.0V$		225	500		225	750	ns
		$V_{DD}=10V$		75	175		75	200	ns
		$V_{DD}=15V$		57	130		57	150	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD}=5.0V$		70	175		70	175	ns
		$V_{DD}=10V$		35	75		35	75	ns
		$V_{DD}=15V$		25	55		25	55	ns
t_{PHZ}, t_{PLZ}	Propagation Delay into TRI-STATE from Logic Level	$V_{DD}=5.0V$		50	125		50	125	ns
		$V_{DD}=10V$		25	75		25	75	ns
		$V_{DD}=15V$		19	60		19	60	ns
t_{PZH}, t_{PZL}	Propagation Delay to Logic Level from TRI-STATE	$V_{DD}=5.0V$		50	125		50	125	ns
		$V_{DD}=10V$		25	75		25	75	ns
		$V_{DD}=15V$		19	60		19	60	ns
C_{IN}	Input Capacitance	(Note 3)		7.5	15		7.5	15	pF
C_{OUT}	TRI-STATE Output Capacitance	(Note 3)		7.5	15		7.5	15	pF
C_{PD}	Power Dissipation Capacity	(Note 4)		150			150		pF

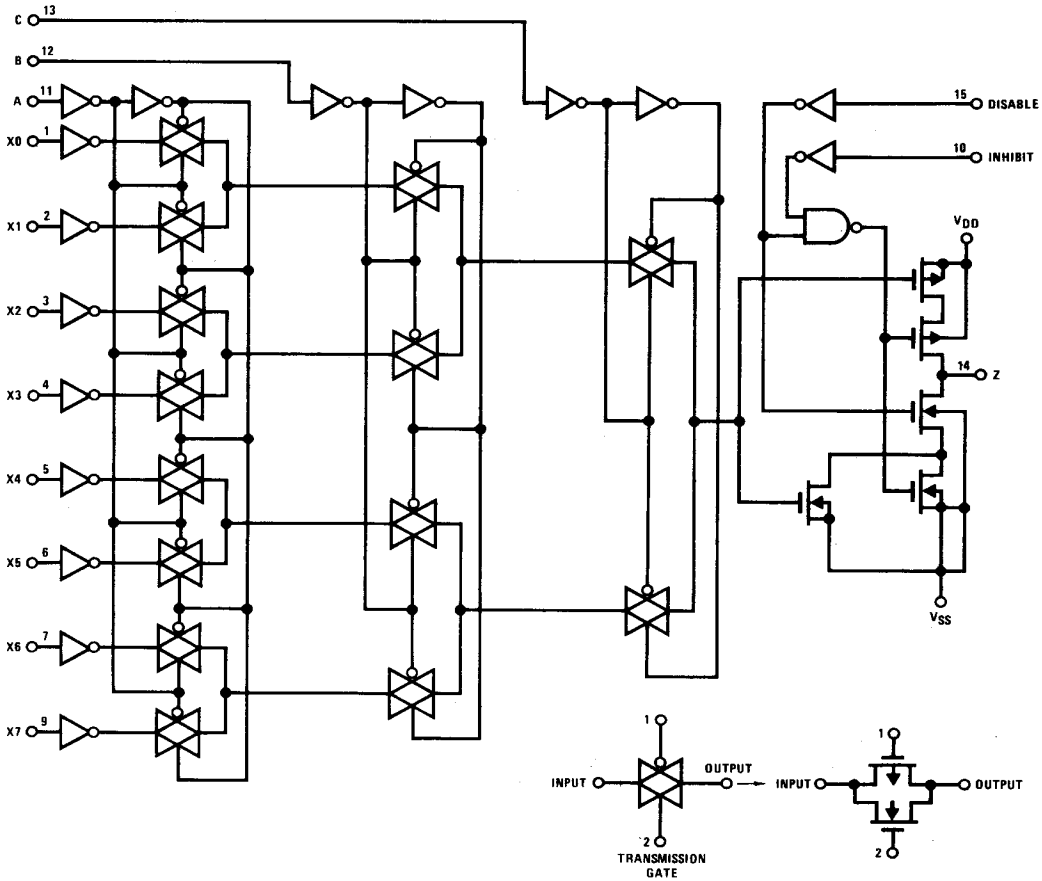
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS}=0V$ unless otherwise specified.

Note 3: Capacitance guaranteed by periodic testing.

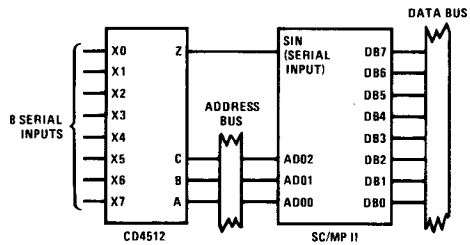
Note 4: C_{PD} determines the no load AC power of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note AN-90.

Logic Diagram

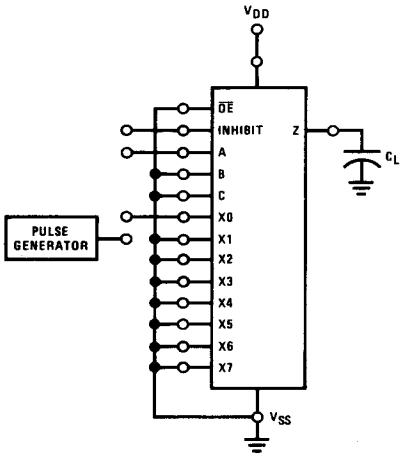


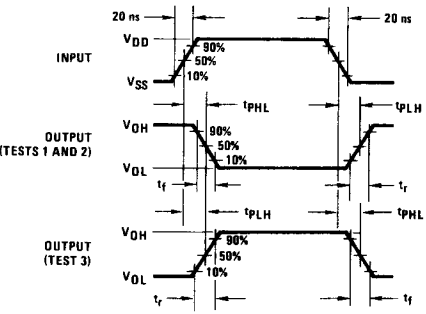
Typical Application

Serial Data Routing Interface



AC Test Circuit and Switching Time Waveforms

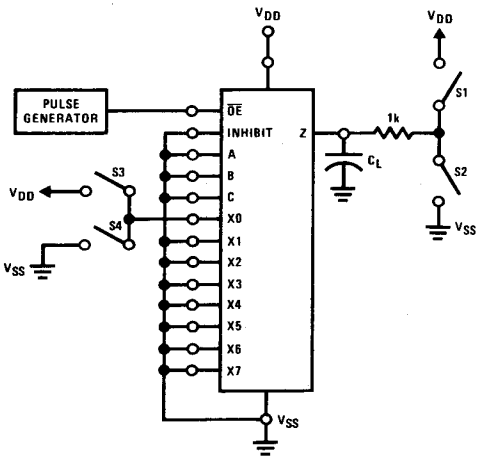


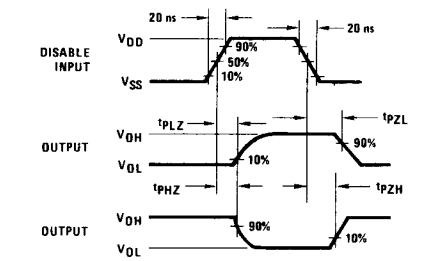


INPUT CONNECTIONS FOR t_r, t_f, t_{PLH}, t_{PHL}

TEST	INHIBIT	A	X0
1	PG	GND	V_{DD}
2	GND	PG	V_{DD}
3	GND	GND	PG

TRI-STATE AC Test Circuit and Switching Time Waveforms





SWITCH POSITIONS FOR TRI-STATE TEST

TEST	S1	S2	S3	S4
t_{PHZ}	Open	Closed	Closed	Open
t_{PLZ}	Closed	Open	Open	Closed
t_{PZL}	Closed	Open	Open	Closed
t_{PZH}	Open	Closed	Closed	Open