To all our customers

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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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Keep safety first in your circuit designs!

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   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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HAT3006R

Silicon N Channel / P Channel Power MOS FET
High Speed Power Switching

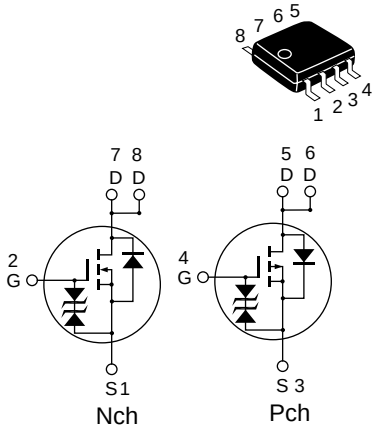
ADE-208-480F (Z)
7th. Edition
Feb. 1999

Features

- Low on-resistance
- Capable of 4 V gate drive
- Low drive current
- High density mounting

Outline

SOP–8



1, 3	Source
2, 4	Gate
5, 6, 7, 8	Drain

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings		Unit
		Nch	Pch	
Drain to source voltage	V_{DSS}	30	– 30	V
Gate to source voltage	V_{GSS}	± 20	± 20	V
Drain current	I_D	6.5	– 4.5	A
Drain peak current	$I_{D(pulse)}$ Note1	52	– 36	A
Body-drain diode reverse drain current	I_{DR}	6.5	– 4.5	A
Channel dissipation	Pch Note2	2		W
Channel dissipation	Pch Note3	3		W
Channel temperature	Tch	150		°C
Storage temperature	Tstg	– 55 to + 150		°C

Note: 1. PW ≤ 10µs, duty cycle ≤ 1 %
2. 1 Drive operation : When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW≤ 10s
3. 2 Drive operation : When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW≤ 10s

Electrical Characteristics (N channel) (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	I_G = ± 100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	± 10	µA	V_{GS} = ± 16 V, V_{DS} = 0
Zero gate voltege drain current	I_{DSS}	—	—	10	µA	V_{DS} = 30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	0.03	0.045	Ω	I_D = 4 A, V_{GS} = 10 V Note4
	$R_{DS(on)}$	—	0.05	0.08	Ω	I_D = 4 A, V_{GS} = 4 V Note4
Forward transfer admittance	$\|y_{fs}\|$	5	8	—	S	I_D = 4 A, V_{DS} = 10 V Note4
Input capacitance	Ciss	—	560	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	380	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	170	—	pF	f = 1MHz
Turn-on delay time	$t_{d(on)}$	—	30	—	ns	V_{GS} = 4 V, I_D = 4 A
Rise time	t_r	—	270	—	ns	V_{DD} ≅ 10 V
Turn-off delay time	$t_{d(off)}$	—	40	—	ns	
Fall time	t_f	—	65	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.9	1.4	V	IF = 6.5 A, V_{GS} = 0 Note4
Body–drain diode reverse recovery time	t_{rr}	—	45	—	ns	IF = 6.5 A, V_{GS} = 0 diF/ dt = 20 A/µs

Note: 4. Pulse test

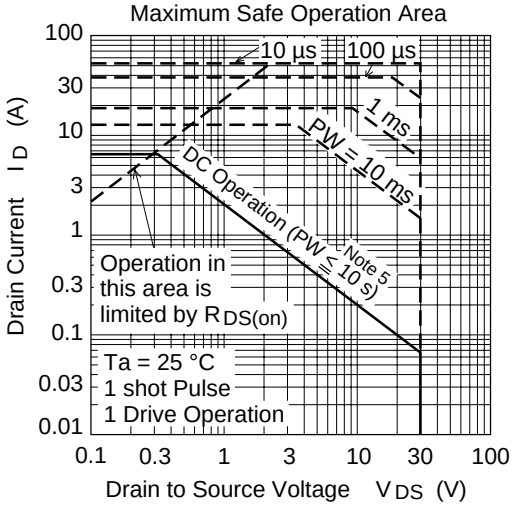
Electrical Characteristics (P channel) (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	– 30	—	—	V	I_D = – 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	I_G = ± 100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	± 10	µA	V_{GS} = ± 16 V, V_{DS} = 0
Zero gate voltege drain current	I_{DSS}	—	—	– 10	µA	V_{DS} = – 30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	– 1.0	—	– 2.5	V	V_{DS} = –10 V, I_D = –1mA
Static drain to source on state resistance	$R_{DS(on)}$	—	0.07	0.09	Ω	I_D = – 3 A, V_{GS} = –10V Note5
	$R_{DS(on)}$	—	0.11	0.18	Ω	I_D = – 3 A, V_{GS} = –4V Note5
Forward transfer admittance	$\|y_{fs}\|$	4	6	—	S	I_D = – 3 A, V_{DS} = –10V Note5
Input capacitance	Ciss	—	660	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	440	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	140	—	pF	f = 1MHz
Turn-on delay time	$t_{d(on)}$	—	24	—	ns	V_{GS} = – 4 V, I_D = – 3 A
Rise time	t_r	—	165	—	ns	V_{DD} ≅ –10 V
Turn-off delay time	$t_{d(off)}$	—	35	—	ns	
Fall time	t_f	—	70	—	ns	
Body–drain diode forward voltage	V_{DF}	—	– 0.9	– 1.4	V	IF = – 4.5 A, V_{GS} = 0 Note5
Body–drain diode reverse recovery time	t_{rr}	—	60	—	ns	IF = –4.5 A, V_{GS} = 0 diF/ dt = 20A/µs

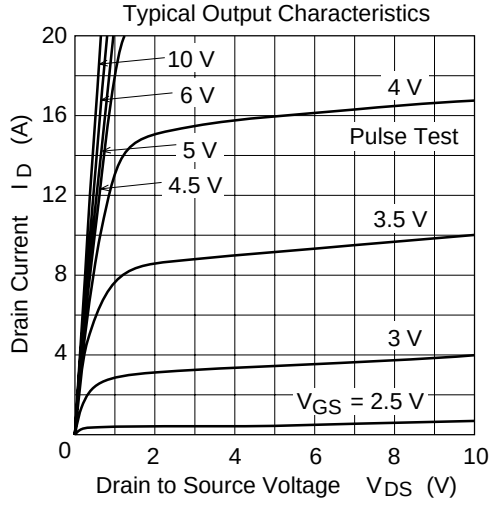
Note: 5. Pulse test

Main Characteristics (N channel)

Maximum Safe Operation Area

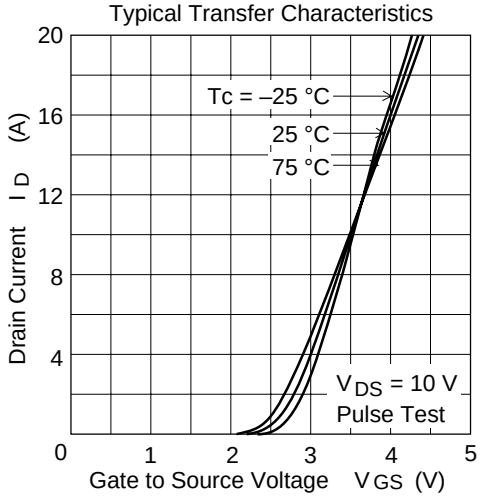


Typical Output Characteristics

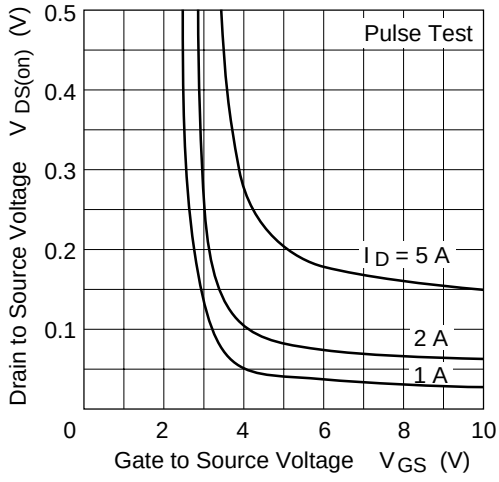


Note 5 :
When using the glass epoxy board
(FR4 40x40x1.6 mm)

Typical Transfer Characteristics

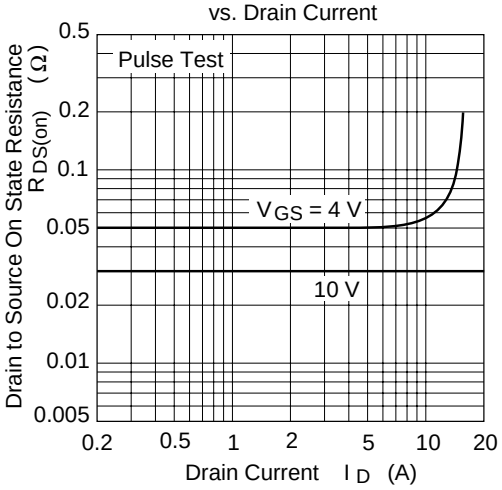


Drain to Source Saturation Voltage vs.
Gate to Source Voltage

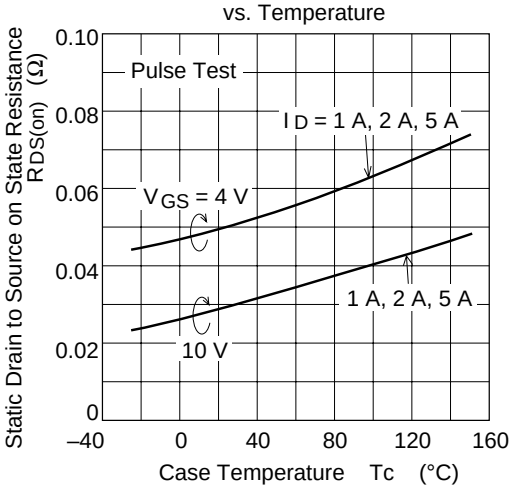


Main Characteristics (N channel)

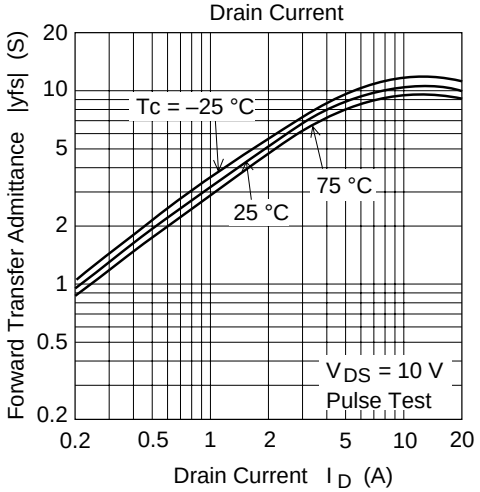
Static Drain to Source on State Resistance vs. Drain Current



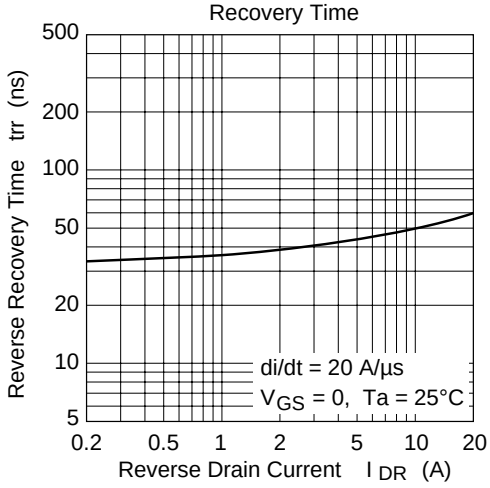
Static Drain to Source on State Resistance vs. Temperature



Forward Transfer Admittance vs. Drain Current

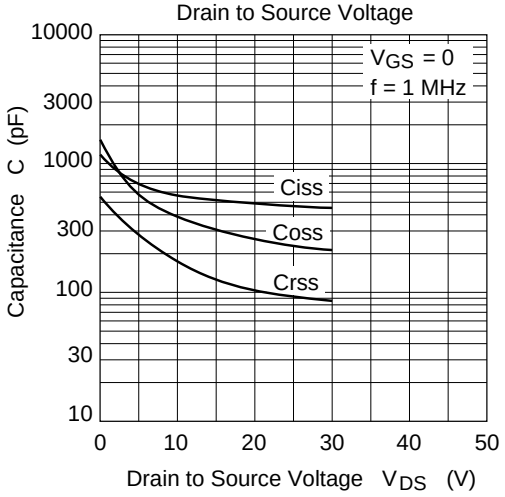


Body–Drain Diode Reverse Recovery Time

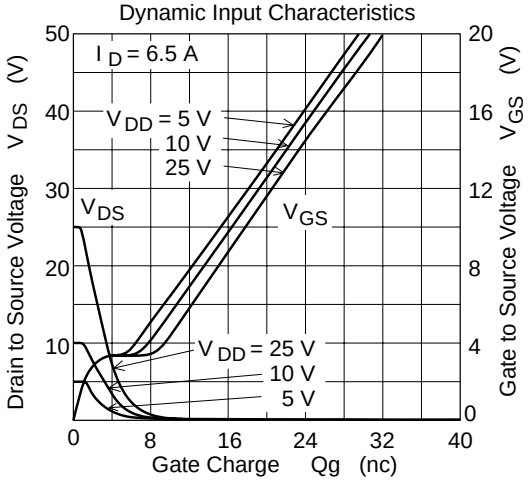


Main Characteristics (N channel)

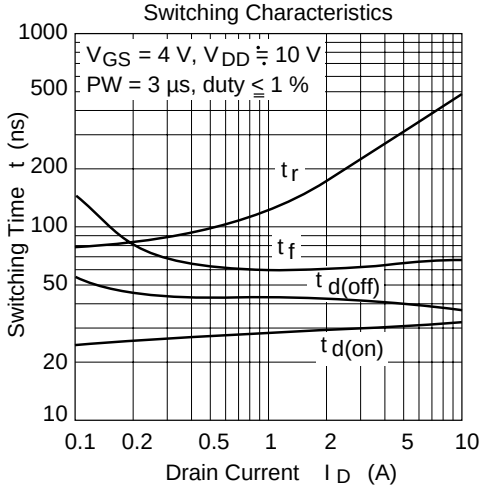
Typical Capacitance vs.
Drain to Source Voltage



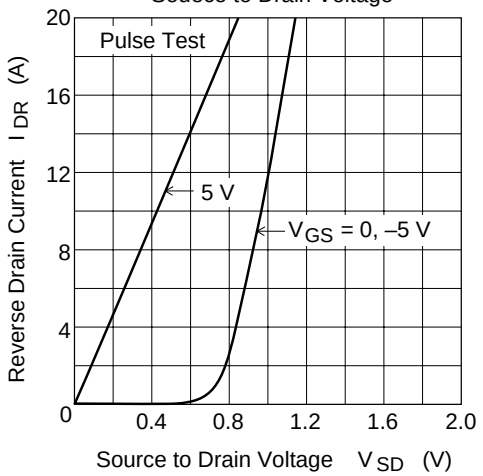
Dynamic Input Characteristics



Switching Characteristics

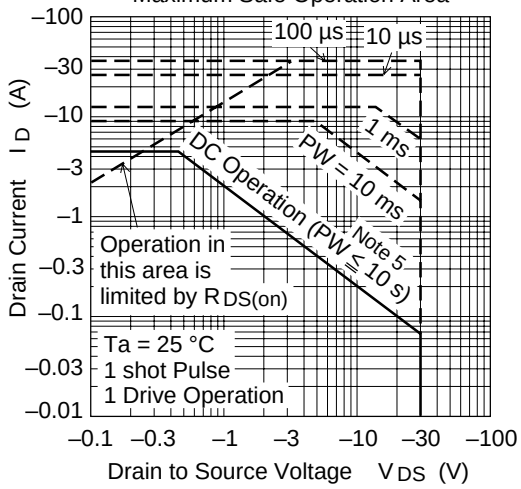


Reverse Drain Current vs.
Souece to Drain Voltage



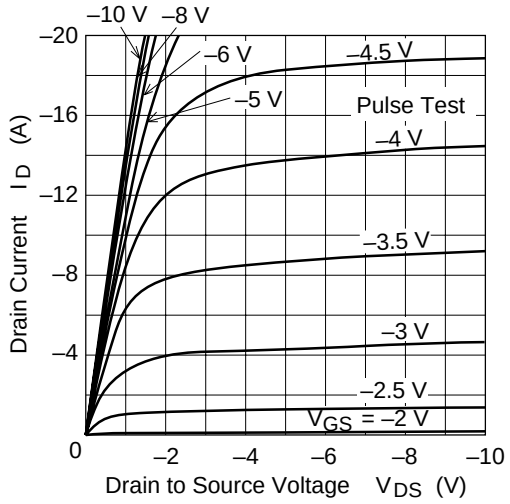
Main Characteristics (P channel)

Maximum Safe Operation Area

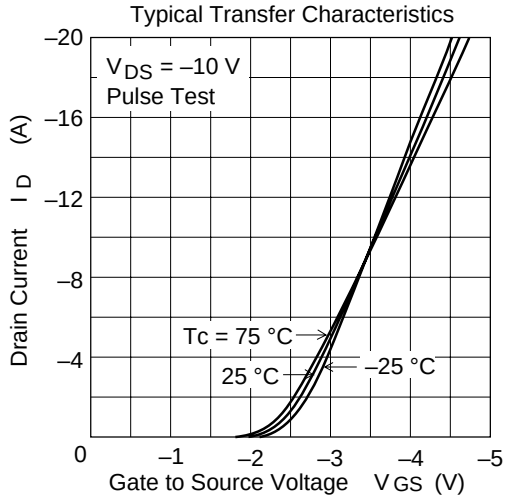


Note 5 :
When using the glass epoxy board
(FR4 40 x 40 x 1.6 mm)

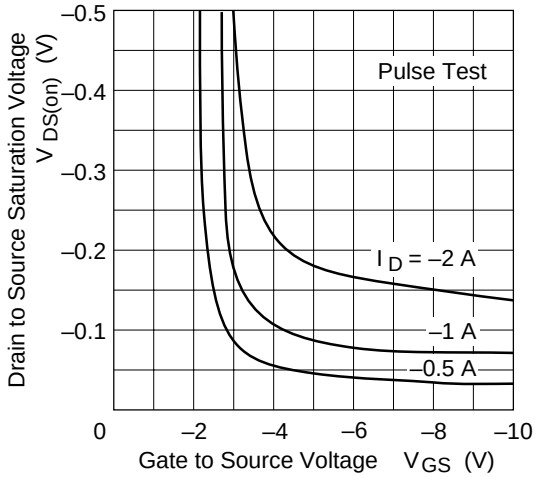
Typical Output Characteristics



Typical Transfer Characteristics

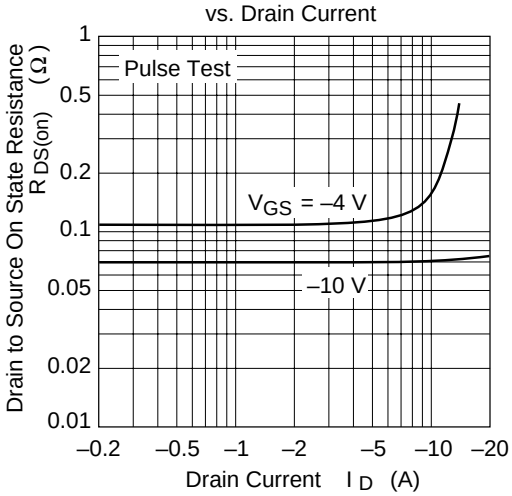


Drain to Source Saturation Voltage vs.
Gate to Source Voltage

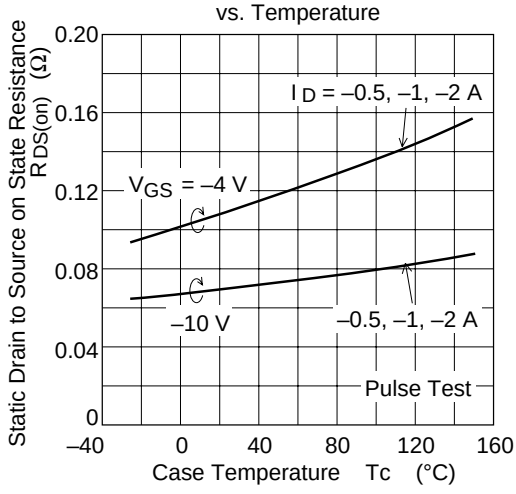


Main Characteristics (P channel)

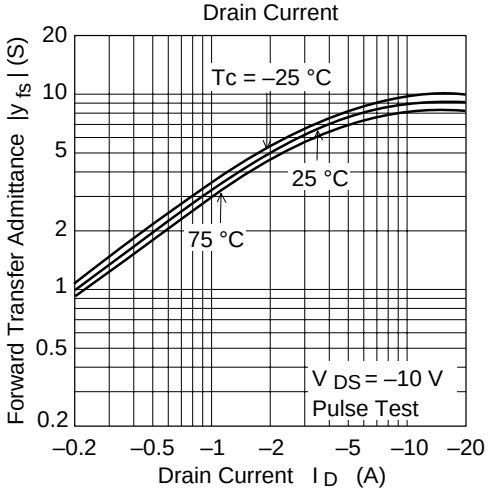
Static Drain to Source on State Resistance vs. Drain Current



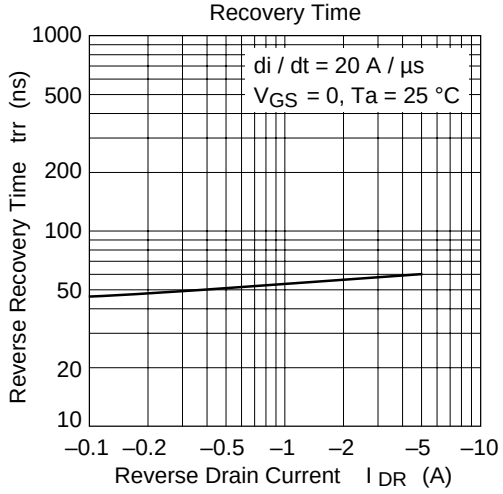
Static Drain to Source on State Resistance vs. Temperature



Forward Transfer Admittance vs. Drain Current

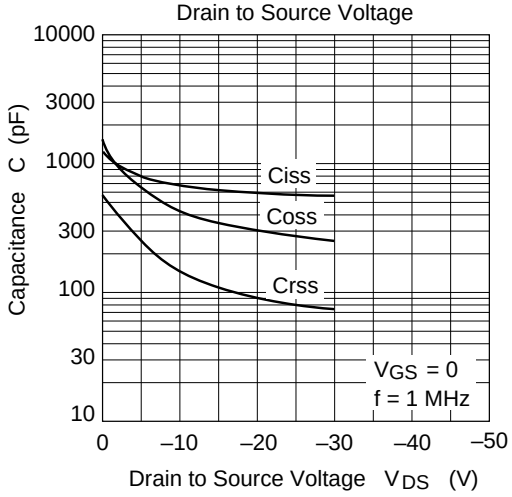


Body–Drain Diode Reverse Recovery Time

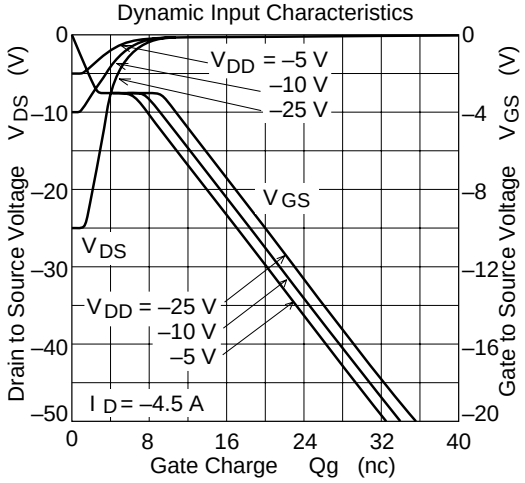


Main Characteristics (P channel)

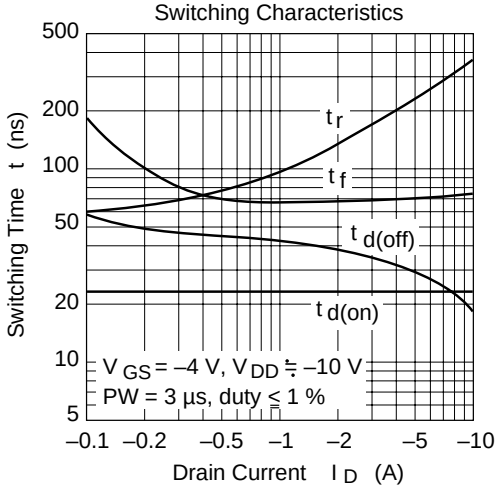
Typical Capacitance vs.
Drain to Source Voltage



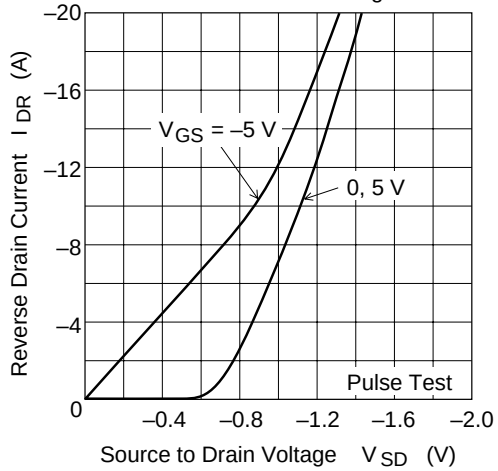
Dynamic Input Characteristics

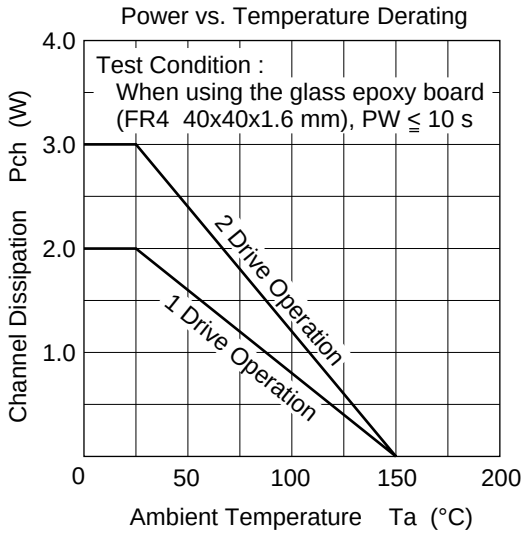


Switching Characteristics

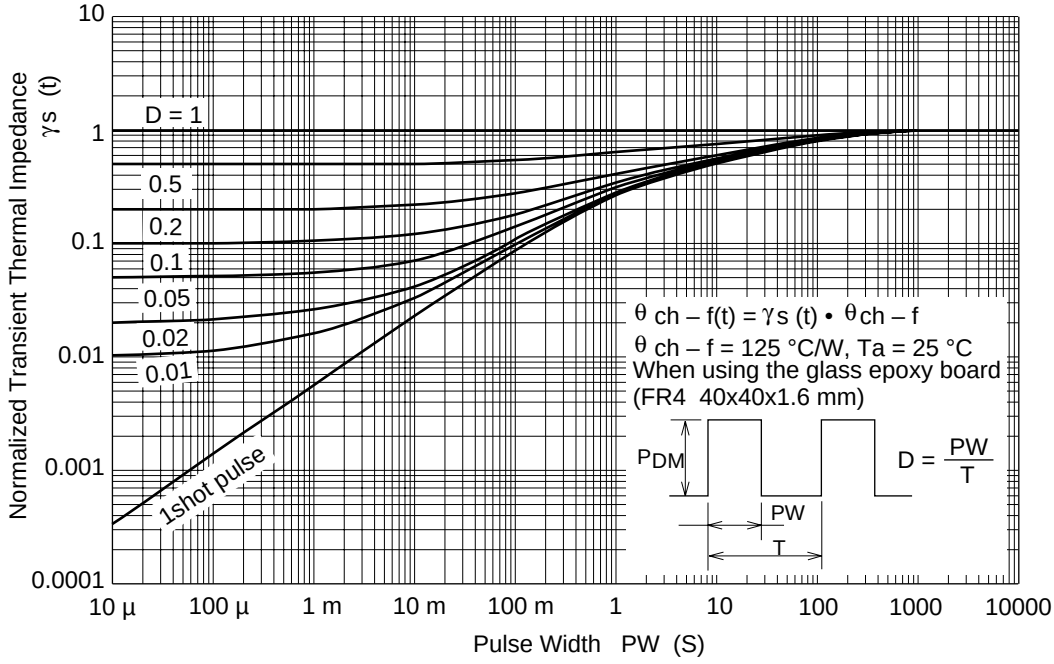


Reverse Drain Current vs.
Source to Drain Voltage

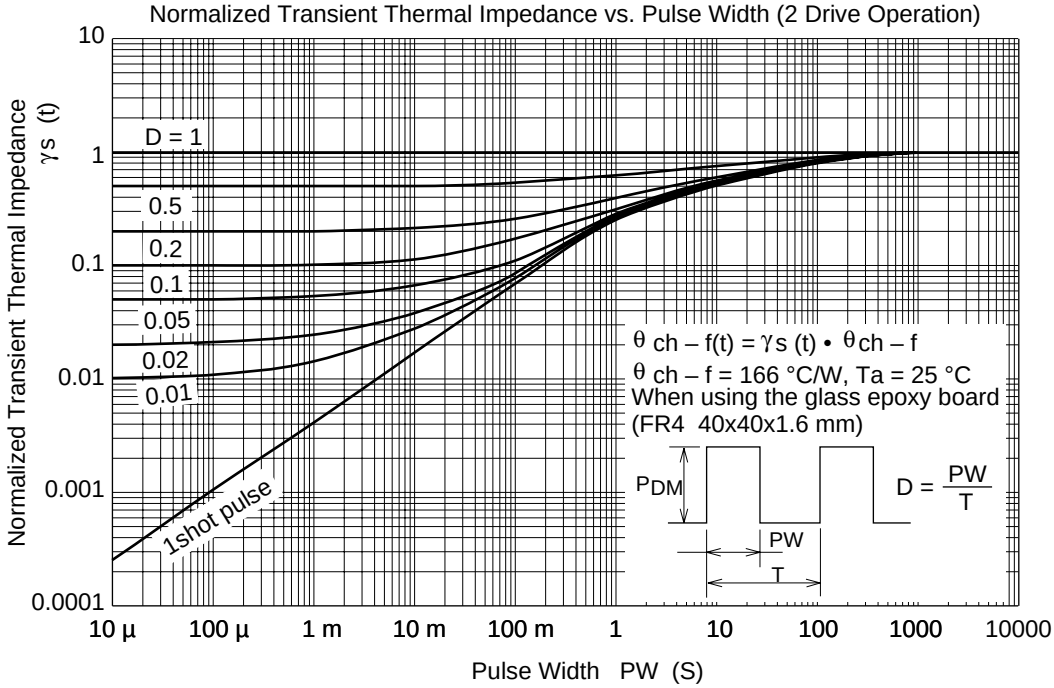



Power vs. Temperature Derating
Test Condition :
When using the glass epoxy board
(FR4 40x40x1.6 mm), PW ≦ 10 s
Channel Dissipation Pch (W)
4.0
3.0
2.0
1.0
0
50
100
150
200
2 Drive Operation
1 Drive Operation
Ambient Temperature Ta (°C)

Normalized Transient Thermal Impedance vs. Pulse Width (1 Drive Operation)

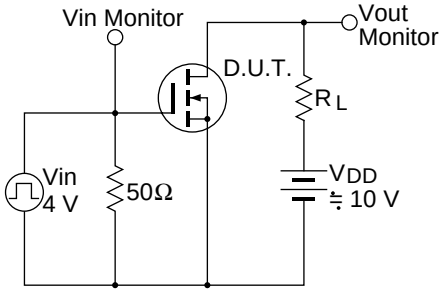


Normalized Transient Thermal Impedance vs. Pulse Width (2 Drive Operation)

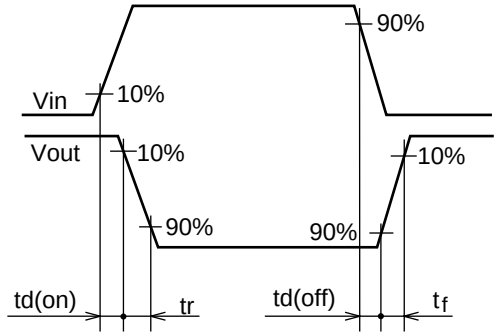


N channel

Switching Time Test Circuit

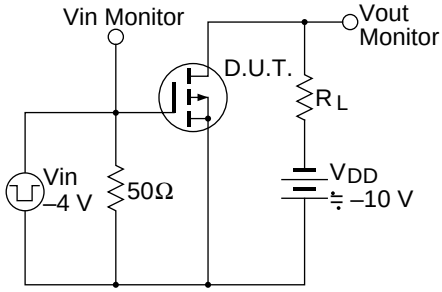


Switching Time Waveform

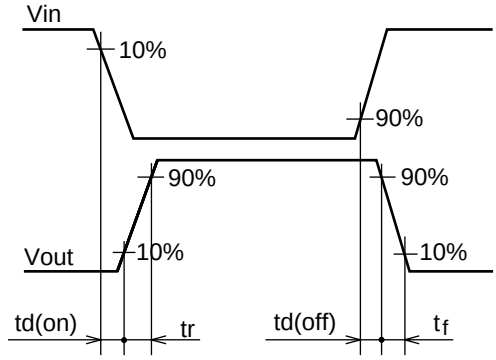


P channel

Switching Time Test Circuit



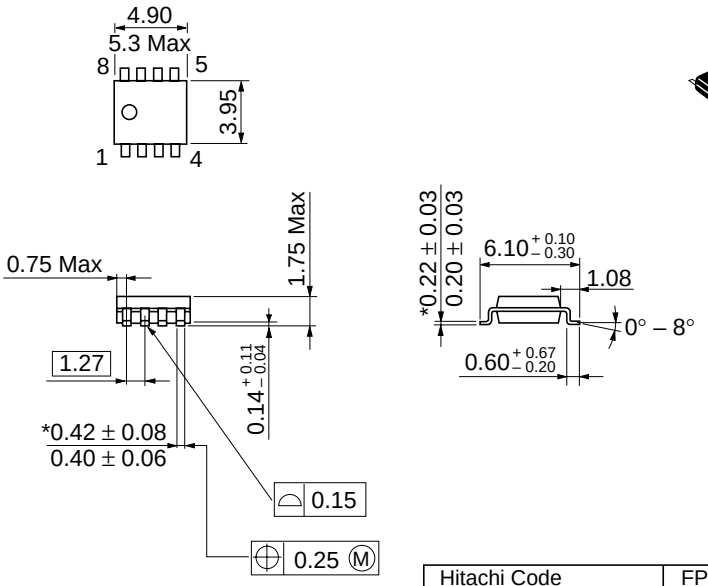
Switching Time Waveform



Package Dimensions

As of January, 2001

Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-8DA
JEDEC	Conforms
EIAJ	—
Mass (reference value)	0.085 g

Cautions

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Hitachi, Ltd.
Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

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For further information write to:

Hitachi Semiconductor (America) Inc.
179 East Tasman Drive,
San Jose,CA 95134
Tel: <1> (408) 433-1990
Fax: <1>(408) 433-0223

Hitachi Europe GmbH
Electronic Components Group
Dornacher Straβe 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 585160

Hitachi Asia Ltd.
Hitachi Tower
16 Collyer Quay #20-00,
Singapore 049318
Tel : <65>-538-6533/538-8577
Fax : <65>-538-6933/538-3877
URL : http://www.hitachi.com.sg

Hitachi Asia Ltd.
(Taipei Branch Office)
4/F, No. 167, Tun Hwa North Road,
Hung-Kuo Building,
Taipei (105), Taiwan
Tel : <886>-(2)-2718-3666
Fax : <886>-(2)-2718-8180
Telex : 23222 HAS-TP
URL : http://www.hitachi.com.tw

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower,
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon,
Hong Kong
Tel : <852>-(2)-735-9218
Fax : <852>-(2)-730-0281
URL : http://www.hitachi.com.hk

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