REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
C	Convert to military drawing format. Add an LCC package. Editorial changes throughout.	27 JAN 88	M.A. Frye

CURRENT CAGE CODE 67268

REV	C	C	C	C	C	C	C	C	C	C	C															
PAGE	24	25	26	27	28	29	30	31	32	33	34															

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Defense Electronics Supply Center
Dayton, Ohio

Original date of drawing:
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SIZE: A

CODE IDENT. NO.: 14933

REV: C

MILITARY DRAWING

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TITLE: MICROCIRCUITS, MICROPROCESSOR PERIPHERAL COUNTER/TIMER, PARALLEL INPUT/OUTPUT N-CHANNEL, MONOLITHIC SILICON

DWG NO. 83001

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5962-E709

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DESC FORM 193
MAY 86

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

83001	01	Q	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Frequency	Circuit
01	Z8536/Z0853604	4 MHz	Counter timer and parallel input/output peripheral unit
02	Z8536A/Z0853606	6 MHz	Counter timer and parallel input/output peripheral unit

1.2.2 Case outlines. The case outlines shall be as follows:

Outline letter	Case outline
Q	D-5 (40-lead, 9/16" x 2 1/16"), dual-in-line package
Y	C-5 (44-terminal, .650" x .650"), square chip carrier package

1.3 Absolute maximum ratings.

Supply voltage range (referenced to ground)	-0.3 V dc to +7.0 V dc
Voltage on any pin (referenced to ground)	-0.3 V dc to V_{CC} +0.3 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation at -55°C	1.2 W
Maximum power dissipation at +125°C	0.60 W
Lead temperature (soldering, 10 seconds)	+270°C
Maximum junction temperature (T_J) at T_C = +125°C	+170°C
Thermal resistance, junction to case (θ_{JC}):	
Cases Q and Y	(See MIL-M-38510, appendix C)

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
Minimum high level input voltage (V_{IH})	2.4 V dc
Maximum low level input voltage (V_{IL})	0.8 V dc
Frequency of operation:	
Device type 01	0.5 to 4.0 MHz
Device type 02	0.5 to 6.0 MHz
Case operating temperature range (T_C)	-55°C to +125°C
Clock rise time	20 ns maximum
Clock fall time	20 ns maximum

1.4 Recommended operating conditions - Continued.

Parameter	Reference number 1/	Minimum	Maximum	Unit
Trigger input to PCLK setup time (timer mode) 2/	71	150		ns
Trigger input to counter input setup time (counter mode) 2/	72	150		ns
Trigger input pulse width (high or low)	73	200		ns
Gate input to PCLK setup time (timer mode) 2/	74	100		ns
Gate input to counter input setup time (counter mode) 2/	75	100		ns
Gate input to PCLK hold time (timer mode) 2/	76	100		ns
Gate input to counter input hold time (counter mode) 2/	77	100		ns
PCLK to counter output delay (timer mode)	78		475	ns
Counter input to counter output delay (counter mode)	79		475	ns

1/ The reference number refers to identified parameter on figure 3 for device type 01 only.

2/ These parameters must be met to guarantee trigger or gate are valid for the next counter/ timer cycle.

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Logic functions. The logic functions shall be as specified on figure 2.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.5 herein.

TABLE I. Electrical performance characteristics.

Parameter	Symbol	Conditions $-55°C \le T_C \le +125°C$, unless otherwise specified $4.5\ V \le V_{CC} \le 5.5\ V$	Device type	Group A subgroups	Limits Min	Limits Max	Unit
Input high voltage	V_{IH}		All	1, 2, 3	2.2	V_{CC} +0.3 1/	V
Input low voltage	V_{IL}				-0.3 1/	0.8	V
Output low voltage	V_{OL}	I_{OL} = 2.0 mA				0.4	V
Output high voltage	V_{OH}	I_{OH} = -250 µA			2.4		V
Power supply current	I_{CC}	Outputs open V_{CC} = 5.5 V				200	mA
Input capacitance	C_{IN}		01,02	4		10 1/	pF
Output capacitance	C_{OUT}		01,02	4		15 1/	pF
Bidirectional capacitance	$C_{I/O}$		01,02	4		20 1/	pF
Output leakage current low, open drain outputs	I_{LOL}	$0.4\ V \le V_{OUT} \le +2.4\ V$	All	1, 2, 3	-10	+10	µA
Output leakage current high, open drain outputs	I_{LOH}				-10	+10	µA
Input low current (input and bi-directional)	I_{IL}	$0.4\ V \le V_{IN} \le 2.4\ V$			-10	+10	µA
Input high current (input and bi-directional)	I_{IH}				-10	+10	µA
Maximum frequency 1/	f_{MAX}		01 02	9, 10, 11	4.0 6.0		MHz
Functional tests		See 4.3.1c		7, 8			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Parameter	Symbol	Conditions T_C = -55°C to +125°C, V_{CC} = 4.5 to 5.5 V, See figure 3, C_L = 50 pF ±10%			Minimum	Maximum	Unit
		Reference 2/ number	Device type	Group A subgroups			
PCLK cycle time	t_{CYC1}	1	01 02	9,10,11	250 165	4000 4000	ns
PCLK width high 1/	t_{PWH1}	2	01 02	9,10,11	105 70	2000 2000	ns
PCLK width low 1/	t_{PWL1}	3	01 02	9,10,11	105 70	2000 2000	ns
PCLK rise time 1/	t_{RC1}	4	01 02	9,10,11		20 10	ns
PCLK fall time 1/	t_{FC1}	5	01 02	9,10,11		20 15	ns
$\overline{INTACK}$ to PCLK setup time 1/	t_{SHL1} t_{SLH1}	6	All	9,10,11	100		ns
$\overline{INTACK}$ to PCLK hold time 1/	t_{HHL1} t_{HLH1}	7	All	9,10,11	0		ns
$\overline{INTACK}$ to $\overline{RD}$ setup time 1/	t_{SHL2} t_{SLH2}	8	All	9,10,11	200		ns
$\overline{INTACK}$ to $\overline{RD}$ hold time 1/	t_{HHL2} t_{HLH2}	9	All	9,10,11	0		ns
$\overline{INTACK}$ to $\overline{WR}$ setup time 1/	t_{SHL3} t_{SLH3}	10	All	9,10,11	200		ns
$\overline{INTACK}$ to $\overline{WR}$ ↑ hold time 1/	t_{HHL3} t_{HLH3}	11	All	9,10,11	0		ns
Address to $\overline{RD}$ ↓ setup time	t_{SHL4} t_{SLH4}	12	All	9,10,11	80		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Parameter	Symbol	Conditions T_C = -55°C to +125°C, V_{CC} = 4.5 to 5.5 V, See figure 3, C_L = 50 pF ±10%			Minimum	Maximum	Unit
		Reference 2/ number	Device type	Group A subgroups			
Address to $\overline{RD}$ ↑ hold time 1/	t_{HHL4} t_{HLH4}	13	All	9,10,11	0		ns
Address to $\overline{WR}$ ↑ setup time	t_{SHL5} t_{SLH5}	14	All	9,10,11	80		ns
Address to $\overline{WR}$ ↑ hold time 1/	t_{HHL5} t_{HLH5}	15	All	9,10,11	0		ns
$\overline{CE}$ low to $\overline{RD}$ ↓ setup time 3/	t_{SHL6}	16	All	9,10,11	0		ns
$\overline{CE}$ high to $\overline{RD}$ ↓ setup time 1/ 3/	t_{SLH7}	17	01 02	9,10,11	100 70		ns
$\overline{CE}$ to $\overline{RD}$ ↑ hold time 3/	t_{HHL6} t_{HLH6}	18	All	9,10,11	0		ns
$\overline{CE}$ low to $\overline{WR}$ ↓ setup time	t_{SHL8}	19	All	9,10,11	0		ns
$\overline{CE}$ high to $\overline{WR}$ ↓ setup time 1/	t_{SLH9}	20	01 02	9,10,11	100 70		ns
$\overline{CE}$ to $\overline{WR}$ ↑ hold time	t_{HHL7} t_{HLH7}	21	All	9,10,11	0		ns
$\overline{RD}$ to low width 1/ 3/	t_{PWL2}	22	01 02	9,10,11	390 250		ns
$\overline{RD}$ ↓ to read data active delay 1/	t_{PHL1} t_{PLH1}	23	All	9,10,11	0		ns
$\overline{RD}$ ↓ to read data valid delay 1/	t_{PHL2} t_{PLH2}	24	01 02	9,10,11		255 180	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Parameter	Symbol	Conditions T_C = -55°C to +125°C, V_{CC} = 4.5 to 5.5 V, See figure 3, C_L = 50 pF ±10%			Minimum	Maximum	Unit
		Reference 2/ number	Device type	Group A subgroups			
$\overline{RD}$ ↑ to read data not valid delay	t_{PHL3} t_{PLH3}	25	All	9,10,11	0		ns
$\overline{RD}$ ↑ to read data float delay 4/	t_{PHZ1} t_{PZH1}	26	01 02	9,10,11		70 45	ns
$\overline{WR}$ low width 1/	t_{PWL3}	27	01 02	9,10,11	390 250		ns
Write data to $\overline{WR}$ ↑ setup time 1/	t_{SHL10} t_{SLH10}	28	All	9,10,11	0		ns
Write data to $\overline{WR}$ ↑ hold time 1/	t_{HHL8} t_{HLH8}	29	All	9,10,11	0		ns
Valid access recovery time 1/ 5/	t_{CYC2}	30	01 02	9,10,11	1000 650		ns
Pattern match to $\overline{INT}$ delay (bit port) 1/	t_{PHL4}	31	All	9,10,11		2* (t_{CYC1}) +800	ns
$\overline{ACKIN}$ to $\overline{INT}$ delay (port with handshake) 1/ 6/	t_{PHL5}	32	All	9,10,11		10* (t_{CYC1}) +600	ns
Counter input to $\overline{INT}$ delay (counter mode) 1/	t_{PHL6}	33	All	9,10,11		2* (t_{CYC1}) +700	ns
PCLK to $\overline{INT}$ delay (timer mode) 1/	t_{PHL7}	34	All	9,10,11		3* (t_{CYC1}) +700	ns
$\overline{INTACK}$ to $\overline{RD}$ ↓ (acknowledge) setup time 1/ 7/	t_{SHL11} t_{SLH11}	35	01 02	9,10,11	350 250		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Parameter	Symbol	Conditions t_C = -55°C to +125°C, V_{CC} = 4.5 to 5.5 V, See figure 3, C_L = 50 pF ±10%			Minimum	Maximum	Unit
		Reference 2/ number	Device type	Group A subgroups			
$\overline{RD}$ acknowledge width 1/	t_{PWL4}	36	01 02	9,10,11	350 250		ns
$\overline{RD}$ ↓ (acknowledge) to read data valid delay 1/	t_{PHL8} t_{PLH8}	37	01 02	9,10,11		250 180	ns
$\overline{INTACK}$ ↓ to 1/ 7/ IEO ↓ delay	t_{PHL9}	38	01 02	9,10,11		350 250	ns
IEI to IEO delay 1/ 7/	t_{PHL10}	39	01 02	9,10,11		150 100	ns
IEI to $\overline{RD}$ ↓ (acknowledge) setup time 1/ 7/	t_{SHL12} t_{SLH12}	40	01 02	9,10,11	100 70		ns
IEI to $\overline{RD}$ ↑ (acknowledge) hold time 1/	t_{HHL9} t_{HLH9}	41	01 02	9,10,11	100 70		ns
$\overline{RD}$ ↓ (acknowledge) to $\overline{INT}$ ↑ delay 1/	t_{PHL11}	42	All	9,10,11		600	ns
Data input to $\overline{ACKIN}$ ↓ setup time 1/	t_{SHL13} t_{SLH13}	43	All	9,10,11	0		ns
$\overline{ACKIN}$ ↓ to RFD ↑ delay 1/	t_{PHL12}	45	All	9,10,11	0		ns
$\overline{RFD}$ ↑ to ACKIN ↓ delay 1/	t_{HHL10}	48	All	9,10,11	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Parameter	Symbol	Conditions t_C = -55°C to +125°C, V_{CC} = 4.5 to 5.5 V, See figure 3, C_L = 50 pF ±10%			Minimum	Maximum	Unit
		Reference 2/ number	Device type	Group A subgroups			
Data out to $\overline{DAV}$ ↑ setup time 1/ 8/	t_{PHL13} t_{PLH13}	49	01 02	9,10,11	25 20		ns
$\overline{DAV}$ ↓ to $\overline{ACKIN}$ ↓ delay 1/	t_{SHL14}	50	All	9,10,11	0		ns
Data out to $\overline{ACKIN}$ ↓ hold time 1/	t_{HHL11} t_{HLH11}	51	All	9,10,11	2*(t_{CYC1})		ns
$\overline{ACKIN}$ ↓ to $\overline{DAV}$ ↑ delay 1/	t_{PLH14}	52	All	9,10,11	2*(t_{CYC1})		ns
RFD ↓ to ACKIN ↑ delay (interlocked handshake) 1/	t_{HLH12}	54	All	9,10,11	0		ns
$\overline{ACKIN}$ ↓ ($\overline{DAV}$) ↓ to RFD ↑ delay (interlocked and three wire handshake) 1/	t_{PLH15}	55	All	9,10,11	0		ns
$\overline{DAV}$ ↓ $\overline{ACKIN}$ ↓ ($\overline{RFD}$) ↓ (interlocked and three wire handshake) 1/	t_{HLH13}	56	All	9,10,11	0		ns
$\overline{ACKIN}$ ↓ ($\overline{RFD}$) ↓ to $\overline{DAV}$ ↓ delay (interlocked and three wire handshake) 1/	t_{PLH16}	57	All	9,10,11	0		ns
$\overline{DAV}$ ↓ to DAC ↑ delay (input three wire handshake) 1/	t_{PLH17}	58	All	9,10,11	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Parameter	Symbol	Conditions t_C = -55°C to +125°C, V_{CC} = 4.5 to 5.5 V, See figure 3, C_L = 50 pF ±10%			Minimum	Maximum	Unit
		Reference 2/ number	Device type	Group A subgroups			
Data input to DAC ↑ hold time (three wire handshake) 1/	t_{HHL14} t_{HLH14}	59	All	9,10,11	0		ns
DAC ↑ to $\overline{DAV}$ ↓ delay (input three wire handshake) 1/	t_{HLH15}	60	All	9,10,11	0		ns
$\overline{DAV}$ ↑ to DAC ↓ delay (input three wire handshake) 1/	t_{PHL18}	61	All	9,10,11	0		ns
$\overline{DAV}$ ↓ to DAC ↑ delay (output three wire handshake) 1/	t_{SLH15}	62	All	9,10,11	0		ns
Data output to DAC ↑ hold time (three wire handshake) 1/	t_{PHL19} t_{PLH19}	63	All	9,10,11	$2*(t_{CYC1})$		ns
DAC ↑ to $\overline{DAV}$ ↑ delay (output three wire handshake) 1/	t_{PHL20}	64	All	9,10,11	$2*(t_{CYC1})$		ns
DAV ↑ to $\overline{DAC}$ ↓ delay (output three wire handshake) 1/	t_{HHL16}	65	All	9,10,11	0		ns
Counter input cycle time 1/	t_{CYC3}	66	01 02	9,10,11	500 330		ns
Counter input high width 1/	t_{PWH5}	67	01 02	9,10,11	230 150		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Parameter	Symbol	Conditions t_C = -55°C to +125°C, V_{CC} = 4.5 to 5.5 V, See figure 3, C_L = 50 pF ±10%			Minimum	Maximum	Unit
		Reference number 2/	Device type	Group A subgroups			
Counter input low width 1/	t_{PWL5}	68	01 02	9,10,11	230 150		ns
Counter input fall time 1/	t_{FC2}	69	01 02	9,10,11		20 15	ns
Counter input rise time 1/	t_{RC2}	70	01 02	9,10,11		20 15	ns
$\overline{RD}$ ↓ to REQ ↓ delay	t_{PHL21}	80	01	9,10,11		500	ns
$\overline{RD}$ ↓ to $\overline{WAIT}$ ↓ delay	t_{PHL22}	81	01	9,10,11		500	ns
$\overline{WR}$ ↓ to REQ ↓ delay	t_{PHL23}	82	01	9,10,11		500	ns
$\overline{WR}$ ↓ to $\overline{WAIT}$ ↓ delay	t_{PHL24}	83	01	9,10,11		500	ns
PCLK ↓ to REQ ↑ delay	t_{PHL25}	84	01	9,10,11		300	ns
PCLK ↓ to $\overline{WAIT}$ ↑ delay	t_{PHL26}	85	01	9,10,11		300	ns
$\overline{ACKIN}$ ↓ to REQ ↑ delay 6/	t_{PHL27}	86	01	9,10,11		$8*(t_{CYC1})$ +1000	ns
$\overline{ACKIN}$ ↓ to $\overline{WAIT}$ ↑ delay 6/	t_{PHL28}	87	01	9,10,11		$10*(t_{CYC1})$ +600	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Parameter	Symbol	Conditions t_C = -55°C to +125°C, V_{CC} = 4.5 to 5.5 V, See figure 3, C_L = 50 pF ±10%			Minimum	Maximum	Unit
		Reference 2/ number	Device type	Group A subgroups			
Delay from $\overline{RD}$ ↑ to $\overline{WR}$ ↓ for no reset 1/	t_{SHL16}	88	All	9,10,11	50		ns
Delay from $\overline{WR}$ ↑ to $\overline{RD}$ ↓ for no reset 1/	t_{SHL17}	89	All	9,10,11	50		ns
Width of $\overline{RD}$ and $\overline{WR}$ low to insure reset	t_{PWL6}	90	All	9,10,11	250		ns
Any input rise time not otherwise specified 1/	t_{RI1}	91	All	9,10,11		100	ns
Any input fall time not otherwise specified 1/	t_{FI1}	92	All	9,10,11		100	ns
1's catcher high width 1/ 9/	t_{PWH7}	93	01 02	9,10,11	250 170		ns
Pattern match input valid (bit port) 1/	t_{PWL8} t_{PWH8}	94	01 02	9,10,11	750 500		ns
Data latched on pattern match setup time (bit port) 1/	t_{SHL18} t_{SLH18}	95	All	9,10,11	0		ns
Data latched on pattern match hold time (bit port) 1/	t_{HHL17} t_{HLH17}	96	01 02	9,10,11	1000 650		ns

See footnotes on next page.

1/ Guaranteed if not tested.

2/ The reference number refers to the parameter being measured on figure 3.

3/ Parameter does not apply to Interrupt Acknowledge transactions.

4/ Float delay is measured to the time when the output has changed 0.5 V with minimum ac load and maximum dc load.

5/ t_{CYC2} is 1 µs or t_{CYC1}, whichever is longer.

6/ The delay is from $\overline{DAV}$ ↓ for 3-wire input handshake. The delay is from DAC ↓ for 3-wire output handshake.

7/ The parameters for the devices in any particular daisy chain must meet the following constraint: The delay from $\overline{INTACK}$ ↓ to $\overline{RD}$ ↓ must be greater than the sum of tdIA(IEO) for the highest priority peripheral, tsIEI(RDA) for the lowest priority peripheral, and tdIEI(IEO) for each peripheral separating them in the chain.

8/ This time can be extended through the use of deskew timers.

9/ If the input is programmed inverting, a low-going pulse of the same width will be detected.

Device types 01 and 02

Case Q

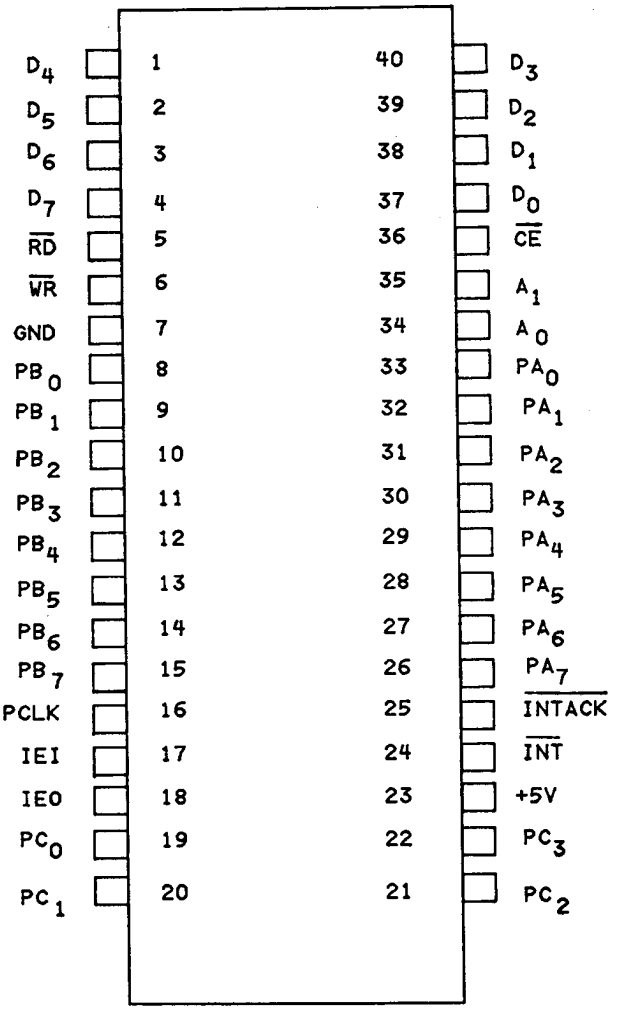

FIGURE 1. Terminal connections (top view).

Device types 01 and 02

Case Y

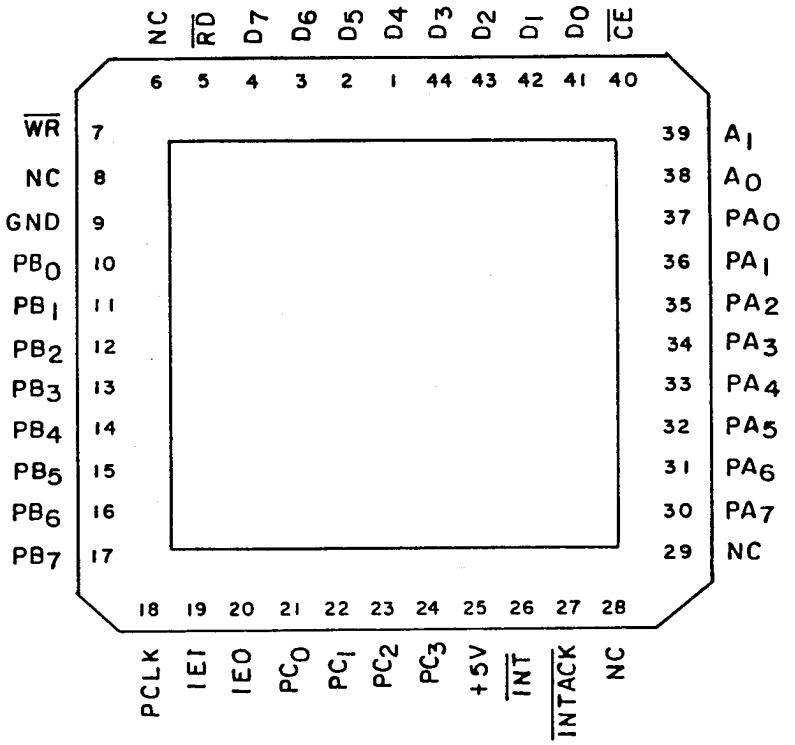

FIGURE 1. Terminal connections - Continued.

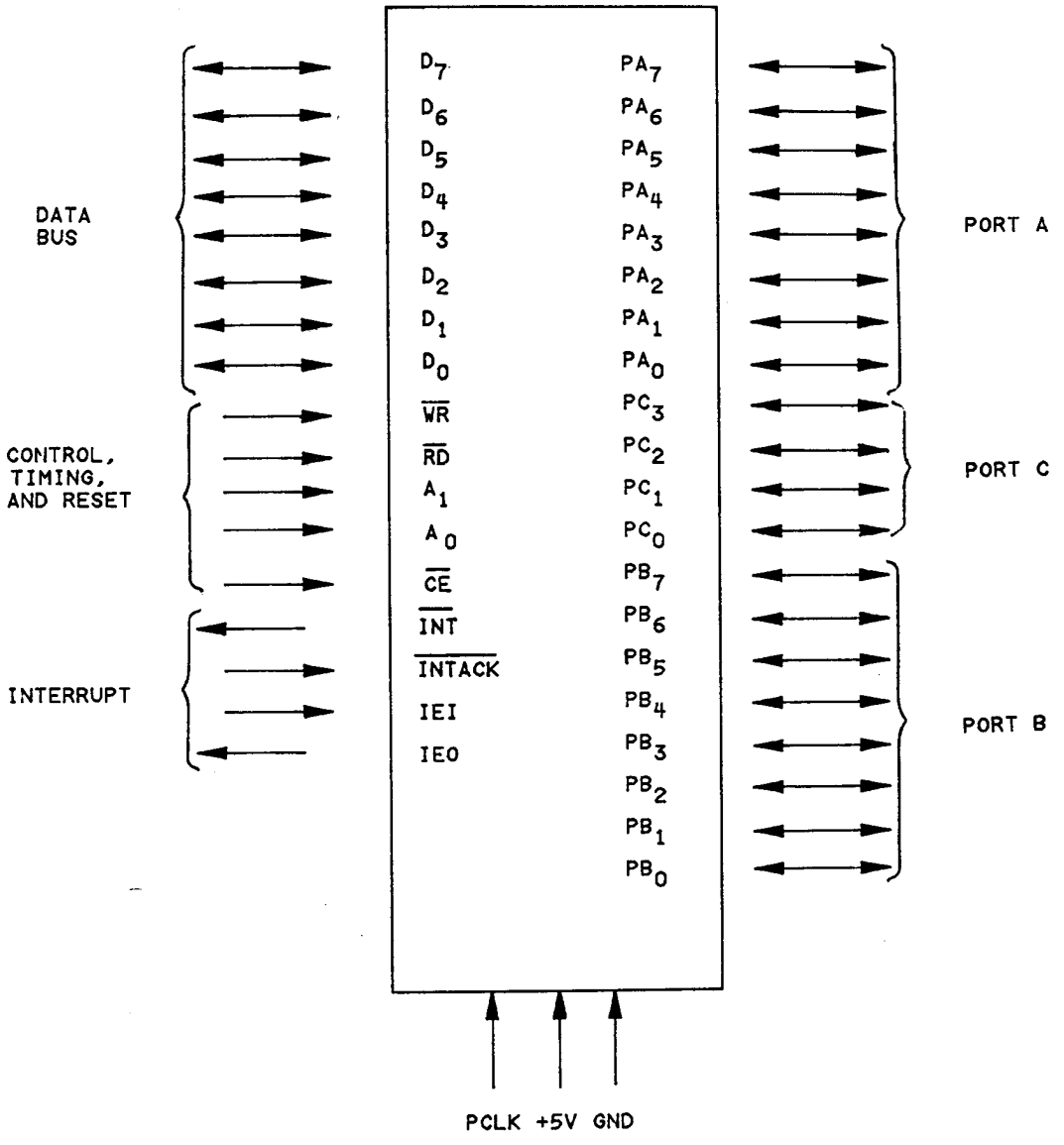

FIGURE 2. Logic functions.

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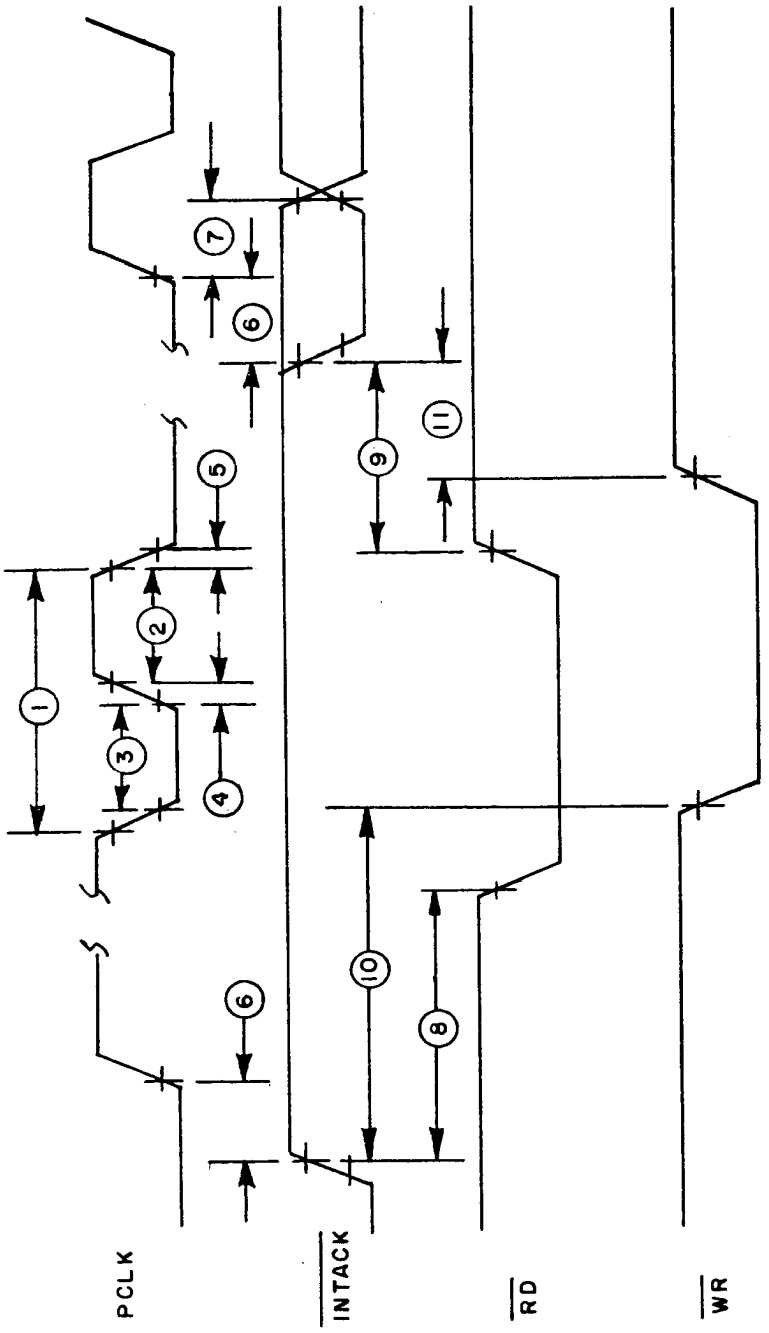
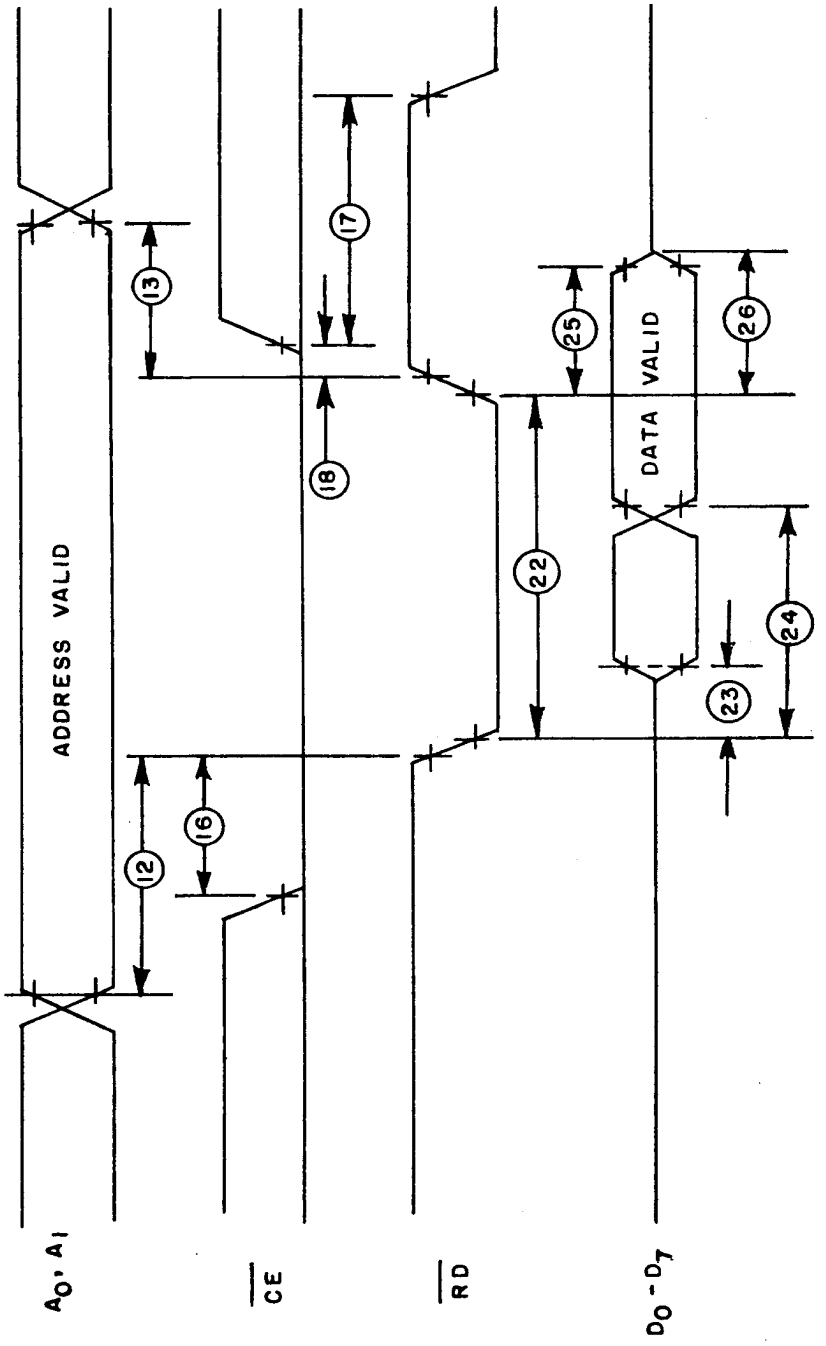


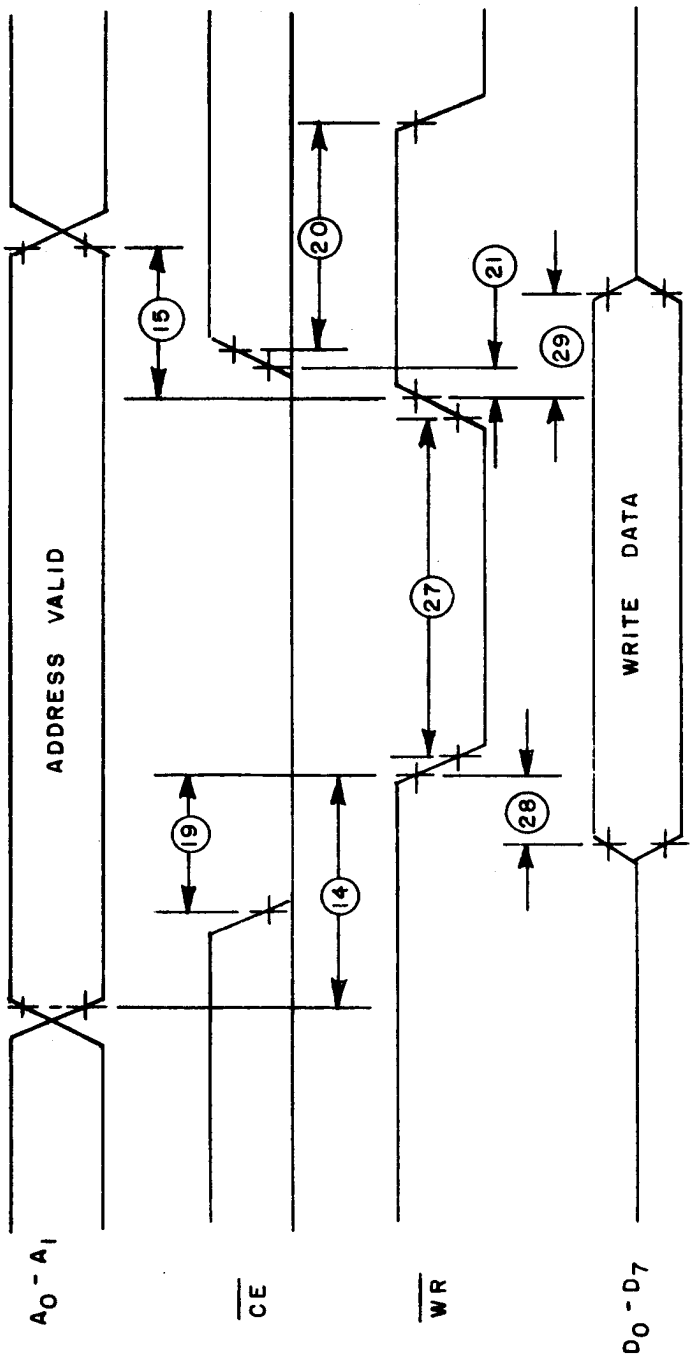
PCLK, INTACK timing

FIGURE 3. Timing waveforms.



Read cycle timing

FIGURE 3. Timing waveforms - Continued.



Write cycle timing

FIGURE 3. Timing waveforms - Continued.

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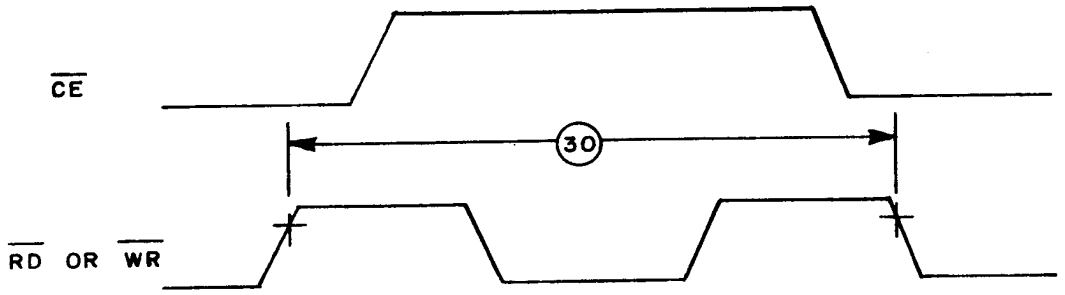

Valid access recovery time

FIGURE 3. Timing waveforms - Continued.

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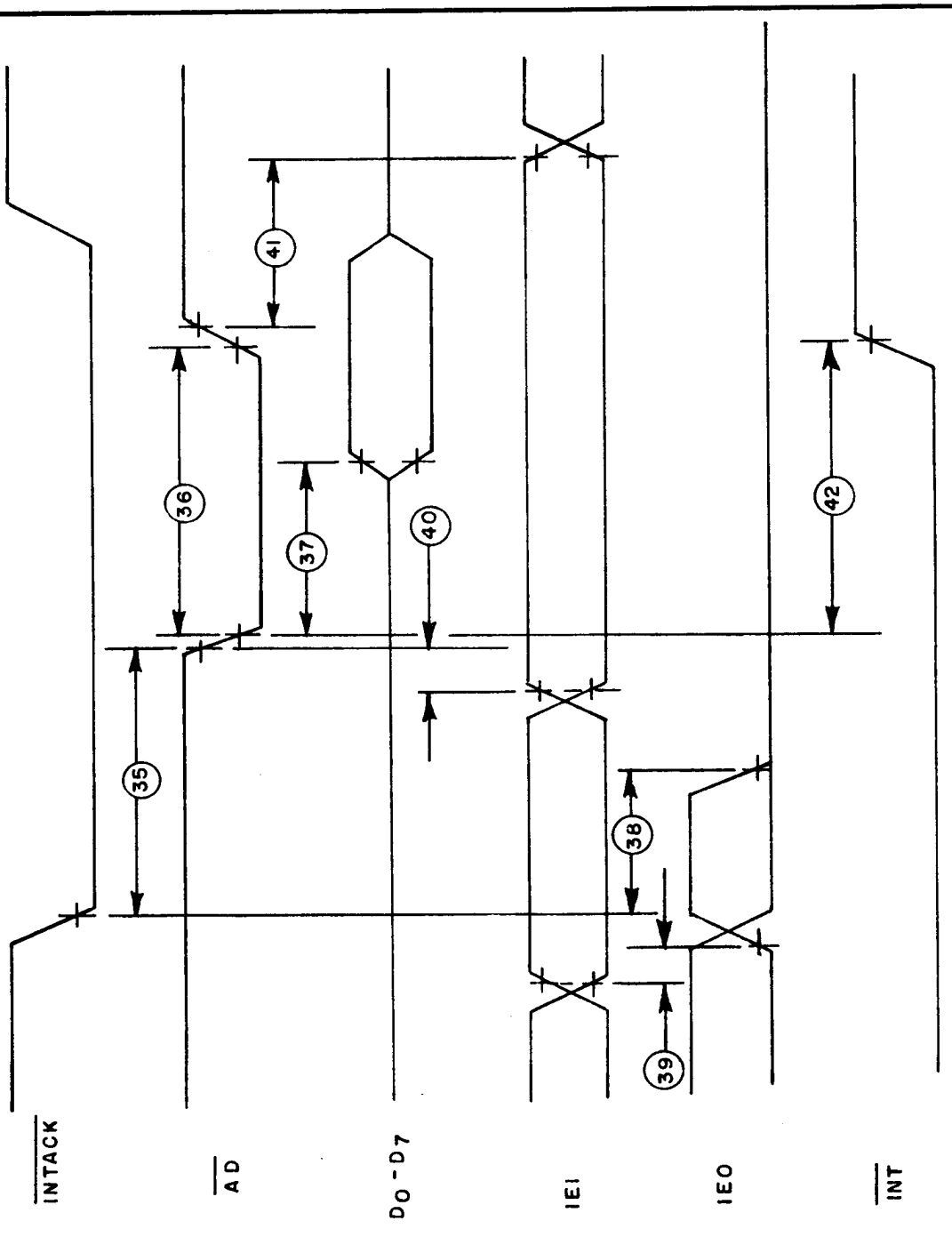
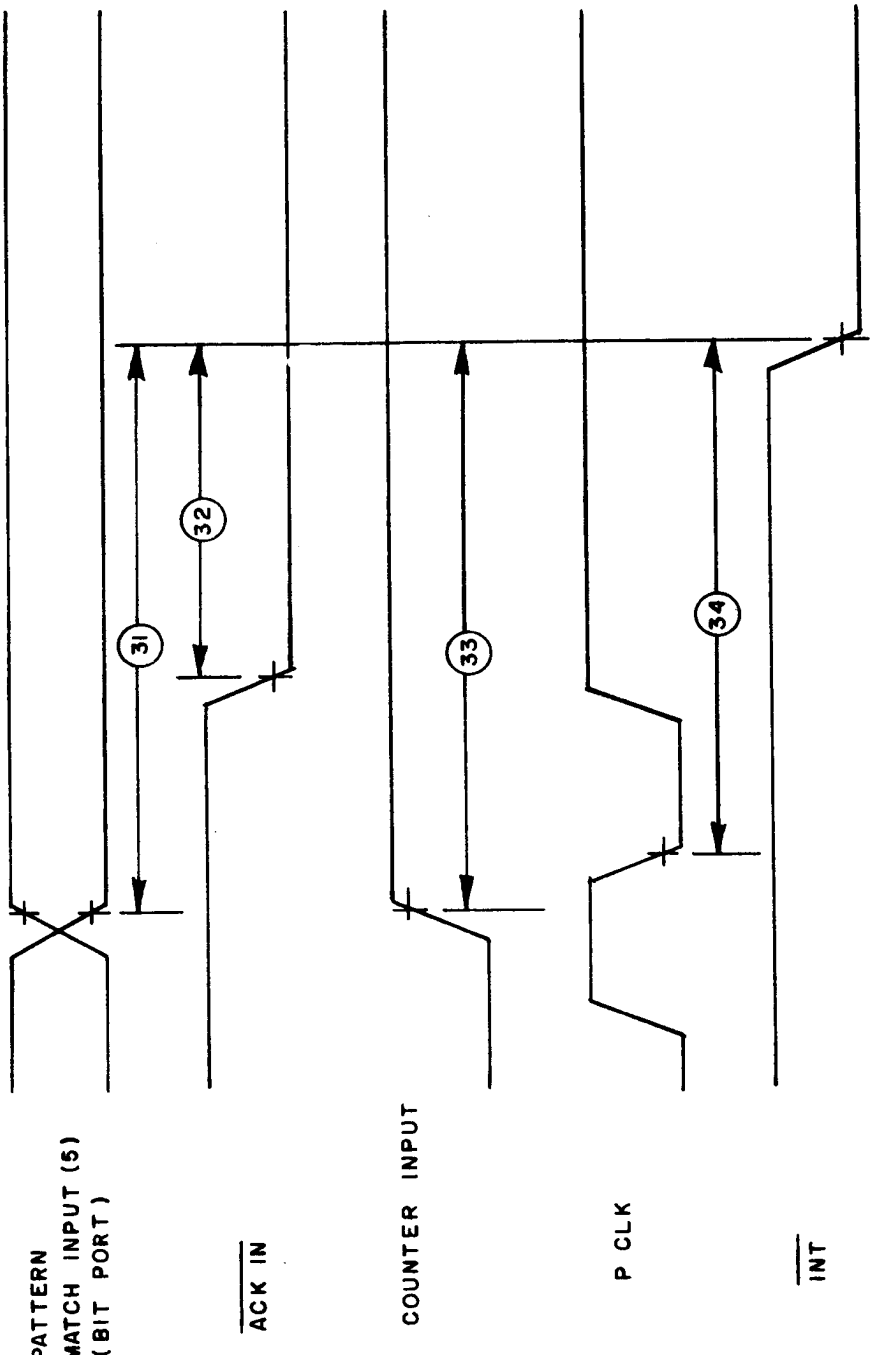


Interrunt acknowledge timing

FIGURE 3. Timing waveforms - Continued.



Interrupt timing

FIGURE 3. Timing waveforms - Continued.

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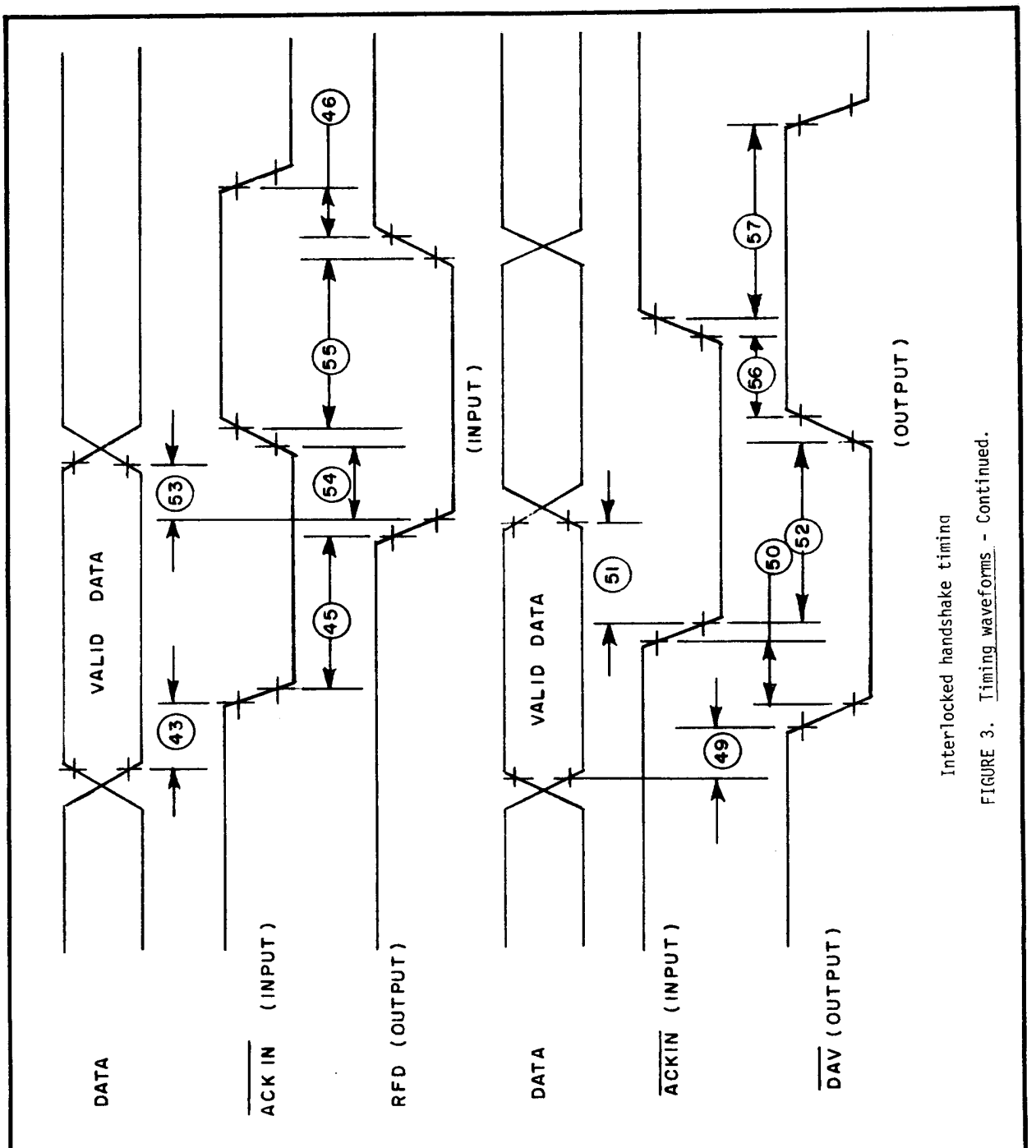

Interlocked handshake timing

FIGURE 3. Timing waveforms - Continued.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		83001
		REVISION LEVEL C	SHEET 24

DESC FORM 193A
SEP 87

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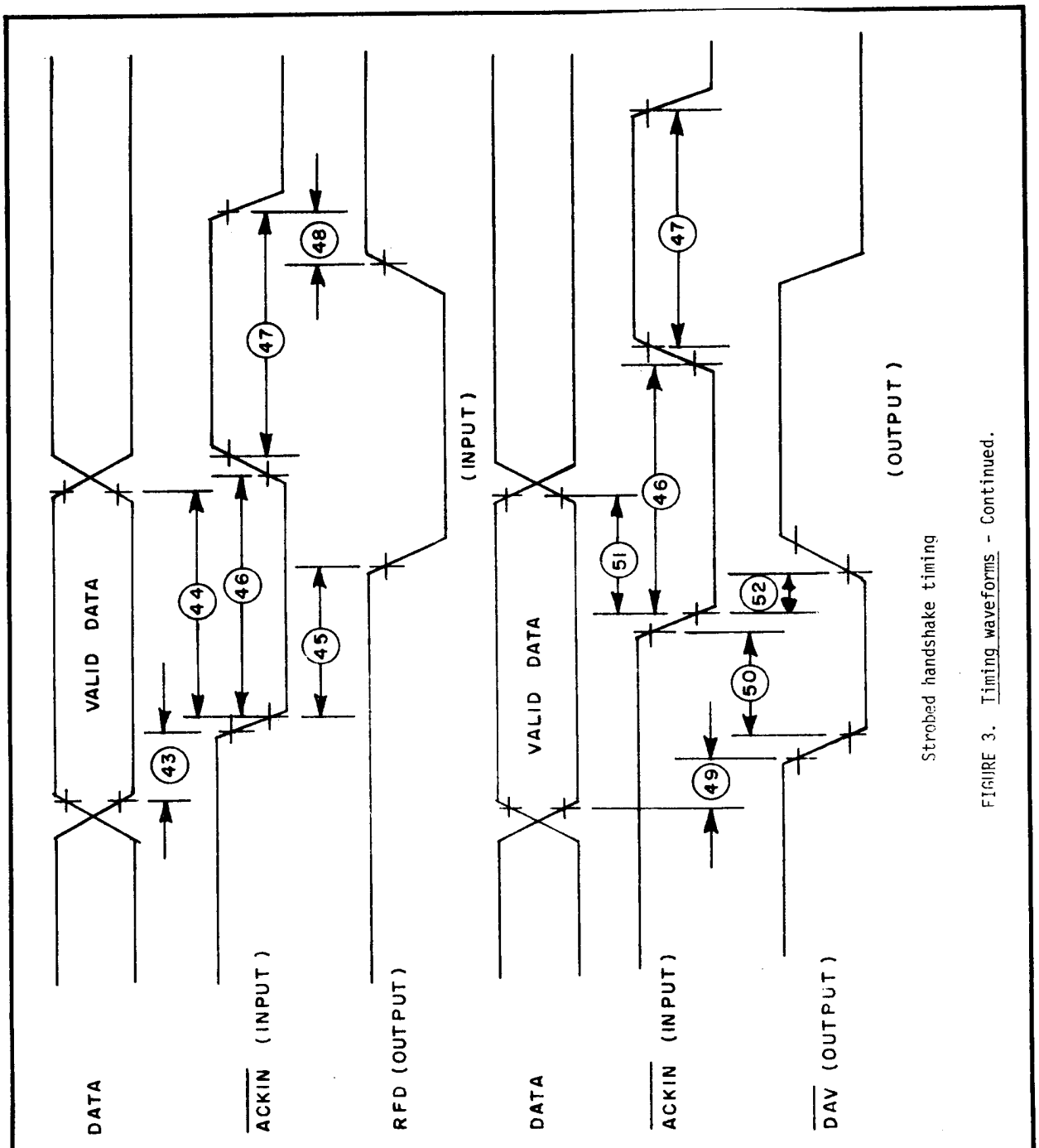

Strobed handshake timing

FIGURE 3. Timing waveforms - Continued.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		83001
		REVISION LEVEL C	SHEET 25

DESC FORM 193A
SEP 87

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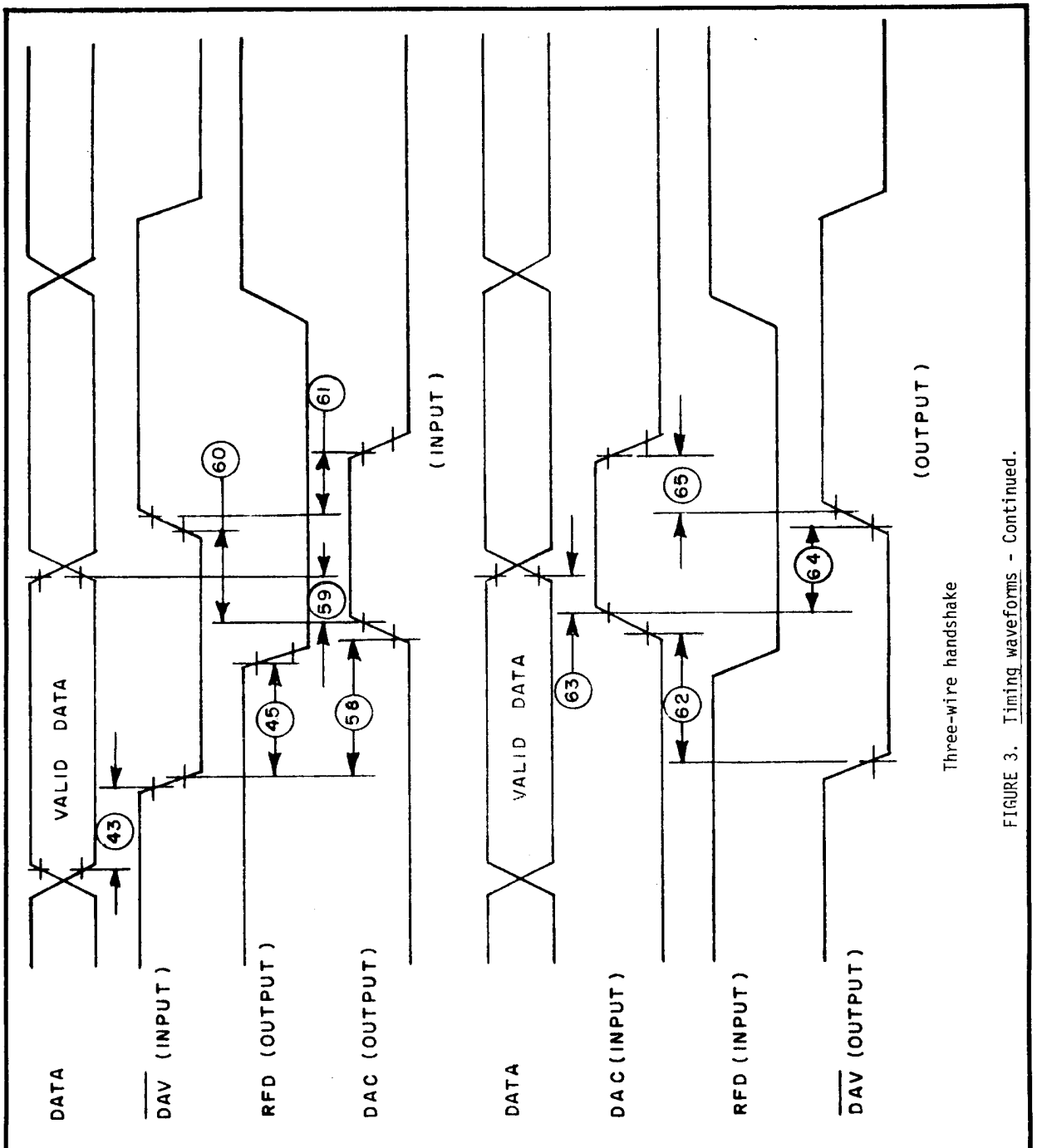

Three-wire handshake

FIGURE 3. Timing waveforms - Continued.

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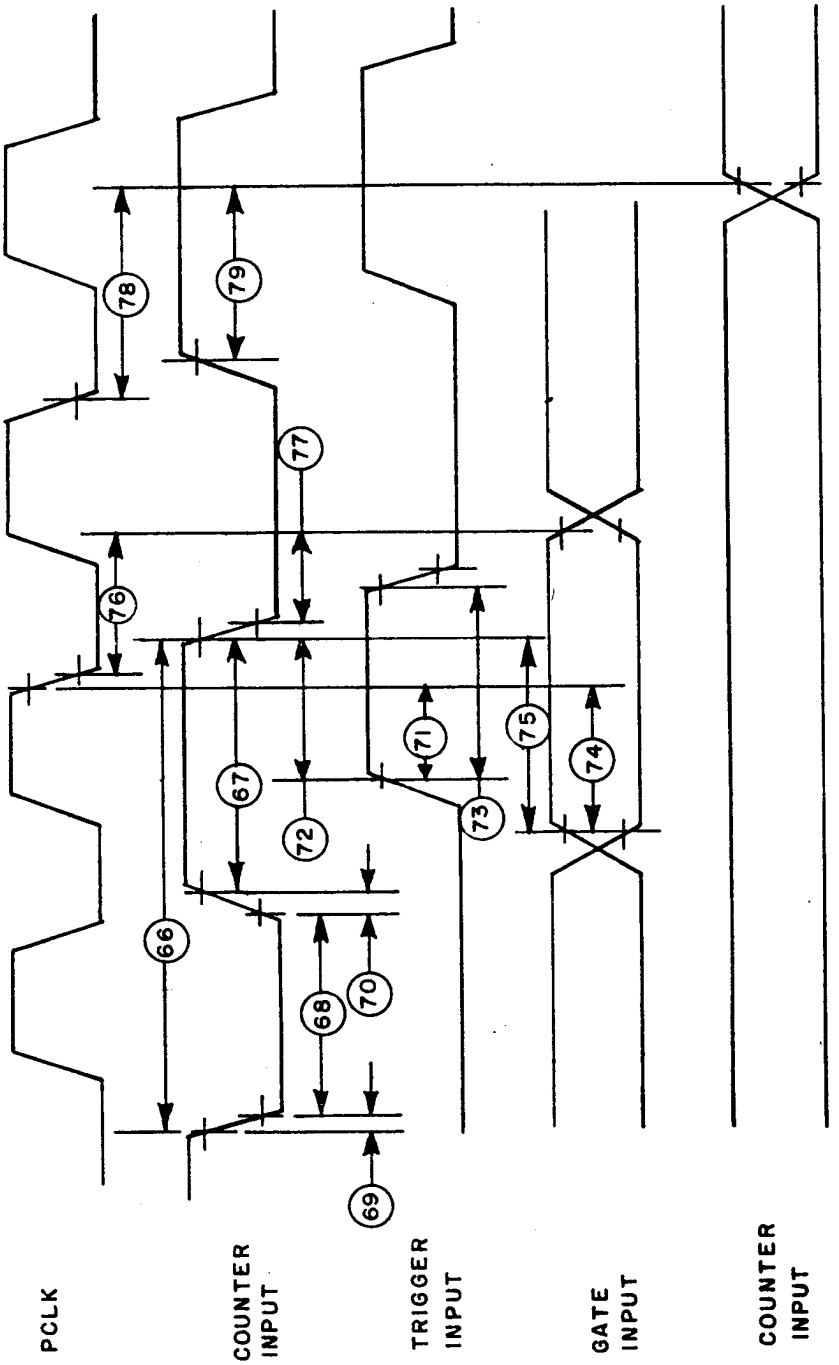

Counter/timer timing

FIGURE 3. Timing waveforms - Continued.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		83001
		REVISION LEVEL C	SHEET 27

DESC FORM 193A
SEP 87

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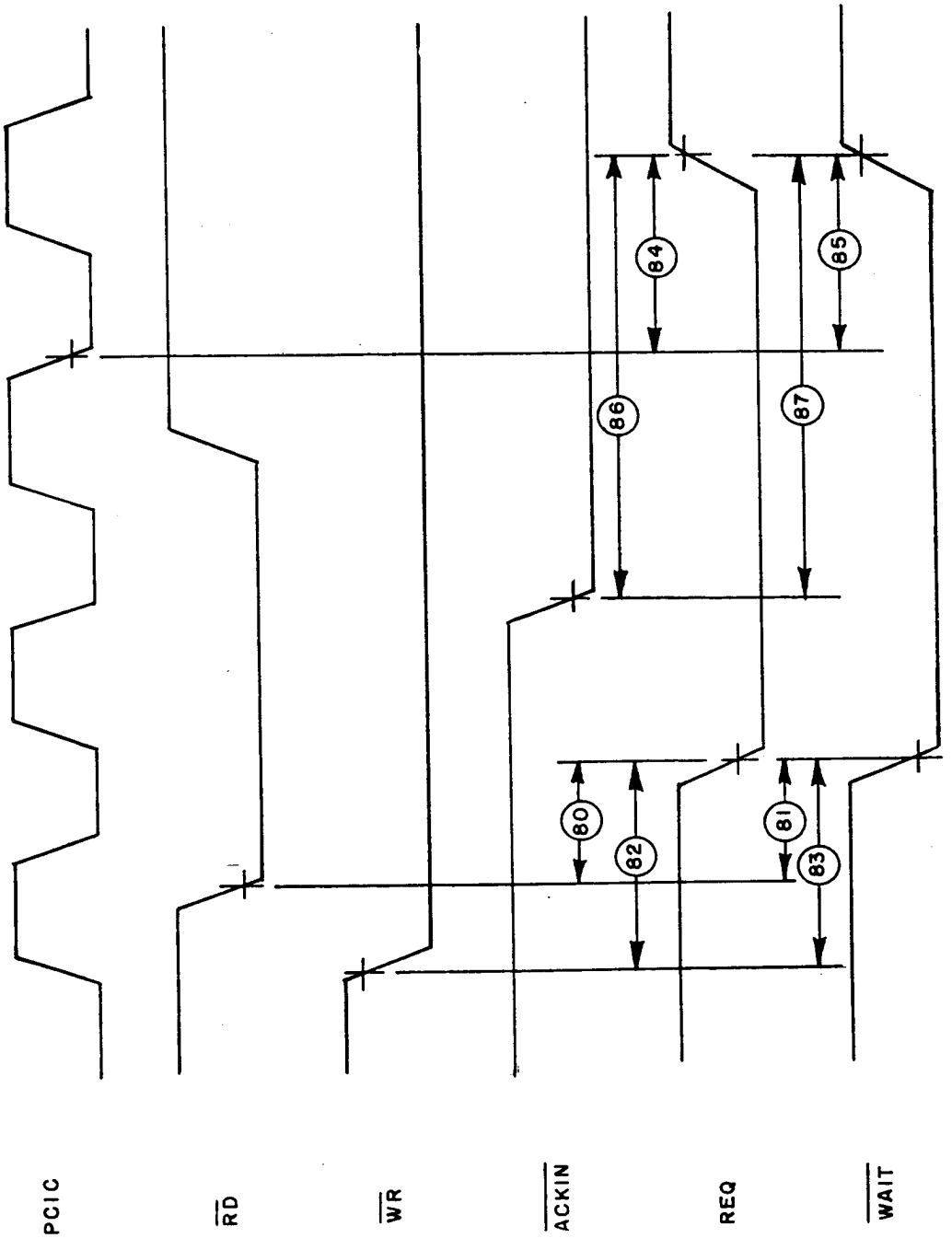
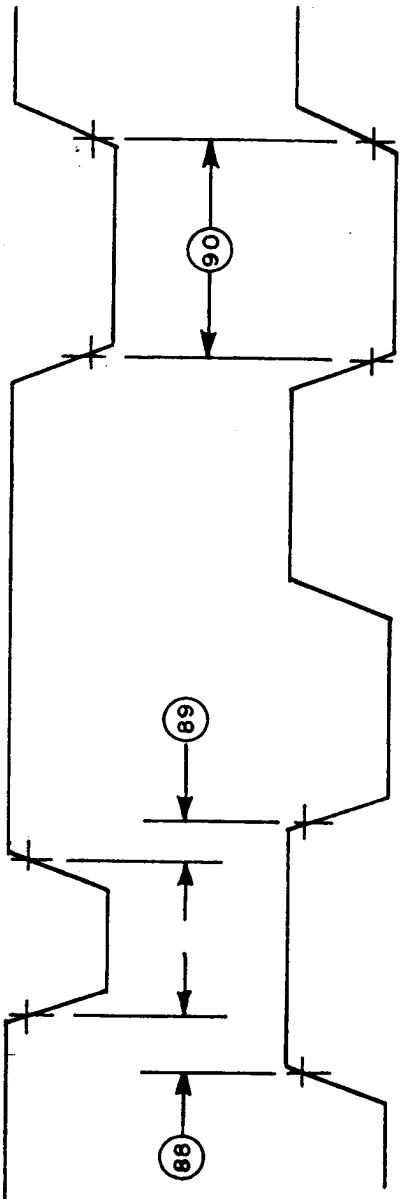


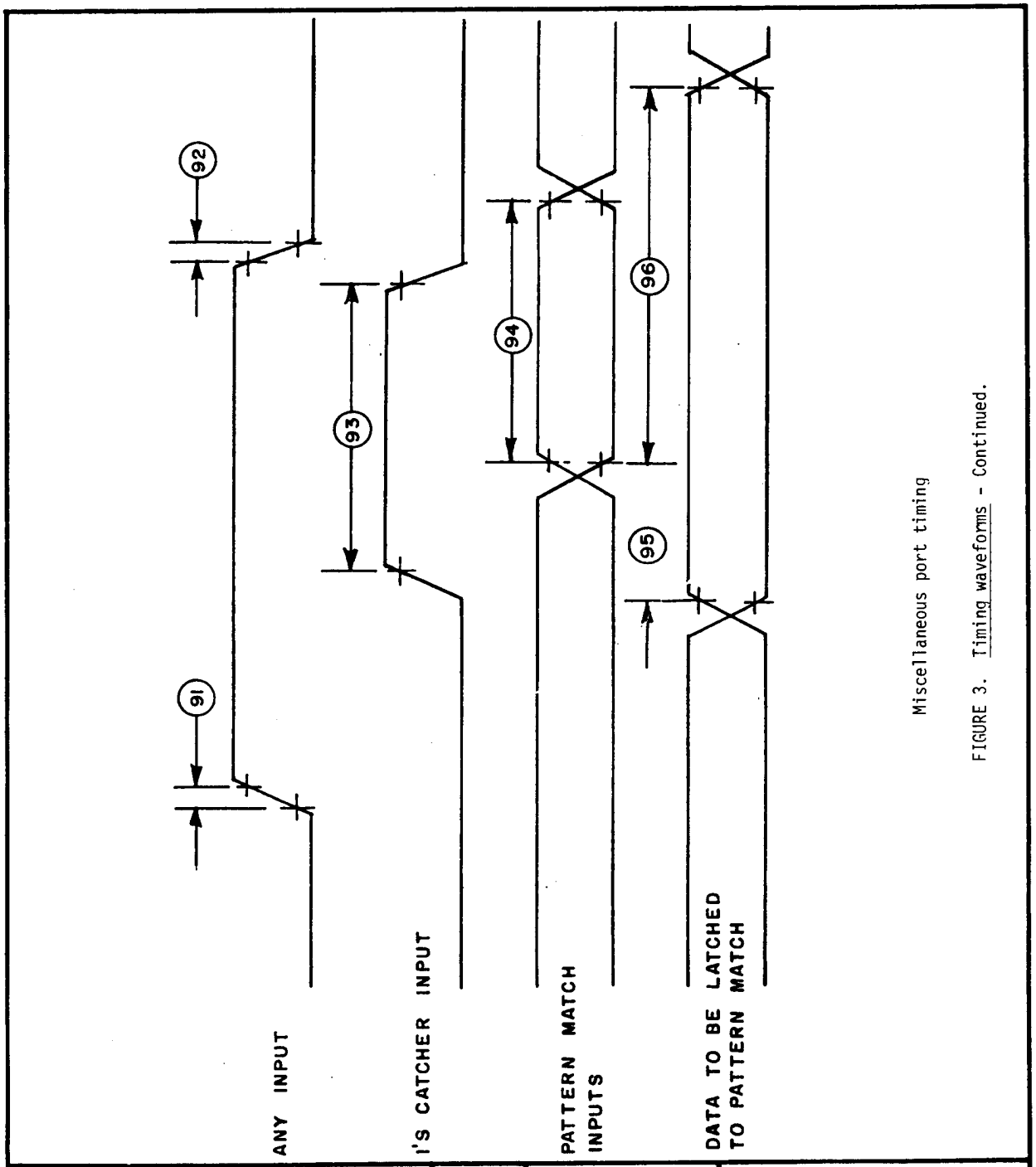
FIGURE 3. Timing waveforms - Continued.

REQUEST/WAIT timing



Reset timing

FIGURE 3. Timing waveforms - Continued.



Miscellaneous port timing

FIGURE 3. Timing waveforms - Continued.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.5. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 7 functional test shall include verification of programming set.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test (method 1005 of MIL-STD-883) conditions:

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	
Final electrical test parameters (method 5004)	1*,2,3,9
Group A test requirements (method 5005)	1,2,3,7,8,9, 10, 11**
Groups C and D end-point electrical parameters (method 5005)	1,2,3

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Terminal and functional definitions. Terminal and functional definitions and descriptions for this device shall be as follows:

IEI	Interrupt enable in (input, active high). When this line is active, the CIO is able to interrupt the CPU.
IEO	Interrupt enable out (output, active high). This output is high only if IEI is high and the CPU is not servicing an interrupt from this CIO. In conjunction with IEI, this line can be used to implement a system-wide interrupt priority daisy chain.
$\overline{INT}$	Interrupt request (output, open drain, active low). This signal is pulled low when the CIO requests an interrupt.
$\overline{INTACK}$	Interrupt acknowledge (input, active low). This signal indicates to the CIO that an interrupt acknowledge cycle is in progress. $\overline{INTACK}$ must be synchronized to P clock.
PA0-PA7	Port A I/O lines (bidirectional, tristate or open drain). These eight I/O lines transfer information between the CIO's port A and external devices.
PB0-PB7	Port B I/O lines (bidirectional, tristate or open drain). These eight I/O lines transfer information between the CIO's port B and external devices. They also provide external access to counter/timers 1 and 2.
PC0-PC3	Port C I/O lines (bidirectional, tristate or open drain). These four I/O lines are used to provide handshake, WAIT, and REQUEST lines for ports A and B, to provide external access to counter/timer 3 or to the CIO's port C.
PCLK	Peripheral clock (input, TTL compatible). This is a peripheral clock that may be, but is not necessarily the CPU clock. It is used with the timers and the REQUEST/WAIT logic. The maximum input frequency is 4 MHz.
A0-A1	Address lines (input). These two lines are used to select the register involved in a data transaction between the CIO and CPU.
$\overline{CE}$	Chip enable (input, active low). A low level on this input enables the CPU to be read from or written to.
D0-D7	Data bus (bidirectional, tristate). These eight data lines are used for transfers between the CPU and the CIO.
$\overline{RD}$ *	Read (input, active low). This signal indicates that a CPU is reading from the CIO. During an INT ACK cycle, gates the interrupt vector on to data bus.
$\overline{WR}$ *	Write (input, active low). This signal indicates a CPU write to the CIO.
*	When $\overline{RD}$ and $\overline{WR}$ are detected low at same time (normally an illegal condition) the device is reset.

6.5 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
8300101QX 8300101YX	56708 56708	Z0853604CMB 2/ Z0853604LMB	---
8300102QX 8300102YX	56708 56708	Z0853606CMB 3/ Z0853606LMB	---

1/ Caution: Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

2/ Part was previously designated Z8536CMB.

3/ Part was previously designated Z8536ACMB.

Vendor CAGE number	Vendor name and address
56708	Zilog Incorporated 210 Hacienda Avenue Campbell, California 95008

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