

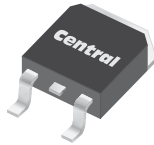
CJD112 NPN
CJD117 PNP

**SURFACE MOUNT
COMPLEMENTARY SILICON
POWER DARLINGTON TRANSISTORS**



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**DPAK
POWER!**



DPAK TRANSISTOR CASE

DESCRIPTION:

The CENTRAL SEMICONDUCTOR CJD112, CJD117 types are Complementary Silicon Power Darlington Transistors manufactured in a surface mount package designed for low speed switching and amplifier applications.

MARKING: FULL PART NUMBER

MAXIMUM RATINGS: ($T_C=25^\circ\text{C}$ unless otherwise noted)

	SYMBOL		UNITS
Collector-Base Voltage	V_{CBO}	100	V
Collector-Emitter Voltage	V_{CEO}	100	V
Emitter-Base Voltage	V_{EBO}	5.0	V
Continuous Collector Current	I_C	2.0	A
Peak Collector Current	I_{CM}	4.0	A
Continuous Base Current	I_B	50	mA
Power Dissipation	P_D	20	W
Power Dissipation ($T_A=25^\circ\text{C}$)	P_D	1.75	W
Operating and Storage Junction Temperature	T_J, T_{stg}	-65 to +150	$^\circ\text{C}$
Thermal Resistance	θ_{JC}	6.25	$^\circ\text{C/W}$
Thermal Resistance	θ_{JA}	71.4	$^\circ\text{C/W}$

ELECTRICAL CHARACTERISTICS: ($T_C=25^\circ\text{C}$ unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
I_{CEO}	$V_{CE}=50\text{V}$		20	μA
I_{CEV}	$V_{CE}=80\text{V}, V_{BE(\text{off})}=1.5\text{V}$		10	μA
I_{CEV}	$V_{CE}=80\text{V}, V_{BE(\text{off})}=1.5\text{V}, T_C=125^\circ\text{C}$		500	μA
I_{CBO}	$V_{CB}=80\text{V}$		10	μA
I_{CBO}	$V_{CB}=100\text{V}$		20	μA
I_{EBO}	$V_{EB}=5.0\text{V}$		2.0	mA
BV_{CEO}	$I_C=30\text{mA}$		100	V
$V_{CE(\text{SAT})}$	$I_C=2.0\text{A}, I_B=8.0\text{mA}$		2.0	V
$V_{CE(\text{SAT})}$	$I_C=4.0\text{A}, I_B=40\text{mA}$		3.0	V
$V_{BE(\text{SAT})}$	$I_C=4.0\text{A}, I_B=40\text{mA}$		4.0	V
$V_{BE(\text{ON})}$	$V_{CE}=3.0\text{V}, I_C=2.0\text{A}$		2.8	V
h_{FE}	$V_{CE}=3.0\text{V}, I_C=0.5\text{A}$	500		
h_{FE}	$V_{CE}=3.0\text{V}, I_C=2.0\text{A}$	1000	12000	
h_{FE}	$V_{CE}=3.0\text{V}, I_C=4.0\text{A}$	200		
f_T	$V_{CE}=10\text{V}, I_C=750\text{mA}, f=1.0\text{MHz}$	25		MHz
C_{ob}	$V_{CB}=10\text{V}, I_E=0, f=0.1\text{MHz}$ (CJD112)		100	pF
C_{ob}	$V_{CB}=10\text{V}, I_E=0, f=0.1\text{MHz}$ (CJD117)		200	pF

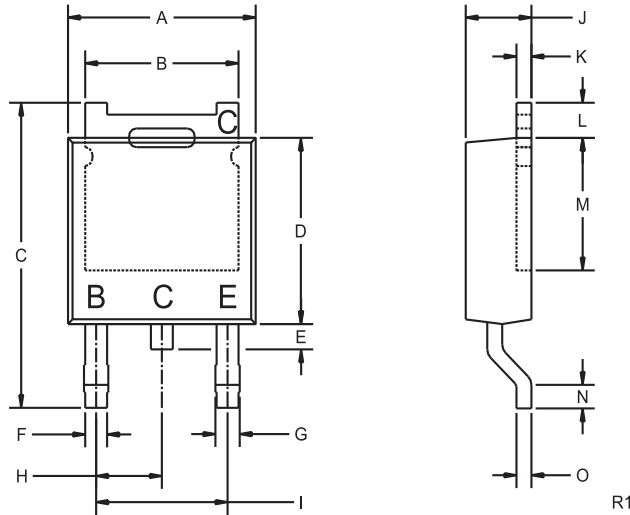
R2 (4-January 2010)

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DPAK TRANSISTOR CASE - MECHANICAL OUTLINE



DIMENSIONS				
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.250	0.265	6.35	6.73
B	0.205	0.215	5.21	5.46
C	0.374	0.409	9.50	10.40
D	0.235	0.245	5.97	6.22
E	0.025	0.040	0.64	1.02
F	0.025	0.035	0.64	0.88
G	0.030	0.045	0.76	1.14
H	0.090		2.28	
I	0.180		4.57	
J	0.086	0.094	2.19	2.38
K	0.018	0.023	0.46	0.58
L	0.040	0.050	1.02	1.27
M	0.170	-	4.32	-
N	0.020	-	0.51	-
O	0.018	0.023	0.46	0.58

LEAD CODE:
B) BASE
C) COLLECTOR
E) EMITTER
C) COLLECTOR

MARKING:
FULL PART NUMBER

DPAK TRANSISTOR (REV: R1)

R2 (4-January 2010)