Video output amplifier TDA6101BQ

FEATURES

- High bandwidth and high slew rate
- Maximum operating voltage 250 V
- Black-current measurement output for automatic black current stabilization (ABS)
- Two cathode outputs: one for DC currents and one for transient currents
- A feedback output separated from the cathode outputs
- Internal protection against positive appearing CRT flashover discharges
- ESD protection
- Simple application with a variety of colour decoders
- Differential input, with a designed maximum common mode input capacitance of 3 pF; a differential mode input capacitance of 2 pF and a differential input voltage temperature drift of 0.4 mV/K.

GENERAL DESCRIPTION

The TDA6101BQ is a video output amplifier with an 8 MHz bandwidth. The device is contained in a SIL9 MP (single in-line 9 pin medium power) package. The device employs high voltage DMOS technology, and is designed to drive the cathode of a CRT.

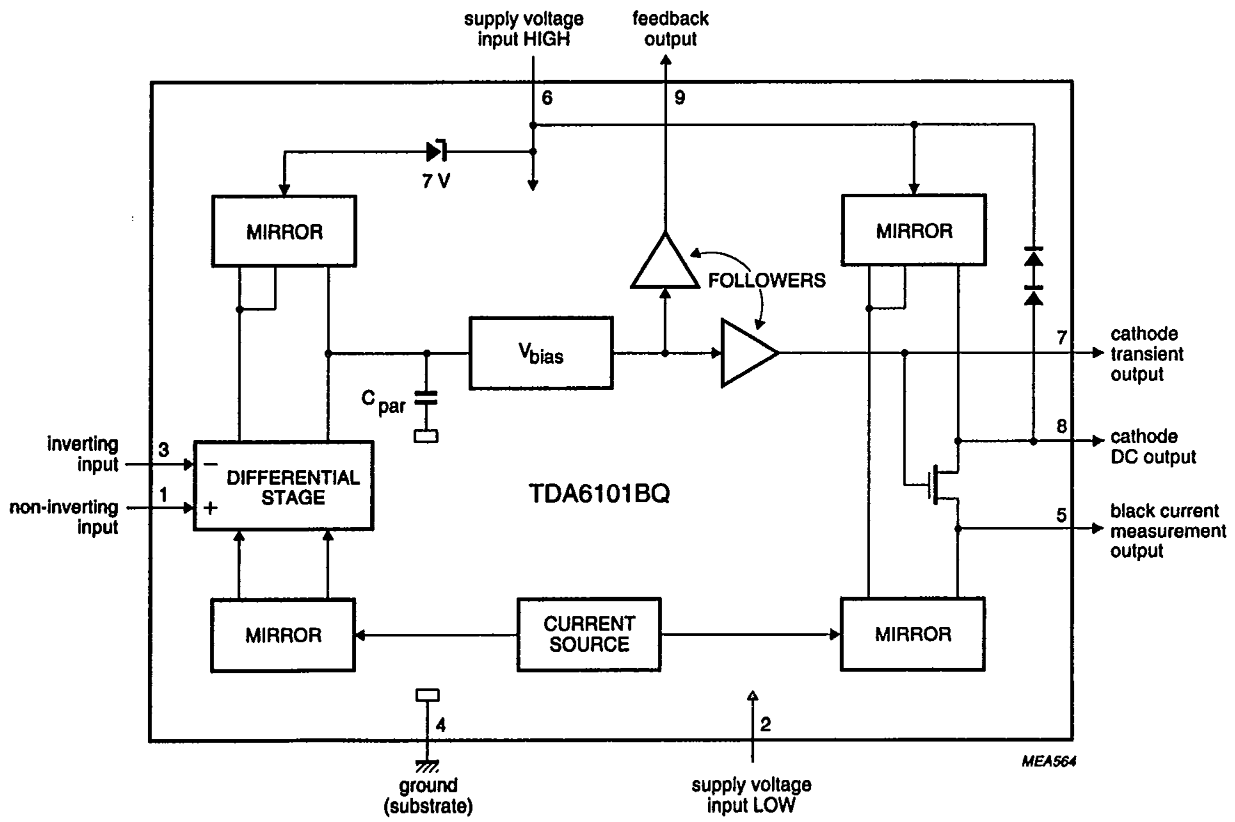


Fig.1 Block diagram.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA6101BQ	9	DBS	plastic	SOT111

PINNING

SYMBOL	PIN	DESCRIPTION
V_{ip}	1	non inverting input
V_{DDL}	2	supply voltage LOW
V_{in}	3	inverting input
GND	4	ground; substrate
I_{om}	5	black current measurement output
V_{DDH}	6	supply voltage HIGH
V_{cn}	7	cathode transient output
V_{oc}	8	cathode DC output
V_{of}	9	feedback output

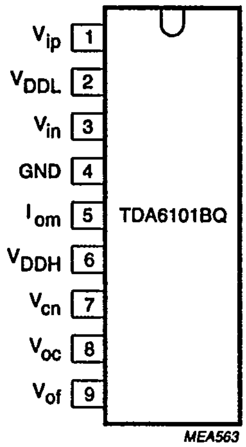


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Dissipation

A distinction must first be made between static dissipation (independent of frequency) and dynamic dissipation (proportional to frequency).

The static dissipation of the TDA6101BQ is due to HIGH and LOW voltage supply currents and load currents in the feedback network and CRT.

$P_{stat} = V_{DDL} \times I_{DDL} + V_{DDH} \times I_{DDH} + V_{oc} \times I_{oc} - V_{of} \times V_{of}/Rt$

Where R_t = value of feedback resistor and I_{oc} = DC value of cathode current.

The dynamic dissipation equals:

$P_{dyn} = V_{DDH} \times (C_L + C_t + C_{int}) \times f \times V_{O\ (p\text{-}p)} \times b$

Where:

C_L = load capacitance

C_t = feedback capacitance

C_{int} = internal load capacitance (4 pF)

f = frequency

$V_{O\ (p\text{-}p)}$ = output voltage (peak-to-peak value)

b = non-blanking duty cycle

The IC must be mounted on the picture tube base print to minimize the load capacitance C_L.

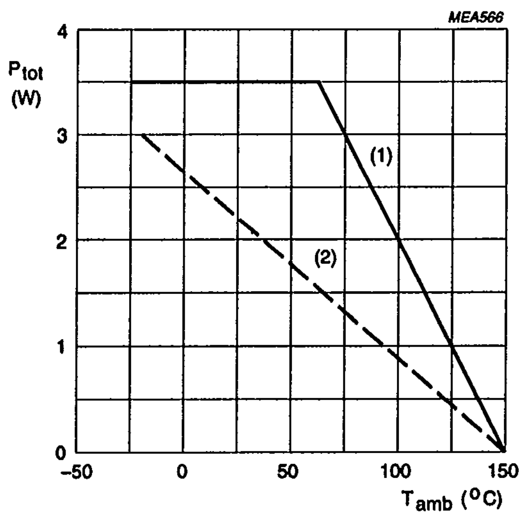
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134). Voltages with respect to pin 4 (ground) unless otherwise specified, currents specified as in Fig.1.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDH}	HIGH level supply voltage	0	280	V
V_{DDL}	LOW level supply voltage	0	14	V
V_I	input voltage	0	V_{DDL}	V
$V_{I,dm}$	differential mode input voltage	−6	+6	V
V_{om}	measurement output voltage	0	V_{DDL}	V
V_{oc},V_{of}	output voltage	V_{DDL}	V_{DDH}	V
I_{in},I_{ip}	input current	0	1	mA
I_{OCL}	LOW non-repetitive peak cathode output current (50 µC)	0	5	A
I_{OCH}	HIGH non-repetitive peak cathode output current (100 nC)	0	10	A
P_{tot}	total power dissipation	0	1.9	W
T_{stg}	storage temperature	−55	+150	°C
T_j	junction temperature	−20	+150	°C
V_{ESD}	voltage peak (ESD-HBM)	–	> 2000	V
V_{ESD}	voltage peak (ESD-MM)	–	> 400	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	56 K/W
$R_{th\ j\text{-}c}$	from junction to mounting case	12 K/W



(1) Mounted on heatsink of 12 K/W.
(2) No external heatsink.

Fig.3 Power derating curves.

Quality specification

Quality specification SNW-FQ-611 part E is applicable.

CHARACTERISTICS

Operating range: T_{amb} = −20 to 65 °C; V_{DDH} = 180 to 250 V; V_{DDL} = 10.8 to 13.2 V; V_{ip} = 2.6 to 5 V; V_{om} = 1.4 V to V_{DDL}.
Test conditions: (unless otherwise specified) T_{amb} = 25 °C; V_{DDH} = 230 V; V_{DDL} = 12 V; V_{ip} = 5 V; V_{om} = 6 V; C_L = 10 pF (C_L consists of parasitic and cathode capacitance). Measured in Test circuit Fig.4.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DDH}	quiescent HIGH voltage supply current	$V_{oc} = V_{DDH}/2$	3.7	4.6	5.7	mA
I_{DDL}	quiescent LOW voltage supply current	$V_{oc} = V_{DDH}/2$	2.3	2.9	3.6	mA
I_{bias}	input bias current	$V_{oc} = V_{DDH}/2$	0	–	20	µA
$I_{i,OFF}$	input offset current	$V_{oc} = V_{DDH}/2$	−3	–	+3	µA
$I_{om,OFF}$	offset current of measurement output	I_{oc} = 0 µA; −1.0 V < V_{1-3} < 1.0 V; 1.4 < V_{om} < V_{DDL}	−5	0	+5	µA
$\Delta I_{om} / \Delta I_{oc}$	linearity of current transfer	−10 µA < I_{oc} < 3 mA; −1.0 V < V_{1-3} < 1.0 V; 1.4 < V_{om} < V_{DDL}	0.9	1	1.1	
$V_{i,OFF}$	input offset voltage	$V_{oc} = V_{DDH}/2$	−50	–	+50	mV
$V_{oc\ min}$	minimum output voltage	V_{1-3} = −1 V	–	–	20	V
$V_{oc\ max}$	maximum output voltage	V_{1-3} = 1 V	V_{DDH}−12	–	–	V
GB	gain-bandwidth product of open-loop gain: $V_o/V_{i,dm}$	f = 500 kHz; $V_{oc-DC} = V_{DDH}/2$	–	0.9	–	GHz
B_S	small signal bandwidth	V_{oc-AC} = 60 V (p-p); $V_{oc-DC} = V_{DDH}/2$	6.5	9	–	MHz
B_L	large signal bandwidth	V_{oc-AC} = 100 V (p-p); $V_{oc-DC} = V_{DDH}/2$	5	7	–	MHz
t_{prop}	cathode output propagation time 50% input to 50% output (see Fig.5 and Fig.6)	V_{oc-AC} = 100 V (p-p); $V_{oc-DC} = V_{DDH}/2$; square wave: f < 1 MHz; $t_{r,i}$, $t_{f,i}$ = 40 ns	25	36	47	ns
t_r	cathode output rise time 10% output to 90% output (see Fig.5)	V_{oc} = 65 to 165 V; square wave: f < 1 MHz; t_f, input = 40 ns;	38	50	63	ns
t_f	cathode output fall time 90% output to 10% output (see Fig.6)	V_{oc} = 165 to 65 V; square wave: f < 1 MHz; t_r, input = 40 ns;	38	50	63	ns
t_s	settling time 50% input – (99% < output < 101%) (see Fig.5 and Fig.6)	V_{oc-AC} = 100 V (p-p); $V_{oc-DC} = V_{DDH}/2$;; square wave: < 1 MHz; $t_{r,i}$; $t_{f,i}$ = 40 ns	–	–	350	ns
SR	slew rate between 50 V to 150 V	V_{1-3} = 2 V(p-p) square wave: f < 1 MHz; $t_{r,i}$; $t_{f,i}$ = 40 ns	–	1700	–	V/µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
O_V	cathode output voltage overshoot (see Fig.5 and Fig.6)	$V_{oc\text{-}AC}$ = 100 V (p-p); $V_{oc\text{-}DC} = V_{DDH}/2$;; square wave: f < 1 MHz; $t_{r,i}$; $t_{f,i}$ = 40 ns; note 1	–	7	–	%
R_i	differential input resistance		–	100	–	kΩ
SVRRH	HIGH voltage power supply rejection ratio	f < 50 kHz; note 2	–	80	–	dB
SVRRL	LOW voltage power supply rejection ratio	f < 50 kHz; note 2	–	80	–	dB

Notes

1. If the difference between V_{DDL} and V_{ip} is less then 7 V, overshoot cannot be specified.
2. SVRR is the ratio of the change in supply voltage to the change in input voltage when there is no change in output voltage.

Cathode output

The cathode output is protected against peak currents (caused by positive voltage peaks during high-resistance flash) of 5 A maximum with a charge content of 50 µC.

The cathode output is also protected against peak currents (caused by positive voltage peaks during low-resistance flash) of 10 A maximum with a charge content of 100 nC.

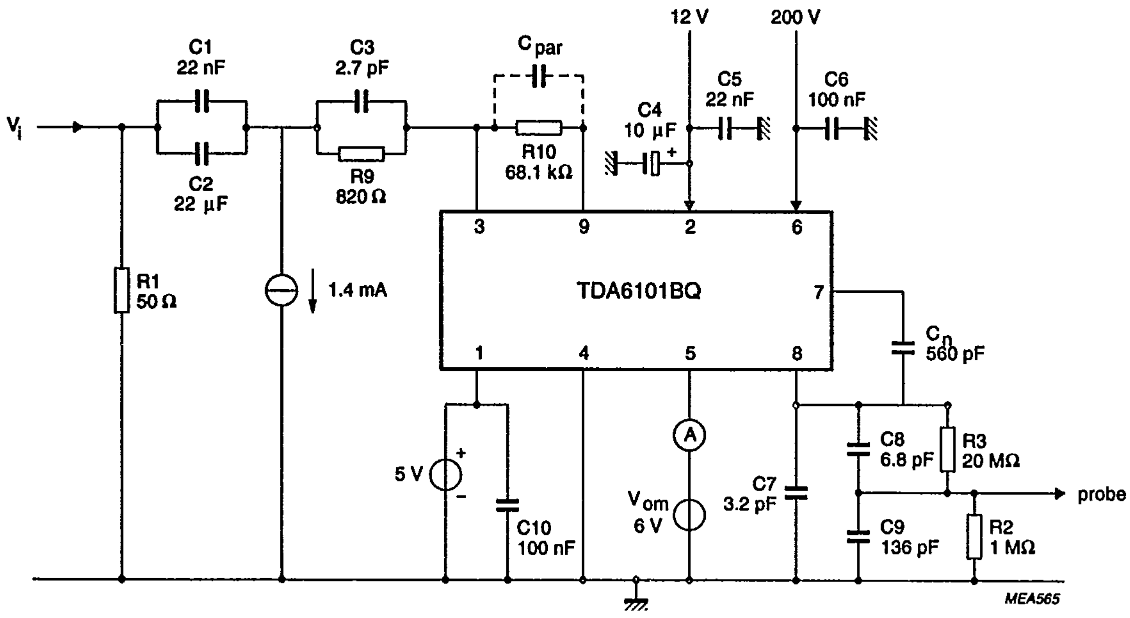


Fig.4 Test circuit with feedback factor 1/83; C_{par} is approximately 150 fF.

Note to Fig.4

FLASHOVER PROTECTION

The TDA6101BQ incorporates protection diodes against CRT flashover discharges that clamp the cathode output voltage until maximum $V_{DDH} + V_{diode}$. To limit the diode current, an external 1 kΩ carbon high-voltage resistor in series with the cathode output and a 2 kV spark gap are required. For this resistor value the ground connection for the CRT must be connected to the main printed-circuit board. This addition produces an increase in the 'rise' and 'fall' times of approximately 5 ns and a decrease in the overshoot of approximately 3%.

V_{DDH} – GND must be decoupled:

(a) With a capacitor > 20 nF with good HF behaviour (e.g. foil). This capacitor must be placed as close as possible to pin 6 and pin 4, definitely within 5 mm.

(b) With a capacitor > 10 µF on the picture tube base print (common for three output stages).

V_{DDL} – GND must be decoupled with a capacitor > 20 nF with good HF behaviour (e.g. ceramic). This capacitor must be placed as close as possible to pin 2 and pin 4, definitely within 10 mm.

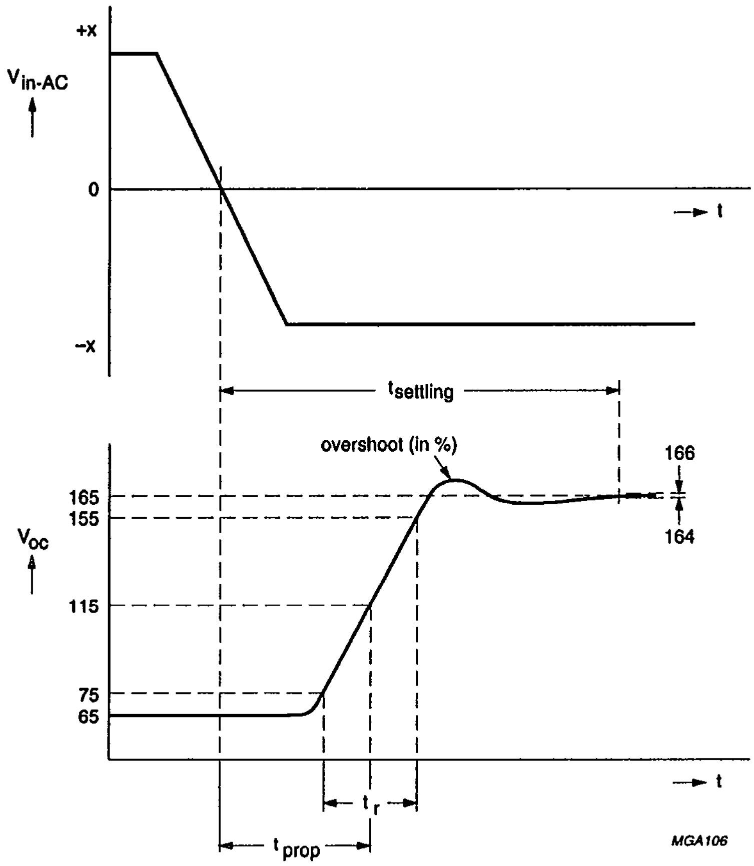


Fig.5 Output rising edge as a function of input signal.

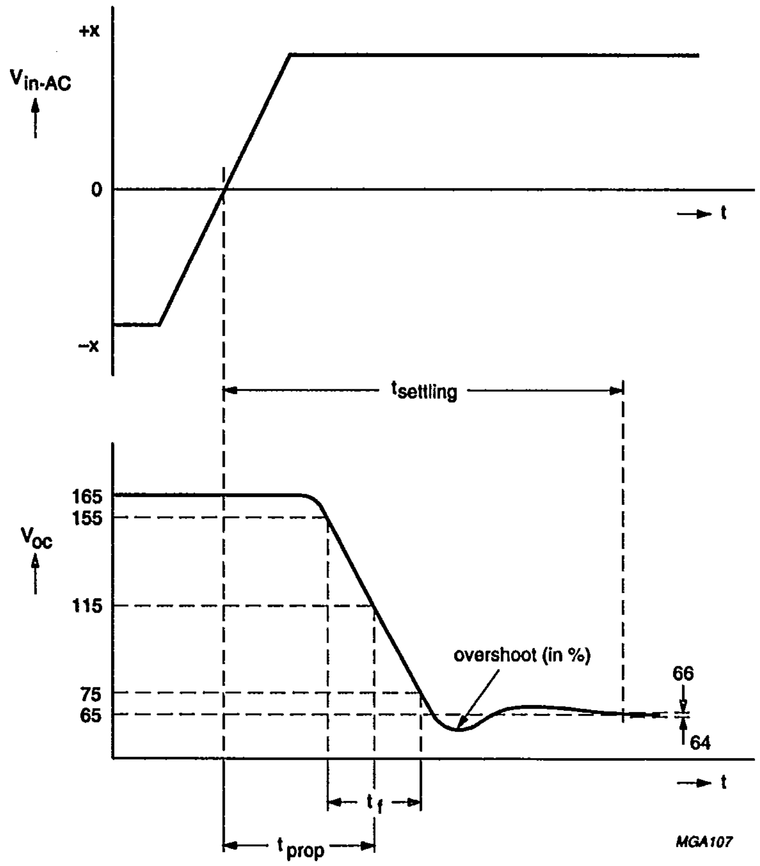
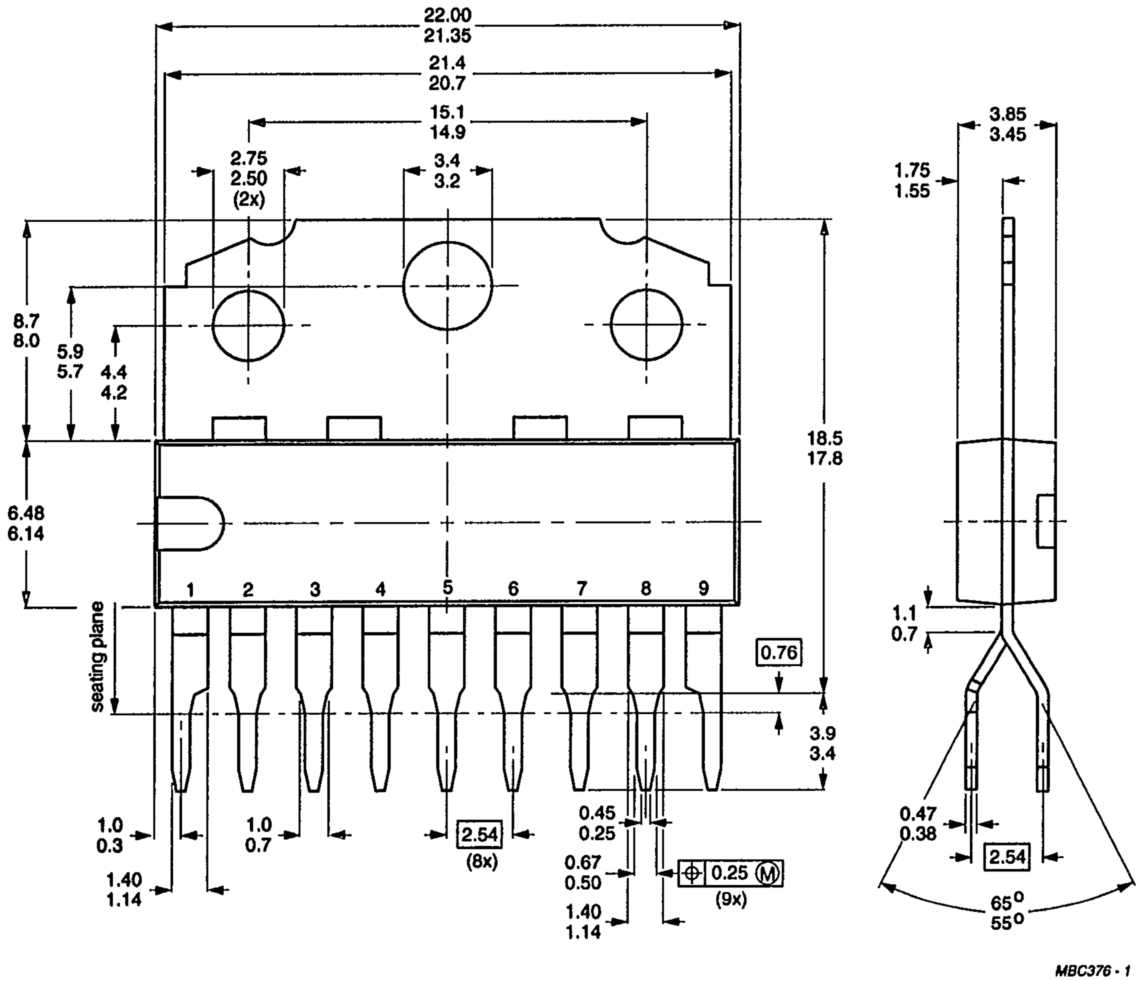


Fig.6 Output falling edge as a function of input signal.

PACKAGE OUTLINE



Dimensions in mm.

Fig.7 9-lead SIL-bent-to-DIL; plastic medium-power (SOT111BE).

SOLDERING

Plastic single in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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