National Semiconductor Corporation

microCMOS

TP3150 Time Slot Assignment Circuit

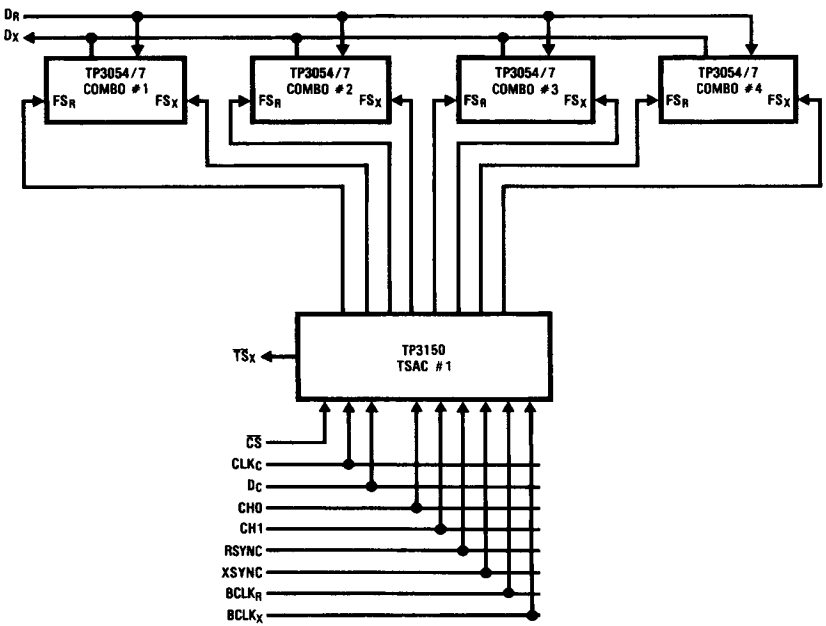
General Description

The TP3150 is a monolithic CMOS logic circuit designed to generate transmit and receive frame synchronization pulses for up to 4 COMBO™ CODEC/Filters. Each frame sync pulse may be independently assigned to a time slot in a frame of up to 32 time slots. Assignments are controlled by loading in an 8-bit word via a simple serial interface port. This control interface is compatible with that used on the TP3020/TP3021 and 2910/2911 CODECs, enabling an easy upgrade to COMBO CODEC/Filters to be made.

Features

- Controls up to 4 COMBO CODEC/Filters
- Independent transmit and receive time slot assignments
- Asynchronous transmit and receive clocks
- Up to 32 time slots per frame
- Serial control interface compatible with TP3020/TP3021 CODECs
- LS TTL and CMOS compatible inputs
- 5 mW, 5V operation

Typical Application



TL/H/8804–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{CC} Relative to GND	7V
Voltage at Any Input or Output	V_{CC} + 0.3V to GND −0.3V
Operating Temperature Range	−25°C to +125°C
Storage Temperature Range	−65°C to +150°C
Maximum Lead Temperature (Soldering, 10 seconds)	300°C

ESD rating to be determined

DC Electrical Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5.0V to ±5%, T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/ or product design and characterization. Typicals specified at V_{CC} = +5.0V, T_A = 25°C.

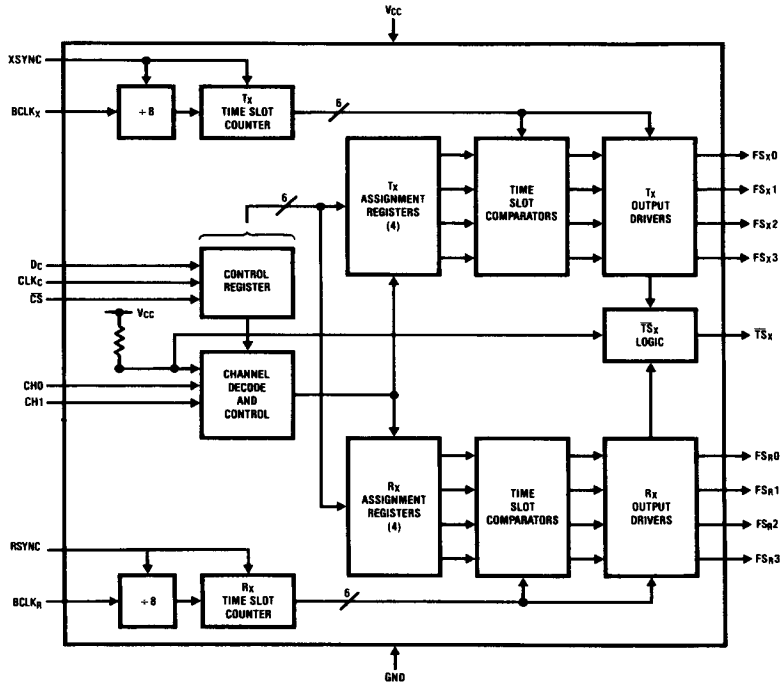
Parameter	Conditions	Min	Typ	Max	Units
Input Voltage Levels					
V_{IH}, Logic High		**2.0**			V
V_{IL}, Logic Low				**0.7**	V
Input Currents					
All Inputs Except MODE	$V_{IL} < V_{IN} < V_{IH}$	**−1**		**1**	μA
MODE	V_{IN} = 0V	**−100**			μA
Output Voltage Levels					
V_{OH}, Logic High	FS_X and FS_R Outputs, I_{OH} = 3 mA	2.4			V
V_{OL}, Logic Low	FS_X and FS_R Outputs, I_{OL} = 5 mA			0.4	V
	$\overline{TS}_X$ Output, I_{OL} = 5 mA			**0.4**	V
Power Dissipation Operating Current	BCLK = 2.048 MHz, All Outputs Open-Circuit		1	**1.5**	mA

Timing Specifications

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5.0V to ±5%, T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/ or product design and characterization. Typicals specified at V_{CC} = +5.0V, T_A = 25°C.
All timing parameters are measured at V_{OH} = 2.0V and V_{OL} = 0.7V.
See Definitions and Timing Conventions section for test methods information.

Symbol	Parameter	Conditions	Min	Max	Units
t_{PC}	Period of Clock	$BCLK_X$, $BCLK_R$, CLK_C	**480**		ns
t_{WCH}	Width of Clock High	$BCLK_X$, $BCLK_R$, CLK_C	**160**		ns
t_{WCL}	Width of Clock Low	$BCLK_X$, $BCLK_R$, CLK_C	**160**		ns
t_{SDC}	Set-Up Time from D_C to CLK_C		**50**		ns
t_{HCD}	Hold Time from CLK_C to D_C		**50**		ns
t_{SCC}	Set-Up Time from $\overline{CS}$ to CLK_C		**30**		ns
t_{HCC}	Hold Time from CLK_C to $\overline{CS}$		**100**		ns
t_{SCHC}	Set-Up Time from Channel Select to CLK_C		**50**		ns
t_{HCHC}	Hold Time from CLK_C to Channel Select		**50**		ns
t_{DBF}	Delay Time from $BCLK_X$ or $BCLK_R$ Low to $FS_{X/R}$ 0–3 High or Low	C_L = 50 pF		**100**	ns
t_{HSYNC}	Hold Time from $BCLK_X$, $BCLK_R$ to Frame Sync		**50**		ns
t_{SSYNC}	Set-Up Time from Frame Sync to $BCLK_X$, $BCLK_R$		**100**		ns
t_{DTL}	Delay from $BCLK_X$ or $BCLK_R$ High to $\overline{TS}_X$ Low	C_L = 50 pF		**140**	ns
t_{DTH}	Delay from $BCLK_X$ or $BCLK_R$ Low to $\overline{TS}_X$ High	R_L = 1k to V_{CC}	**30**	**140**	ns
t_{RC}, t_{FC}	Rise and Fall Time of Clock	$BCLK_X$, $BCLK_R$, CLK_C		50	ns

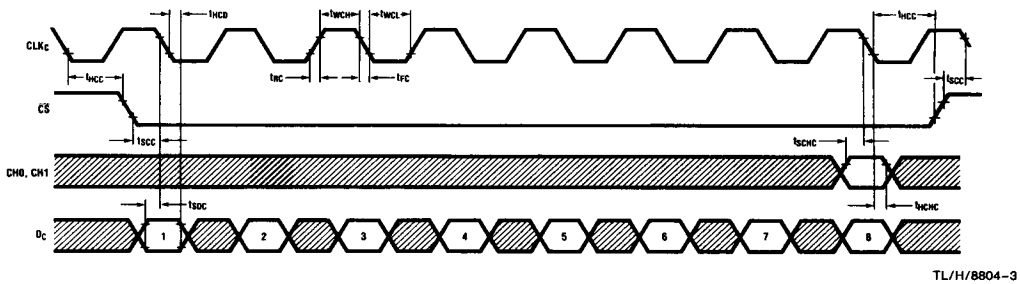
Block Diagram



TL/H/8804–2

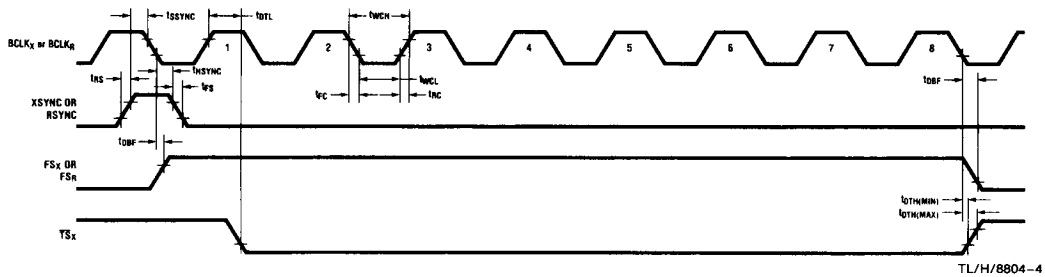
Timing Diagrams

Control Interface



TL/H/8804–3

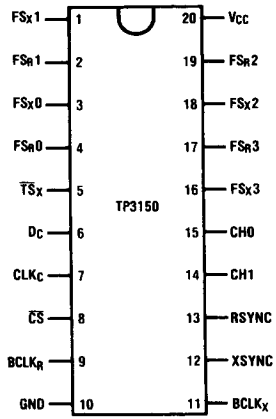
Output



TL/H/8804–4

Connection Diagram

Dual-In-Line Package



TL/H/8804–5

Top View

Order Number TP3150J or TP3150N
See NS Package Number J20A or N20A

Pin Descriptions

Symbol	Description	Symbol	Description
FS_X1	A conventional CMOS frame sync output which is normally low, and goes active-high for 8 cycles of BCLK when a valid transmit time slot assignment is made.	$BCLK_X$	The transmit bit clock input, which should run at the same rate as that for the CODEC/Filter COMBO, and controls four FS_X outputs.
FS_R1	A conventional CMOS frame sync output which is normally low, and goes active-high for 8 cycles of BCLK when a valid receive time slot assignment is made.	XSYNC	The transmit TS0 sync pulse input. Must be synchronous with $BCLK_X$.
FS_X0	A transmit frame sync output similar to pin 1.	RSYNC	The receive TS0 sync pulse input. Must be synchronous with $BCLK_R$.
FS_R0	A receive frame sync output similar to pin 2.	CH1	The input for the next significant bit of the channel select word.
$\overline{TS}_X$	An open-drain N-channel output which is normally high impedance but pulls low during any active transmit time slot.	CH0	The input for the LSB of the channel select word, which defines the frame sync output affected by the following control word.
D_C	The input for an 8-bit serial control word. $\overline{X}$ is the first bit clocked in.	FS_X3	A transmit frame sync output similar to pin 1.
CLK_C	The clock input for the control interface.	FS_R3	A receive frame sync output similar to pin 2.
$\overline{CS}$	The active-low chip select for the control interface.	FS_X2	A transmit frame sync output similar to pin 1.
$BCLK_R$	The receive bit clock input, which should run at the same rate as that for the CODEC/Filter COMBO, and controls four FS_R outputs.	FS_R2	A receive frame sync output similar to pin 2.
GND	The 0V ground connection to the device.	V_{CC}	The positive supply to the device. 5V ±5%.

Functional Description

OPERATING MODES

The TP3150 control interface requires an 8-bit serial control word which is compatible with the TP3020/TP3021 and 2910/2911 CODECs. Two bits, $\overline{X}$ and $\overline{R}$, define which of the two groups of frame sync outputs, FS_X0 to FS_X3 or FS_R0 to FS_R3, is affected by the control word, and a 6-bit assignment field specifies the selected time slot, from 0 to 31. A frame sync output is active-high for one time slot, which is always 8 cycles of $BCLK_X$ or $BCLK_R$. A frame may consist of any number of time slots up to 32. If a timeslot is assigned which is beyond the number of time slots in a frame, the FS_X or FS_R output to which it was assigned will remain inactive. Pin 13 is the RSYNC input which defines the start of each receive frame, and the four outputs, FS_R0-FS_R3, are assigned with respect to RSYNC. Pin 12 is the XSYNC input defines the start of each transmit frame and outputs FS_X0-FS_X3 are assigned with respect to XSYNC. XSYNC may have any phase relationship with RSYNC. Inputs CH0 and CH1 select the channel, from 0 to 3 (see Table Ia).

For asynchronous systems the TP3150 provides independent clocking and synchronization for the transmit and receive time slot counters. $BCLK_X$ and XSYNC control four outputs and $BCLK_R$ and RSYNC control four FS_R outputs.

POWER-UP INITIALIZATION

During power-up, all frame sync outputs, FS_X0-FS_X3 and FS_R0-FS_R3, are inhibited and held low. No outputs will go active until a valid time slot assignment is made.

LOADING CONTROL DATA

During the loading of control data, the binary code for the selected channel must be set on inputs CH0 and CH1 (see Table I).

Control data is clocked into the D_C input on the falling edges of CLK_C while $\overline{CS}$ is low.

A new time slot assignment is transferred to the selected assignment register on the high going transition of $\overline{CS}$. The new assignment is re-synchronized to the system clock such that the new FS output pulses will start at the next complete valid time slot after the rising edge of $\overline{CS}$.

TIME SLOT COUNTER OPERATION

At the start of TS0 of each transmit frame, defined by the first falling edge of $BCLK_X$ after XSYNC goes high, the transmit time slot counter is reset to 000000 and begins to increment once every 8 cycles of $BCLK_R$. Each count is compared with the 4 transmit assignment registers and, on finding a match, a frame sync pulse is generated at that FS_X output.

Similarly, the first falling edge of $BCLK_R$ after RSYNC goes high defines the start of receive TS0, and outputs FS_R0-FS_R3 are generated with respect to TS0 when the receive time slot counter matches the appropriate receive assignment register.

$\overline{TS}_X$ OUTPUT

This output pulls low whenever any FS_X output pulse is being generated. At all other times it is open-circuit, allowing the $\overline{TS}_X$ outputs of a number of TSACS to be wire-ANDed together with a common pull-up resistor. This signal can be used to control the TRI-STATE® enable input of a line driver to buffer the transmit PCM bus from the CODEC/Filters to the backplane.

TABLE I. Control Codes (TP3020/TP3021 Compatible)

$\overline{X}$	$\overline{R}$	T5	T4	T3	T2	T1	T0

$\overline{X}$ is the first bit clocked into the D_C input.

Control Data Format

T5	T4	T3	T2	T1	T0	Time Slot
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
						:
0	1	1	1	1	0	30
0	1	1	1	1	1	31
1	X	X	X	X	X	(Note 1)

CH1	CH0	Channel Selected
0	0	Assign to FS_X0 and/or FS_R0
0	1	Assign to FS_X1 and/or FS_R1
1	0	Assign to FS_X2 and/or FS_R2
1	1	Assign to FS_X3 and/or FS_R3

$\overline{X}$	$\overline{R}$	Action
0	0	Assign time slot to both selected FS_X and FS_R
0	1	Assign time slot to selected FS_X only
1	0	Assign time slot to selected FS_R only
1	1	Disable both selected FS_X and FS_R

Note 1: When T5 = 1 then the appropriate FS_X or FS_R output is inactive.

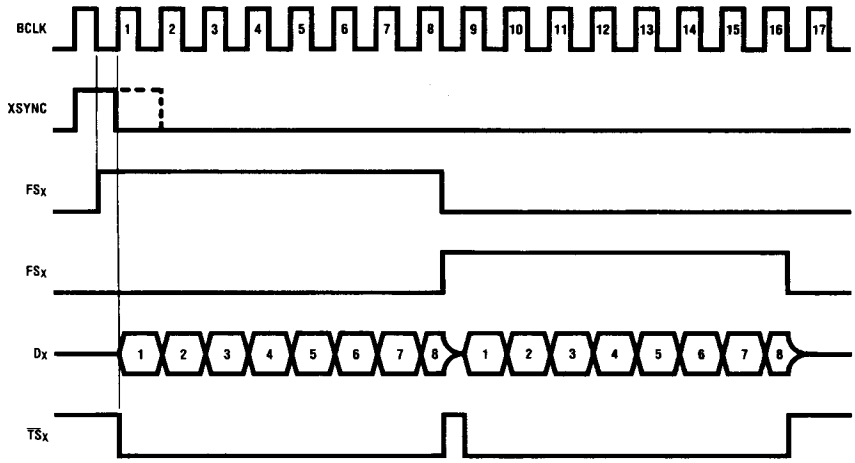
Applications Information

A combination of the TP3150 TSAC and any CODEC/Filter COMBO from the TP3052/3/4/7 or TP3064/7 series will result in data timing as shown in *Figure 1*. Although the FS_X output pulse goes high before $BCLK_X$ goes high, the D_X output of the combo remains in the TRI-STATE mode until both are high. The eight bit period is shortened to prevent a bus clash, just as it is on the TP3020/1 CODECs.

Alternatively, eight full-length bits can be obtained by inverting the BCLK to the combo devices, thereby aligning rising edges of BCLK and $FS_{X/R}$.

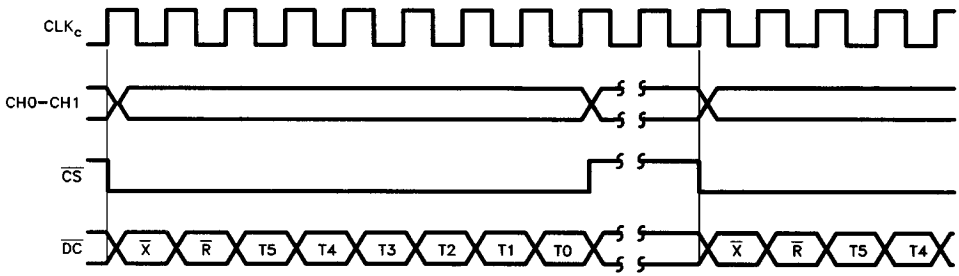
Figure 2 shows typical timing for the control data interface.

Figure 3 shows the digital interconnections of a typical line card application.



TL/H/8804–6

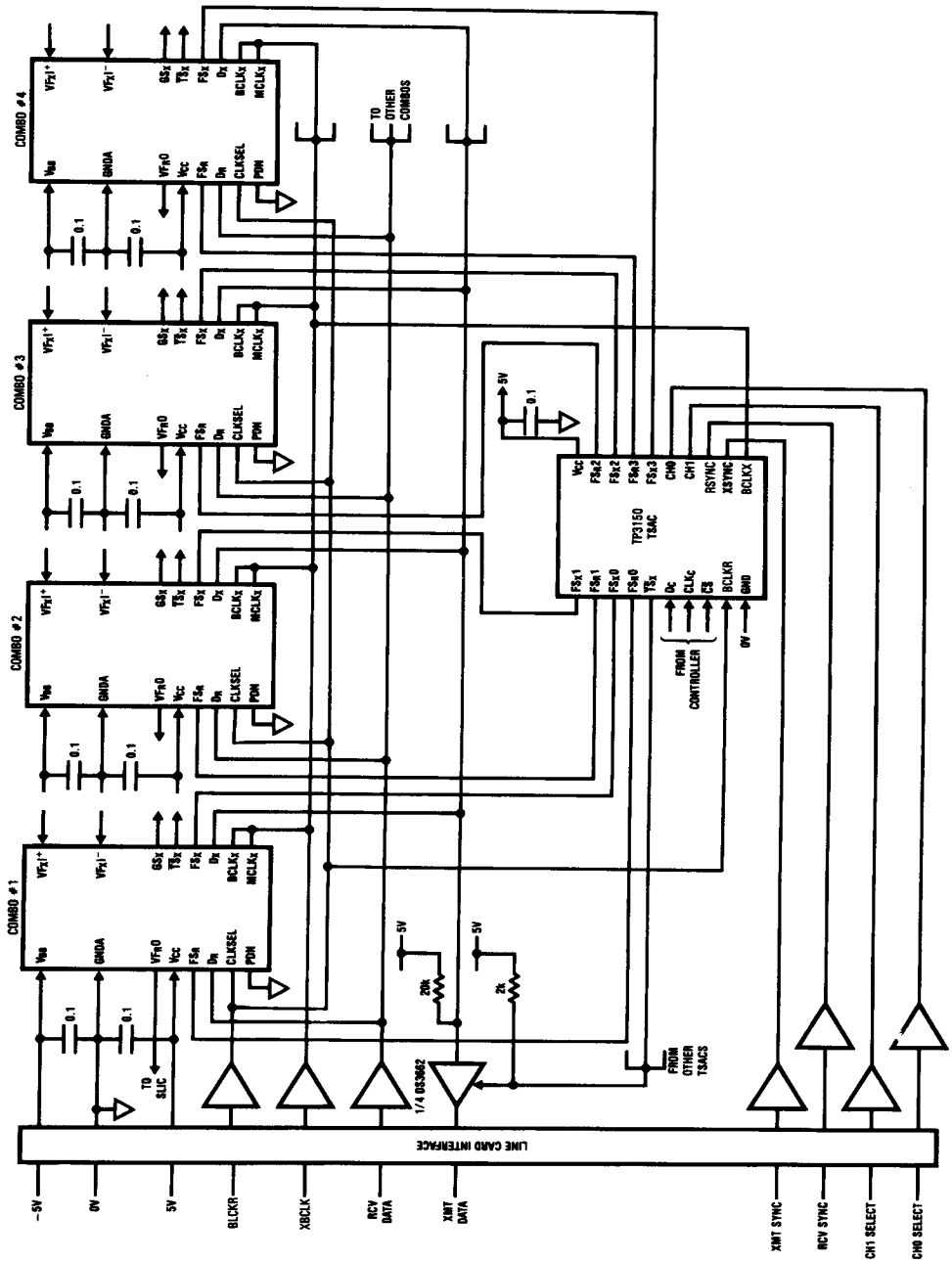
FIGURE 1. Transmit Data Timing



TL/H/8804–7

FIGURE 2. Control Data Timing

Application Information (Continued)



TL/H/8804–8

FIGURE 3. Digital Interconnections on a Typical Synchronous Line Card