ABSOLUTE MAXIMUM RATINGS	
+Vs	+6.2V
−Vs	−9V
Analog Input Voltage Range[1]	+Vs to −Vs
Reference Input Voltage Range[1]	+Vs to −Vs
Digital Input Voltage Range (Pins 2-27)[2]	+Vs +0.3V, GND −0.3V
Power Dissipation	500 mW at 70°C

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±5V Supplies unless otherwise noted.

ANALOG INPUT CHARACTERISTICS	
Type Analog Input	Differential
Zero Input Reading, max. (Octal Reading)[3]	$+0000_8$
Ratiometric Reading, max. (Octal Reading)[4]	4000_8
Input Leakage Current, max. (V_{IN} = 0V)	10 pA
Common Mode Rejection Ratio[13]	86 dB
Input Common Mode Voltage Range, min.	−Vs plus 1.5V
max.	+Vs minus 1.0V

DIGITAL INPUT	
Control I/O Pull-up Current[5]	5 μA
Control I/O Loading, max.[6]	50 pF
Input Voltage Range[7] (Pins 18-21, 26, 27)	
High, min.	2.5V
Low, max.	1V
Input Pull-up Current[8] (Pins 26, 27)	5 μA
(Pins 17, 24)	25 μA
Input Pull-down Current (Pin 21)[9]	5 μA
Mode Input Pulse Width, min.	50 nsec.

OUTPUT CHARACTERISTICS	
Output Voltage,[10] high min.	3.5V at 100 μA
low max.	0.4V at 1.6 mA
Output Leakage Current, max. (Pins 3-16)	1 μA
Reference Output Voltage, min.	−2.4V
max.	−3.2V
Oscillator Output Current,[11] high	1 mA
low	1.5 mA
Buffered Oscillator Output Current,[11] high	2 mA
low	5 mA

PERFORMANCE	
Resolution	12-bits, plus sign and overrange
Non-Linearity, max.	±1 Count
Roll-over Error[12]	±1 Count
Noise, peak-to-peak[14]	15 μV
Zero Drift, max.	1 μV/°C
Scale Factor Tempco, max.[15]	5 ppm/°C
Reference Output Tempco[16]	80 ppm/°C

FOOTNOTES:

1. Positive or negative input. Input voltage can exceed the supply voltage provided the input current is limited to 100 μA.
2. It is recommended that no inputs from sources other than the devices power supply be applied to the device before its power supply is established, and that in multiple supply systems, the supply to the device be activated first. This will avoid destructive device latchup.
3. Vin = 0.0V, Full-Scale = 409.6 mV.
4. Vin = Vref = 204.8 mV.
5. Pins 18, 19, 20. Vout = +V_s minus 3V. Mode input at ground.
6. $\overline{HBEN}$ (Pin 19) $\overline{LBEN}$ (pin 18).
7. With respect to ground.
8. Vout = +V_s minus 3V.
9. Vout = Ground plus 3V.
10. Pins 2 through 16, 18, 19 and 20.
11. Vout = 2.5V.
12. Difference in reading for equal positive and negative inputs near full-scale.
13. Vcm ± 1V, Vin = 0V. Full-scale = 409.6 mV.
14. Not exceeded 95% of the time.
15. Vin = 408.9 mV. External reference tempco = 0 ppm/°C.
16. 25 kΩ between +V_s and reference output.
17. Vin = 0. Crystal oscillator 3.58 MHz. Pins 2-21, 25, 26, 27, 29, open.

POWER REQUIREMENTS	
Supply Voltage	±5V dc
Supply Current (+Vs to GND.) max.[17]	1.5 mA
Supply Current (+Vs to −Vs) max.[17]	1.5 mA

PHYSICAL/ENVIRONMENTAL	
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +125°C
Lead Temperature (soldering 60 sec.)	300°C
Package	40 Pin Plastic DIP

1

TECHNICAL NOTES

1. Differential voltages from 1.0V below the positive supply to 1.5V above the negative supply can be applied to the device's input. In this range, the system has a typical CMRR of 86 dB. However, since the integrator also swings with the common mode voltage, care must be taken to assure that the integrator output does not saturate. To avoid this, the integrator swing can be reduced to less than the recommended 4V full scale with some loss of accuracy. The integrator output can swing to within 0.3V of either supply without loss of linearity.
2. The buffer amplifier and integrator have a Class A output stage with 100 μA of quiescent current. They supply 20 μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For a full-scale range of 4.096V, 200 kΩ is optimum; for 409.6 mV, 20 kΩ should be used. For other values of full-scale: $R_{INT} = V_{FS}/20\ \mu A$.
3. The integrating capacitor should be selected to give the maximum integrator output voltage swing without saturating the integrator (approximately 0.3V from either supply). The value for the integrating capacitor is given by the following equation: $C_{INT} = (2048 \times T_{CLOCK})\ (20\ \mu A)$/Integrator V_{OUT} Swing. The integrating capacitor should be selected to have low dielectric absorption to prevent roll-over errors. Many types of capacitors are adequate for this application, however, polypropylene capacitors will give undetectable errors up to +70°C.
4. The value of the auto zero capacitors depends upon the requirements of the applications. For example, for a full-scale voltage range of 409.6 mV, where noise is a major consideration and the integrating resistor is very small, a value of C_{AZ} twice C_{INT} is optimum. Similarly, for a full-scale range of 4.096V, where recovery is more important than noise, a value of C_{AZ} equal to half C_{INT} is recommended.
5. The analog input required to generate a full-scale output of 4096 counts is $V_{IN} = 2\ V_{REF}$. Thus, for a normalized scale, a reference of 2.048V should be used for a 4.096V full-scale, and 204.8 mV for a 0.4096V full-scale. However, in many applications where the A/D is sensing the output from a transducer, a scale factor other than the unity between the absolute output voltage to be measured and a desired digital output will exist. For example, in a weighing system, a full-scale reading may be desired with 0.682V from the transducer. In this case, rather than dividing the input down to 409.6 mV, it should be applied directly and a reference voltage of 0.341V should be used. Values for R_{INT} and C_{INT} would be 34K and 0.15 μF.

6. The stability of the reference is a major factor in the overall absolute accuracy of the converter. It is recommended that an external high quality reference be used where the ambient temperature is not controlled or where high-accuracy absolute measurements are being made.

If using the internal reference, REF OUT (Pin 29) should be connected to −REF IN (Pin 39), and +REF IN should be connected to the wiper of a precision trimpot between REF OUT and $+V_S$. (See typical connections.)

PIN DESCRIPTION

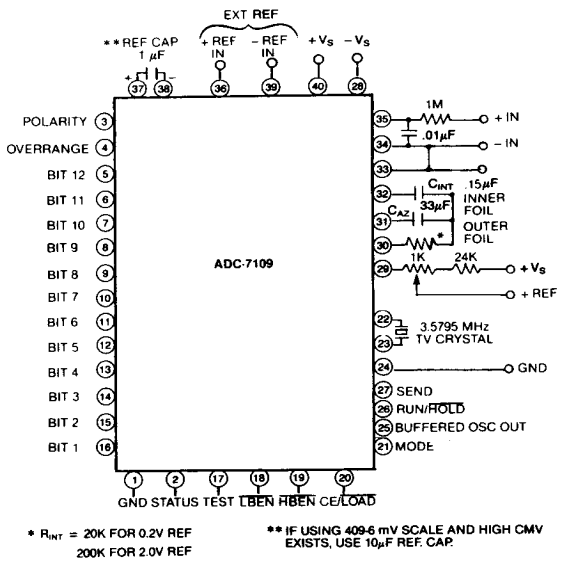
INPUT/OUTPUT CONNECTION AND DESCRIPTION

PIN	FUNCTION	DESCRIPTION
1	DIGITAL GROUND	Ground return for all digital logic.
2	STATUS	Output — High during integrate and deintegrate until data is latched. — Low when analog section is in Auto-Zero configuration.
3	POLARITY	High for Positive Input
4	OVER-RANGE	High if Overranged
5	Bit 12 (MSB)	Data Bits. Three-State Output
6	Bit 11	
7	Bit 10	
8	Bit 9	
9	Bit 8	
10	Bit 7	
11	Bit 6	
12	Bit 5	
13	Bit 4	
14	Bit 3	
15	Bit 2	
16	Bit 1 (LSB)	
17	TEST	Input High — Normal Operation. Input Low — Forces all bit outputs high, and disables internal clock. When returned high and 1 clock pulse is input, the counter outputs will enter negative state. Must be tied high if not used. Note: This input is used for test purposes only.
18	$\overline{\text{LBEN}}$	Low Byte Enable — With Mode (Pin 21) low, and $\overline{\text{CE/LOAD}}$ (Pin 20) low, taking this pin low activates low order byte outputs B1-B8.
19	$\overline{\text{HBEN}}$	High Byte Enable — With Mode (Pin 21) low, and $\overline{\text{CE/LOAD}}$ (Pin 20) low, taking this pin low activates high order byte outputs B9-B12, polarity and overrange outputs.
20	$\overline{\text{CE/LOAD}}$	Chip Enable Load — With Mode (Pin 21) low, $\overline{\text{CE/LOAD}}$ serves as a master output enable. When high, B1-B12, polarity and overrange outputs are disabled. — With Mode (Pin 21) high, this pin serves as a load strobe used in handshake mode.

PIN	FUNCTION	DESCRIPTION
21	MODE	Input Low — Direct output mode where $\overline{\text{CE/LOAD}}$ (Pin 20), $\overline{\text{HBEN}}$ (Pin 19) and $\overline{\text{LBEN}}$ (Pin 18) act as inputs directly controlling byte outputs. Input Pulsed High — Causes immediate entry into handshake mode. Input High — Enables $\overline{\text{CE/LOAD}}$ (Pin 20), $\overline{\text{HBEN}}$ (Pin 19) and $\overline{\text{LBEN}}$ (Pin 18) as outputs, handshake mode will be entered and will be valid at the end of conversion.
22	OSC IN	Oscillator Input
23	OSC OUT	Oscillator Output
24	OSC SELECT	Oscillator Select — Input high configures OSC IN, OSC OUT, BUF OSC OUT as RC oscillator — clock will be same phase and duty cycle as BUF OSC OUT. — Input low configures OSC IN, OSC OUT for crystal oscillator — clock frequency will be 1/58 of frequency at BUF OSC OUT.
25	BUF OSC OUT	Buffered Oscillator Output
26	RUN/$\overline{\text{HOLD}}$	Input High — Conversions continuously performed every 8192 clock pulses. Input Low — Conversion in progress completed, converter will stop in Auto-Zero 7 counts before integrate.
27	SEND	Input — Used in handshake mode to indicate ability of an external device to accept data. Must be tied high if not used.
28	$-V_S$	Negative Supply Voltage — Nominally −5V with respect to GND (Pin 1).
29	REF OUT	Reference Voltage Output — Nominally, 2.8V down from $+V_S$ (Pin 40).
30	BUFFER	Buffer Amplifier Output
31	AUTO-ZERO	Auto-Zero Mode Select
32	INTEGRATOR	Integrator Output
33	COMMON	Analog Common — System is auto-zeroed to COMMON.
34	− ANALOG IN	Negative Differential Analog Input
35	+ ANALOG IN	Positive Differential Analog Input
36	+ REF IN	Positive Differential Reference Input
37	+ REF CAP	Positive Reference Capacitor Connection
38	− REF CAP	Negative Reference Capacitor Connection
39	− REF IN	Negative Differential Reference Input
40	$+V_S$	Positive Supply Voltage — Nominally +5V with respect to GND (Pin 1).

TIMING AND CONNECTION

TYPICAL CONNECTION
(TEST CIRCUIT)

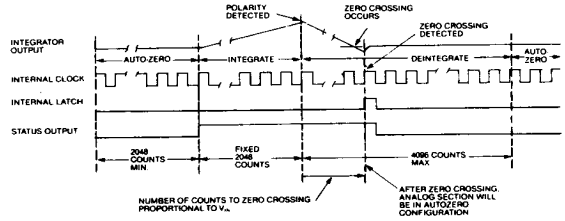


* R_{INT} = 20K FOR 0.2V REF
200K FOR 2.0V REF

** IF USING 409-6 mV SCALE AND HIGH CMV EXISTS, USE 10μF REF. CAP.

NOTES: INPUTS SHOULD SWING FROM GND TO +Vs FOR MINIMUM POWER CONSUMPTION. TTL DRIVEN INPUT SHOULD HAVE 3-5KΩ PULL-UP RESISTORS ADDED FOR MAXIMUM NOISE IMMUNITY.

CONVERSION TIMING



THE CONVERSION PROCESS

There are three steps in the conversion process for the ADC-7109:

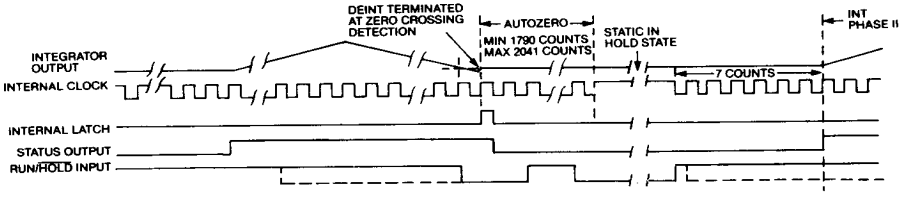
1. Auto Zero
2. Signal Integrate
3. Deintegrate

In the auto zero step, the high and low inputs are internally disconnected from the pins and shorted to analog common. At this point, the reference capacitor is charged to the reference voltage. Then a feedback loop is closed to charge the autozero capacitor (C_{AZ}) which compensates for offset voltages in the buffer amplifier, integrator and comparator. The offset referred to the input is less than 10 μV.

In the signal integrate step, the auto-zero loop is opened and the inputs are connected (internally) back to the external pins. At this point, the differential signal between the inputs is integrated for a fixed time of 2048 clock periods. Upon completion of this phase, the polarity of the integrated signal is determined.

The deintegrate step is the final phase. Here, the negative input is connected to analog common and the positive input is connected across the previously charged reference capacitor, which returns the integrator output to the zero crossing (from auto-zero step) with a fixed slope. Thus, the time for the output to return to zero is proportional to the input signal.

RUN/$\overline{\text{HOLD}}$ OPERATION



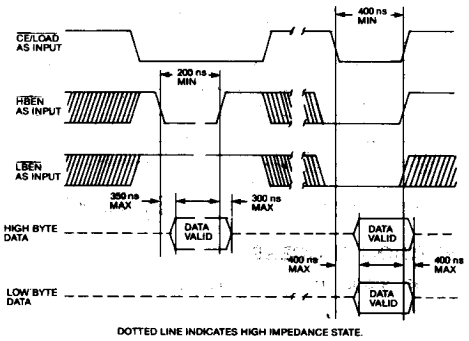
NOTE

The conversion rate is determined by the clock rate (8192 clock periods per cycle) with the RUN/$\overline{\text{HOLD}}$ input left open or connected to +Vs.

If RUN/$\overline{\text{HOLD}}$ goes low any time during the Deintegrate phase after zero crossing has occurred, the deintegrate phase will terminate and the converter will go to auto zero. This feature can be used to save time in deintegrate after zero crossing.

TIMING AND OPERATION

DIRECT MODE OUTPUT



With MODE input low, the data outputs (bits 1-8 low order byte, bits 9-12, polarity and overrange high order byte) are accessible under control of the byte and chip enable terminals as inputs. These three inputs are active low, and are provided with pullup resistors to ensure an active high level when left open.

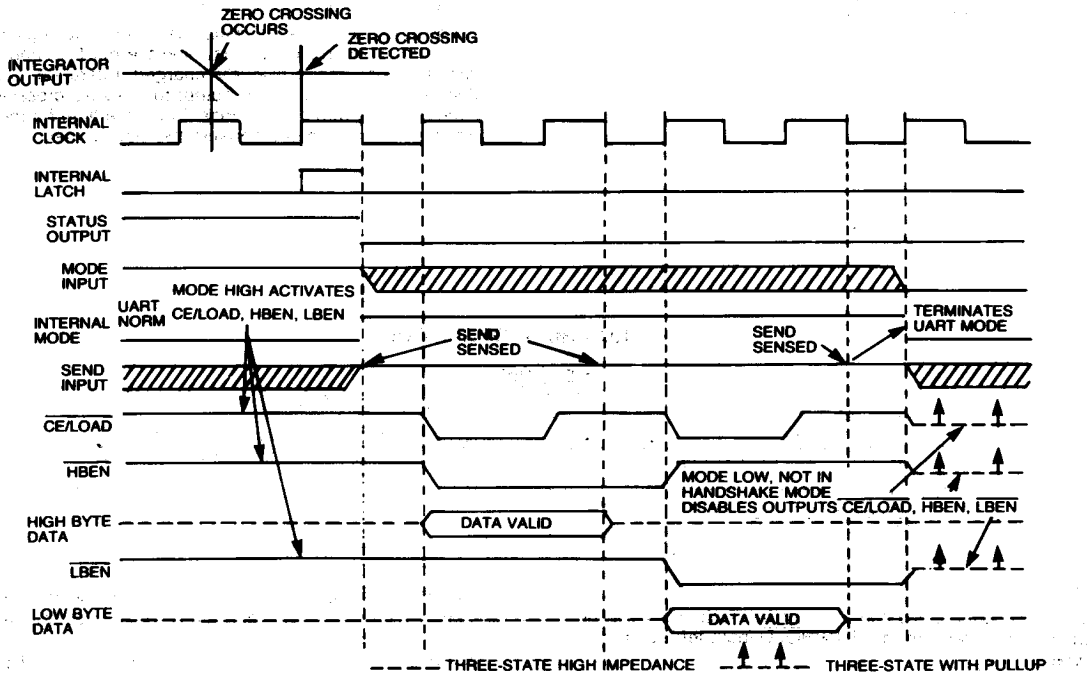
Note that the control inputs are asynchronous with respect to the internal clock—the data may be accessed at any time. Therefore it is possible to access the data while it is being updated which could result in scrambled output data. To prevent this, the access of data should be synchronized with the conversion cycle by monitoring the STATUS output. Data is never updated while STATUS is low.

HANDSHAKE MODE

The handshake mode is an alternative means of interfacing the ADC-7109 to digital systems. In this mode, the A/D actively controls the flow of data rather than passively responding to chip and byte enable inputs and can be interfaced directly to industry standard UART's with no external logic.

The device enters the handshake mode when the MODE input is held high after new data has entered the output latches at the end of every conversion performed. (See timing diagrams.) The MODE input may also be used to trigger entry into the handshake mode on demand. Any time during the conversion cycle,

HANDSHAKE TIMING WITH SEND HELD POSITIVE



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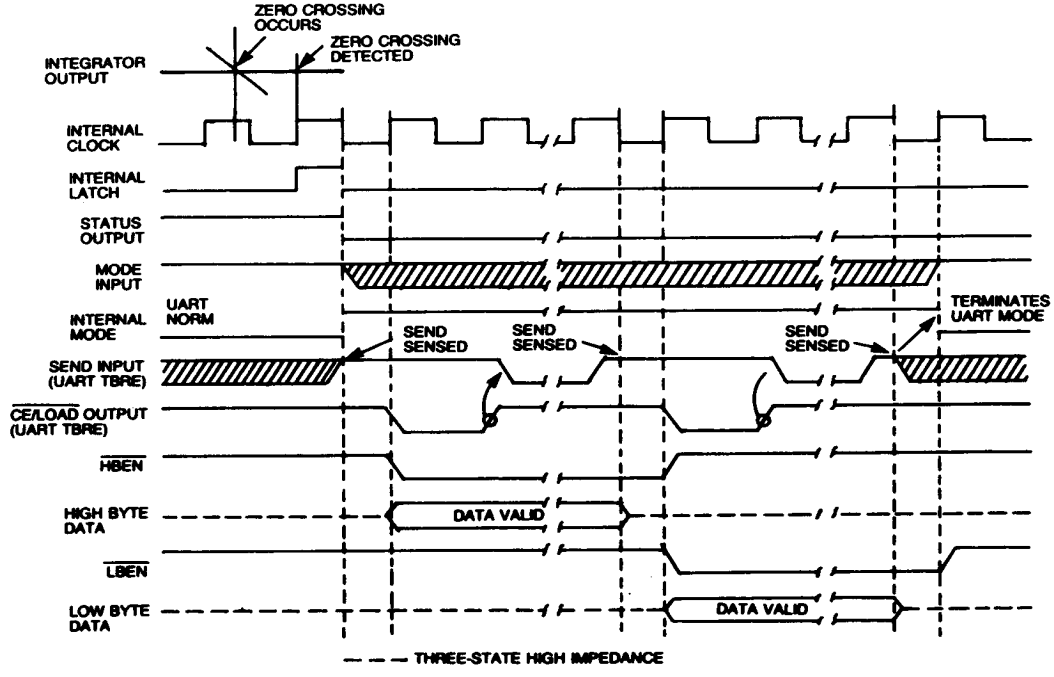
TIMING AND OPERATION (CONT)

the MODE input can be pulsed from low to high and the device will immediately enter the handshake mode. If the pulse occurs while new data is being stored, entry into handshake mode will be delayed until the data is stable. While in the handshake mode, the MODE Input will be ignored, and although conversions will still be performed, data updating will be inhibited until the output cycle is completed and clears the handshake mode.

The timing diagram (Handshake With SEND Held High) shows the sequence of the output cycle with the SEND input held high. The handshake mode is entered after the data latch pulse (generated internally). The SEND input (held high) is sensed on the same high to low internal clock edge. On the next low to high clock edge, the $\overline{CE/LOAD}$ and $\overline{HBEN}$ terminals go low enabling the high-order byte (bits 9 through 12, polarity and overrange). The $\overline{CE/LOAD}$ terminal remains low for one clock period only, the data outputs remain active for 1½ clock periods, and the high byte enable remains low for 2 clock periods. Note that the $\overline{CE/LOAD}$ terminals low level or low to high edge may be used as a synchronizing "OUTPUT" signal to ensure valid data, and the byte enable terminal as an "OUTPUT" may be used as a byte identification flag (in the handshake mode only). With the SEND input remaining high, the converter completes the output cycle using $\overline{CE/LOAD}$ and $\overline{LBEN}$ while the low order byte outputs (bits 1 through 8) are activated. When both bytes are sent, the handshake mode is terminated.

1

TYPICAL UART INTERFACE TIMING. (HANDSHAKE MODE)



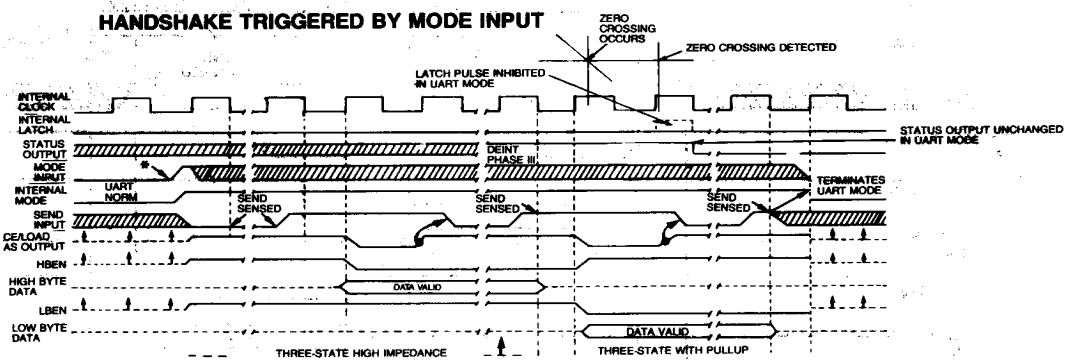
HANDSHAKE MODE (CONT)

The send input may be utilized in delaying portions of the output sequence, or handshake to ensure correct data transfer. The timing diagram (typical UART interface timing) shows the relationships when using the ADC-7109 with an industry standard UART to interface to serial data channels. In this type of interface, the SEND input of the ADC-7109 is driven from the TBRE (Transmitter Buffer Register Empty) output of the UART, and the $\overline{CE/LOAD}$ terminal drives the TBRL (Transmitter Buffer Register Load) input of the UART. The data outputs of the ADC-7109 are paralleled into the Transmitter Buffer Register inputs of the UART.

Assuming the UART Transmitter Buffer Register is empty, the SEND input will be high when the handshake mode is entered after new data is stored. After the SEND input is sensed, the $\overline{CE/LOAD}$ and $\overline{HBEN}$ terminals will go low, activating the high order byte outputs. At the end of 1 clock period, the $\overline{CE/LOAD}$ goes low and the high order byte data is clocked into the UART TBR. The UART TBR output will now go low, which stops the output cycle with the $\overline{HBEN}$ output low, and high order byte outputs active. After the output data has been transferred to the UART transmitter register and cleared the TBR, the TBRE output returns high. On the next clock high to low edge, the high order byte outputs are disabled, and ½ clock pulse later, the $\overline{HBEN}$ terminal returns high, and the $\overline{CE/LOAD}$ and $\overline{LBEN}$ outputs go low, activating the low order byte outputs. The low order byte outputs are similarly clocked into the UART (when $\overline{CE/LOAD}$ returns high) transmitter buffer register and TBRE again goes low. When TBRE returns high, it is sensed on the next high to low clock edge, disabling the data outputs. One half clock pulse later, the handshake mode is cleared, and the $\overline{CE/LOAD}$, $\overline{HBEN}$ and $\overline{LBEN}$ terminals return high and stay active as long as the MODE input stays high.

While the MODE input is high, the ADC-7109 will output the results of every conversion except those completed during a handshake operation. A low to high pulse (edge triggered) on the MODE input will enter the handshake mode and handshake output sequence may be performed on demand.

HANDSHAKE TRIGGERED BY MODE INPUT



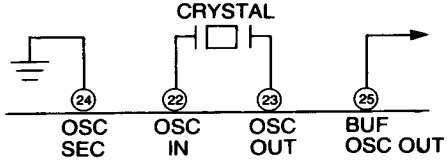
*POSITIVE TRANSITION CAUSES ENTRY INTO HANDSHAKE MODE

TIMING AND OPERATION (CONT)

The timing diagram (Handshake Triggered by Mode Input) shows a handshake output sequence triggered by such an edge. The SEND input is shown as being low when the converter enters the handshake mode. In this case, the entire output sequence is under the control of the SEND input, and the sequence for the high order byte is similar to the low order byte. This timing diagram also shows the output sequence taking longer than the conversion cycle. Note that conversions are still performed with the STATUS output and RUN/$\overline{\text{HOLD}}$ input functioning normally. The only difference is that new data will not be latched when in handshake mode and is therefore lost.

OSCILLATOR[1]

CRYSTAL OSCILLATOR



CRYSTAL OSCILLATOR

Using an inexpensive 3.58 MHz TV crystal provides an integration time given by:

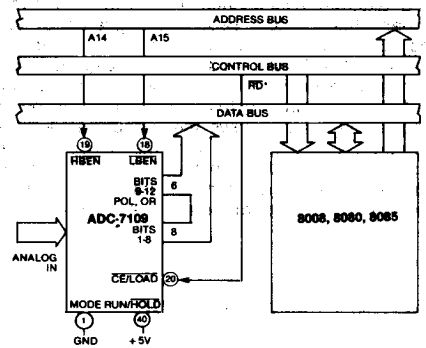
$$T = (2048 \text{ clock periods}) \times \frac{58}{3.58 \text{ MHz}} = 33.18 \text{ msec.}$$

Note this is very close to two 60 Hz periods or 33.33 milliseconds. The error is less than 1% which yields better than 40 dB 60 Hz rejection. The ADC-7109 will operate reliably at conversion speeds of up to 30/second, which corresponds to a clock frequency of 245.8 kHz. See Crystal Oscillator Connection.

To overdrive the internal oscillator, the overdriving signal is applied to the OSCILLATOR INPUT and the OSCILLATOR OUTPUT is left open. The internal clock frequency will be of the same frequency, duty cycle and phase as the input when the OSCILLATOR SELECT input is left open. With the OSCILLATOR SELECT at ground, the clock will be a factor of 58 below the input frequency.

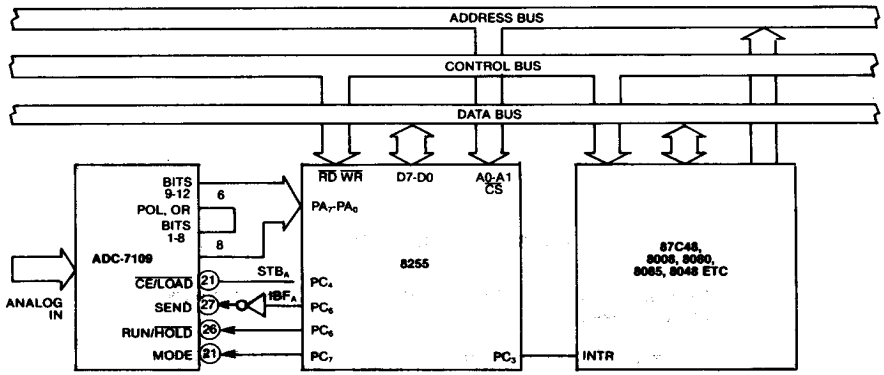
APPLICATIONS

DIRECT INTERFACE TO INTEL 8080/8055



The three-state output capability of the ADC-7109 enables it to be interfaced directly to most microprocessor busses. Note that system timing in this type of interface should be carefully considered to be sure that requirements for set-up and hold times, and minimum pulse widths are met. Drive limitations on long busses should also be considered. This type of interface is favored if the memory peripheral address density is low so that simple address decoding can be used.

HANDSHAKE INTERFACE TO AN INTEL MICROPROCESSOR

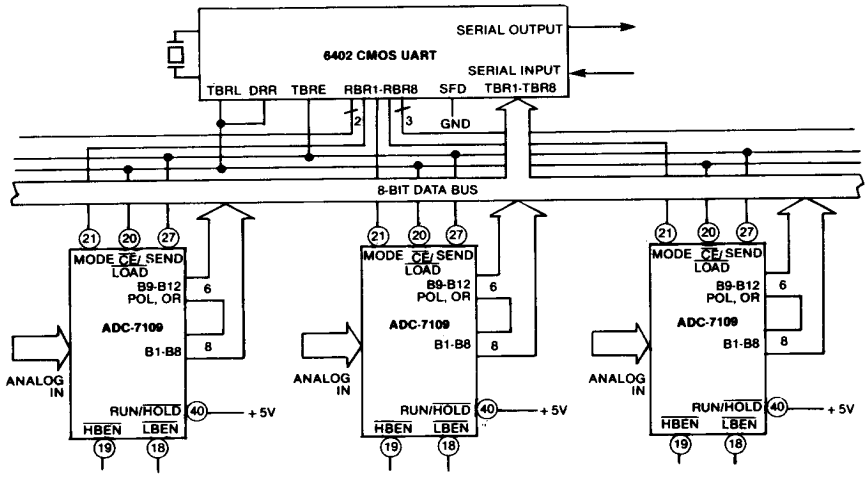


The handshake mode allows ready interface with a wide variety of external devices. The byte enables may be used as byte identification flags or as load enables and external latches may be clocked by the rising edge of the CE/LOAD.

This application shows a handshake interface to Intel microprocessors using an 8255 programmable peripheral interface. Handshake operation with the 8255 is controlled by inverting its Input Buffer Full (IBF) flag to drive the SEND input to the ADC-7109 and using the CE/LOAD to drive the 8255 strobe. The internal control register of the 8255 should be set in MODE 1 for the port used. If the 8255 IBF flag is low and the ADC-7109 is in handshake mode, the next word will be strobed into the port. The strobe will cause IBF (of the 8255) to go high (SEND goes low), which will keep the enabled byte outputs active. The 8255 will generate an interrupt which when executed will result in the data being read. The IBF will be reset low when the byte is read, causing the converter to sequence into the next byte. The MODE input to the ADC-7109 is connected to a control line on the 8255.

The data from every conversion will be sequenced in two bytes in the system, if the output is left high, or tied high separately. Data access must take less time than a conversion. The output sequence can be obtained on demand if this output is forced from low to high and the interrupt may be used to reset the MODE bit. Conversions may be performed on command under software control by driving the RUN/HOLD input to the converter by a bit from the 8255.

MULTIPLEXING SEVERAL CONVERTERS TO A SINGLE UART



In this application, several ADC-7109's are multiplexed to one UART. The word received by the UART (at the UART's RBR outputs when DR is high) is used to select which converter will handshake with the UART. This configuration will allow up to eight ADC-7109's to interface with one UART with no external component requirements.

ORDERING INFORMATION

ACCESSORIES Part Number	Description
ADC-7109	Mating Sockets
TP 1k	Trimming Potentiometers