1 Megabit Static RAM
128K x 8-Bit

Features

- ☐ High speed access times
  Com'l: 20, 25, and 35 ns
  Ind. : 20, 25, and 35 ns
- ☐ Low power operation
  - PDM41024S
    Active: 400 mW (typ.)
    Standby: 150 mW (typ.)
  - PDM41024L
    Active: 350 mW (typ.)
    Standby: 100 mW (typ.)
- ☐ Single +5V (±10%) power supply
- ☐ Packages
  Ceramic LCC - L32

Description

The PDM41024 is a high-performance CMOS static RAM organized as 131,072 x 8 bits. This product is produced in Paradigm's proprietary CMOS technology which offers the designer the highest speed parts. Writing is accomplished when the write enable ($\overline{WE}$) and the chip enable ($\overline{CE1}$) inputs are both LOW and CE2 is HIGH. Reading is accomplished when $\overline{WE}$ and CE2 remain HIGH and $\overline{CE1}$ and $\overline{OE}$ are both LOW.

The PDM41024 operates from a single +5V power supply and all the inputs and outputs are fully TTL compatible. The PDM41024 comes in two versions, the standard power version PDM41024S and a low power version the PDM41024L. The two versions are functionally the same and only differ in their power consumption.

The PDM41024 is available in a 32-pin 450 mil x 550 mil LCC for surface mount applications.

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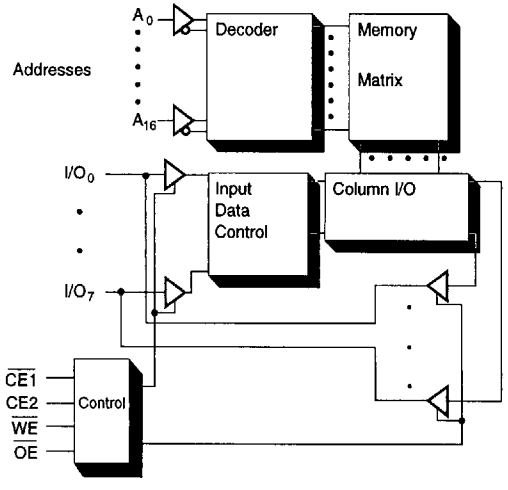
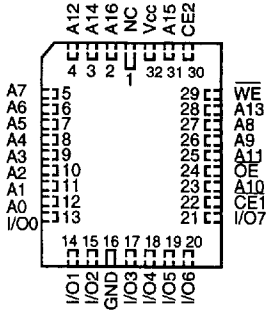
Functional Block Diagram



Pin Configuration

LCC



Truth Table[1]

$\overline{OE}$	$\overline{WE}$	$\overline{CE1}$	CE2	I/O	MODE
X	X	H	X	Hi-Z	Standby
X	X	X	L	Hi-Z	Standby
L	H	L	H	D_{OUT}	Read
X	L	L	H	D_{IN}	Write
H	H	L	H	Hi-Z	Output Disable

NOTE: 1. H = V_{IH}, L = V_{IL}, X = DON'T CARE

Absolute Maximum Ratings [1]

Symbol	Rating	Com'l.	Ind.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
Industrial	Ambient Temperature	–40	25	85	°C
Commercial	Ambient Temperature	0	25	70	°C

DC Electrical Characteristics (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions		PDM41024S		PDM41024L		Unit
				Min.	Max.	Min.	Max.	
I_{LI}	Input Leakage Current	V_{CC} = MAX., V_{IN} = GND to V_{CC}	Com'l	–5	5	–2	2	µA
I_{LO}	Output Leakage Current	V_{CC}= MAX., $\overline{CE}$ = V_{IH}, V_{OUT} = GND to V_{CC}	Com'l	–5	5	–2	2	µA
V_{IH}	Input High Voltage			2.2	6.0	2.2	6.0	V
V_{IL}	Input Low Voltage			–0.5(1)	0.8	–0.5(1)	0.8	V
V_{OL}	Output Low Voltage	I_{OL}= 8 mA, V_{CC} = Min. I_{OL} = 10 mA, V_{CC} = Min.		— —	0.4 0.5	— —	0.4 0.5	V V
V_{OH}	Output High Voltage	I_{OH} = –4 mA, V_{CC} = Min.		2.4	—	2.4	—	V

NOTE: 1. V_{IL}(min) = –3.0V for pulse width less than 20 ns.

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Power Supply Characteristics.

Symbol	Parameter	Power	-20 Com'l., Ind.	-25 Com'l., Ind.	-35(3) ns Com'l., Ind.	Unit
I_{CC}	Operating Current $\overline{CE1}$ = V_{IL}, and CE2 ≥ V_{IH}	S	180	170	165	mA
	V_{CC} = Max., f = f_{MAX} = $1/t_{RC}$ I_{OUT} = 0 mA	L	175	165	160	mA
I_{SB}	Standby Current Current (TTL Level)	S	55	50	45	mA
	$\overline{CE1}$ ≥ V_{IH} or CE2 ≤ V_{IL} V_{CC} = Max., f = f_{MAX} = $1/t_{RC}$	L	45	40	35	mA
I_{SB1}	Full Standby Current $\overline{CE1}$ ≥ V_{HC} or CE2 ≤ V_{LC}	S	10	10	10	mA
	V_{CC} = Max., f = 0 V_{IN} ≥ V_{CC} – 0.2V or ≤ 0.2V	L	5	5	5	mA

NOTES: 1. All Values are maximum guaranteed values.
2. V_{LC} ≤ 0.2V, V_{HC} ≥ V_{CC} – 0.2V
3. This speed grade is available in –55°C to +125°C temperature range only.

Capacitance(1) (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE:1.This parameter is determined by device characterization but is not production tested.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input rise and fall times	5 ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See figures 1 and 2

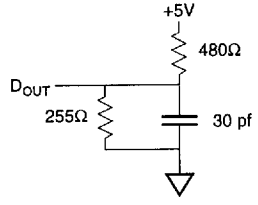


Figure 1. Output Load Equivalent

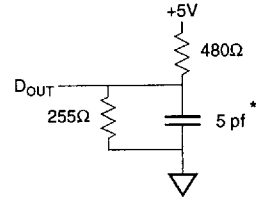
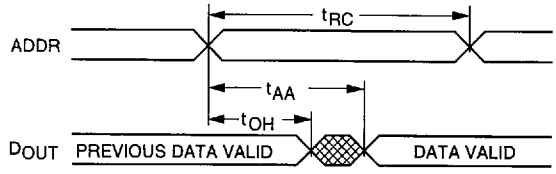
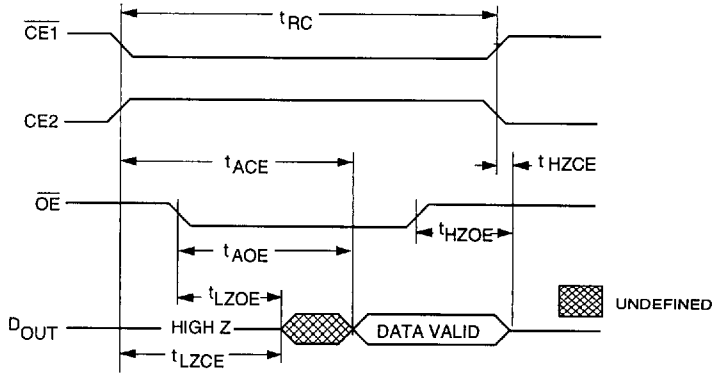


Figure 2. Output Load Equivalent
(for t_{LZCE}, t_{HZWE}, t_{LZWE}, t_{HZWE}, t_{LZOE}, t_{HZOE})

Read Cycle No. 1[6, 7]



Read Cycle No. 2[3, 6, 8] For JEDEC Version

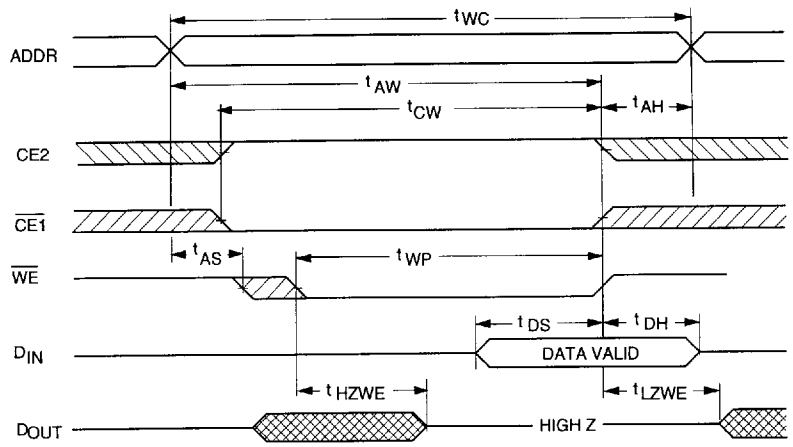


AC Electrical Characteristics (V_{CC} = 5V ± 10%, All Temperature Ranges)

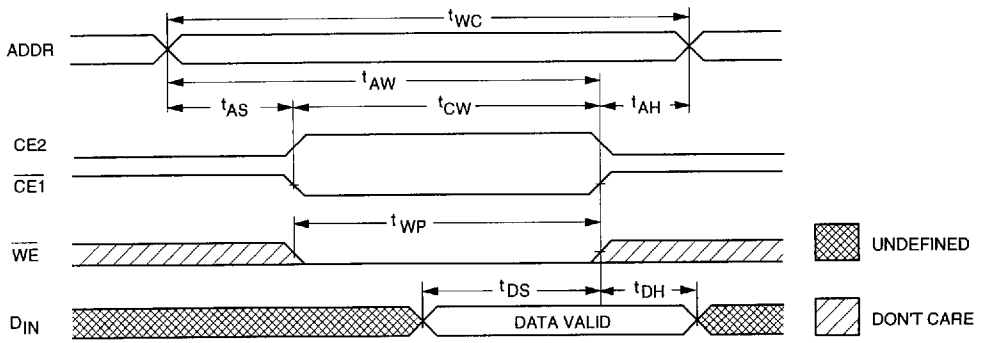
Description		-20		-25		-35		
READ Cycle	Symbol	Min.	Max.	Min.	Max.	Min.	Max.	Units
READ Cycle time	t_{RC}	20		25		35		ns
Address access time	t_{AA}		20		25		35	ns
Chip enable access time	t_{ACE}		20		25		35	ns
Output hold from address change	t_{OH}	3		3		3		ns
Chip enable to output in low Z[2, 4]	t_{LZCE}	5		5		5		ns
Chip disable to output in high Z[2, 3, 4]	t_{HZCE}		10		10		15	ns
Chip enable to power up time[4]	t_{PU}	0		0		0		ns
Chip disable to power down time	t_{PD}		20		25		35	ns
Output enable access time	t_{AOE}		8		8		12	ns
Output Enable to output in low Z[2, 4]	t_{LZOE}	0		0		0		ns
Output disable to output in high Z[2, 4]	t_{HZOE}		8		10		12	ns

Notes referenced are after Data Retention Table.

Write Cycle No. 1 (Write Enable Controlled)



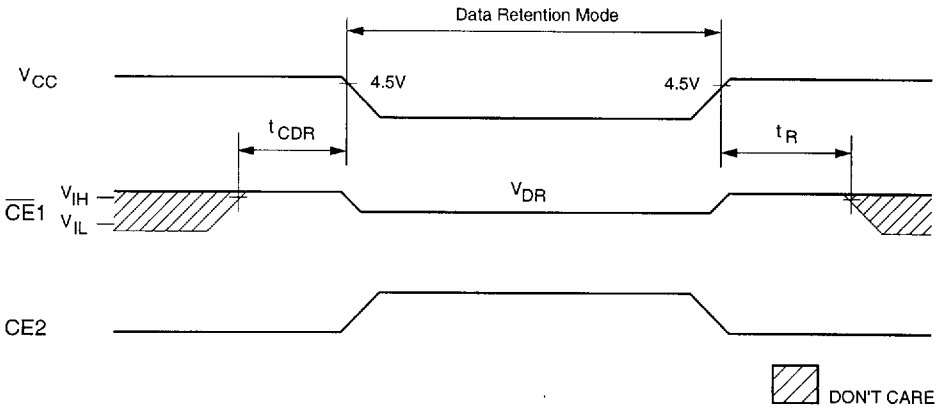
Write Cycle No. 2 (Chip Enable Controlled)



AC Electrical Characteristics (V_{CC} = 5V ± 10%, All Temperature Ranges)

Description		-20		-25		-25[1]		-35		
WRITE Cycle	**Symbol**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
WRITE Cycle time	t_{WC}	20		25		25		35		ns
Chip enable to end of write	t_{CW}	15		15		20		20		ns
Address Valid to end of write	t_{AW}	15		15		20		20		ns
Address setup time	t_{AS}	0		0		0		0		ns
Address hold from end of write	t_{AH}	0		0		0		0		ns
Write pulse width	t_{WP}	15		15		20		20		ns
Data setup time	t_{DS}	10		12		15		15		ns
Data hold time	t_{DH}	0		0		0		0		ns
Write disable to output in low Z[2, 4]	t_{LZ}	0		0		0		0		ns
Write enable to output in high[2, 4]	t_{HZWE}		8		10		10		15	ns

Low V_{CC} Data Retention Waveform



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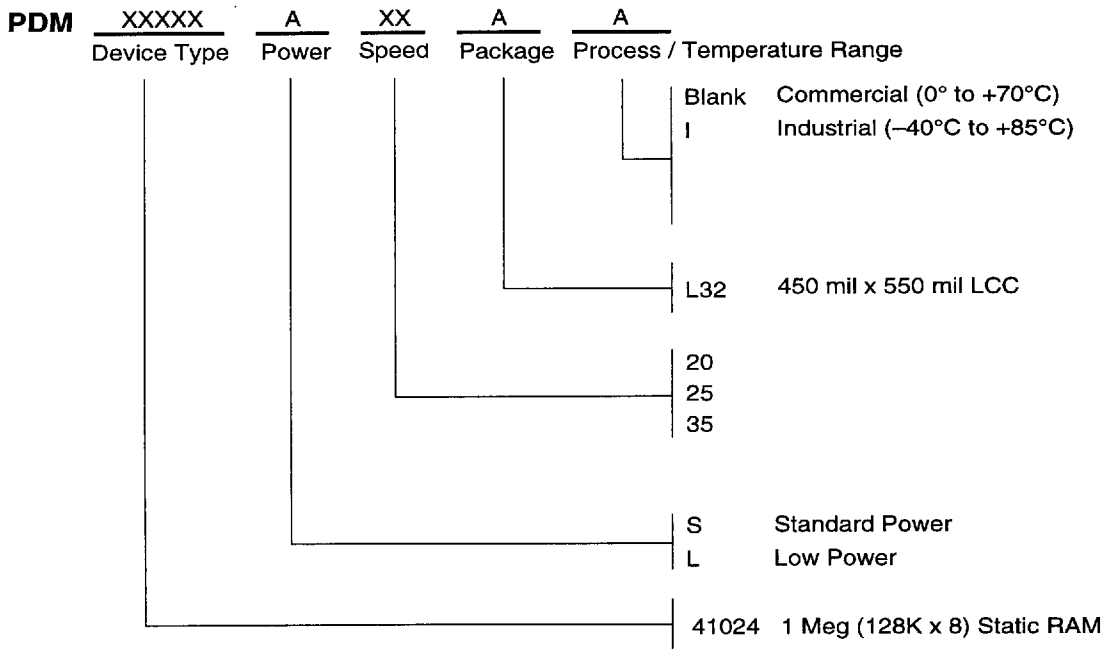
Data Retention Electrical Characteristics (L Version Only)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{DR}	V_{CC} for Retention Data			2	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CE1} \geq V_{CC} - 0.2V$ or $CE2 \leq (V_{SS} + 0.2V)$ $V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$	$V_{CC} = 2V$	—	95	500	µA
			$V_{CC} = 3V$	—	350	750	µA
t_{CDR}	Chip Deselect to Data Retention Time			0	—	—	ns
t_R(4)	Operation Recovery Time			t_{RC}(5)	—	—	ns

NOTES: (For 3 previous Electrical Characteristics tables)

1. −55°C to +125°C temperature range only.
2. The parameter is tested with CL = 5 pF as shown in Fig. #2. Transition is measured ±200 mV from steady state voltage.
3. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}.
4. This parameter is sampled.
5. t_{RC} = Read cycle time.
6. $\overline{WE}$ is high for a READ cycle.
7. The device is continuously selected. All the Chip Enables are held in their active state.
8. The address is valid prior to or coincident with the latest occuring Chip Enable.

Ordering Information



Chip	Package Type
PDM41024	32-pin LCC