CYPRESS SEMICONDUCTOR

256K x 1 Static R/W RAM

Features

- **High speed**
  - **— t_{AA} = 10 ns**
- **BiCMOS for optimum speed/power**
- **Low active power**
  - **— 770 mW**
- **Low standby power**
  - **— 165 mW**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**

Functional Description

The CY7B197 is a high-performance BiCMOS static RAM organized as 256K words by 1 bit. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY7B197 has an automatic power-down feature, reducing the power consumption by more than 50% when deselected.

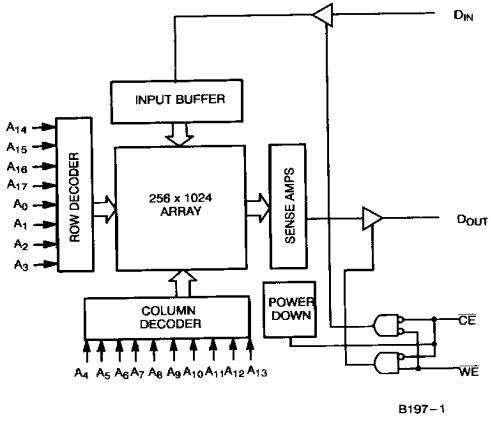
Writing to the device is accomplished by taking chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs LOW. Data on the input pin (D_{IN}) is written into the memory location specified on the address pins (A_0 through A_{17}).

Reading the device is accomplished by taking chip enable ($\overline{CE}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified by the address pins will appear on the data output (D_{OUT}) pin.

The output pin (D_{OUT}) is placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH) or during a write operation ($\overline{WE}$ LOW).

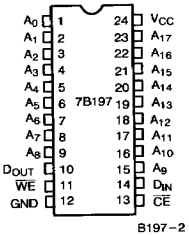
The CY7B197 is available in a leadless chip carrier and space-saving 300-mil-wide DIPs and SOJs. It utilizes a die coat to insure alpha immunity.

Logic Block Diagram



Pin Configurations

DIP
Top View



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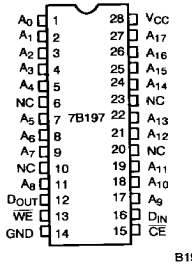
SOJ
Top View



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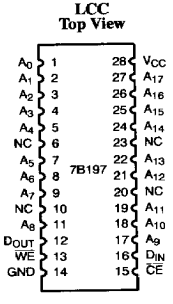
LCC
Top View



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Selection Guide

		7B197–10	7B197–12	7B197–15	7B197–20
Maximum Access Time (ns)		10	12	15	20
Maximum Operating Current (mA)	Commercial	140	130	125	
	Military		130	125	125
Maximum Standby Current (mA)	Commercial	30	30	30	
	Military		40	40	40

Shaded area contains advanced information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage on V_{CC} relative to GND[1] .. − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... − 0.5V to +7.0V

DC Input Voltage[1] ..... − 0.5V to +7.0V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	− 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameters	Description	Test Conditions		7B197−10 Min.	7B197−10 Max.	7B197−12 Min.	7B197−12 Max.	7B197−15, 20 Min.	7B197−15, 20 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 0.8 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]			− 0.3	0.8	− 0.3	0.8	−0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		− 10	+10	− 10	+10	− 10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		− 10	+10	− 10	+10	− 10	+10	μA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			− 300		− 300		− 300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		140		130		125	mA
			Mil				130		125	
I_{SB}	Automatic CE Power-Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 3.0V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V, f = 0	Com'l		30		30		30	mA
			Mil				40		40	

Shaded area contains advanced information.

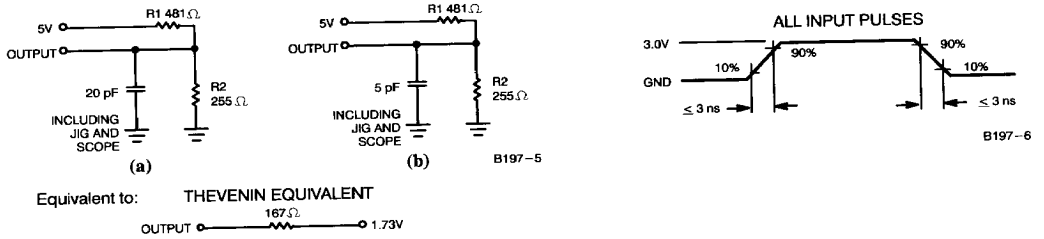
Capacitance[5]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

1. $V_{IL\,(Min)}$ = −2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Switching Characteristics Over the Operating Range[3,6]

Parameters	Description	7B197–10		7B197–12		7B197–15		7B197–20		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	10		12		15		20		ns
t_{AA}	Address to Data Valid		10		12		15		20	ns
t_{OHA}	Output Hold from Address Change	3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		10		12		15		20	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7]	3		3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7, 8]		5		7		8		10	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		10		12		15		20	ns
WRITE CYCLE[9]										
t_{WC}	Write Cycle Time	10		12		15		20		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	8		9		10		15		ns
t_{AW}	Address Set-Up to Write End	8		9		10		15		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	8		9		10		15		ns
t_{SD}	Data Set-Up to Write End	6		7		8		10		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]	2		2		2		2		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7, 8]		5		7		7		10	ns

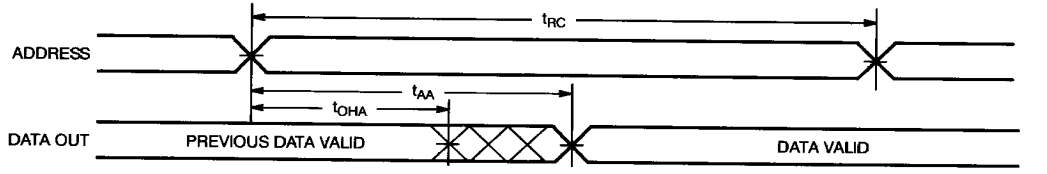
Shaded area contains advanced information.

Notes:

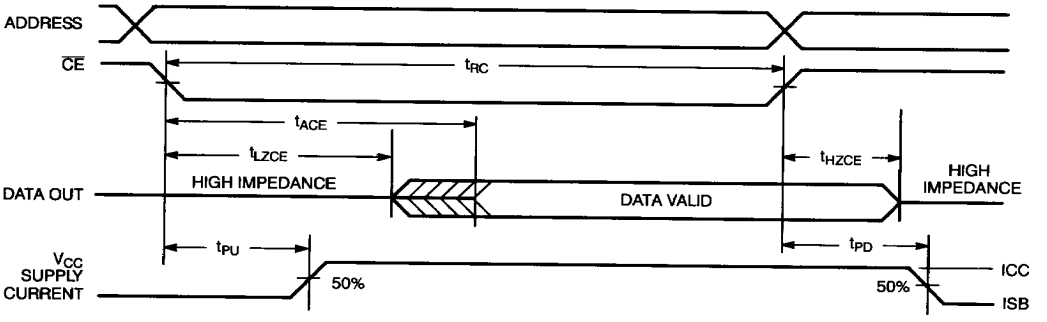
6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 20 pF load capacitance.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} and t_{HZWE} is less than t_{LZWE} for any given device.
8. t_{HZCE} and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) in AC Test Loads and Waveforms. Transition is measured ±500 mV from steady state voltage.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal will terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

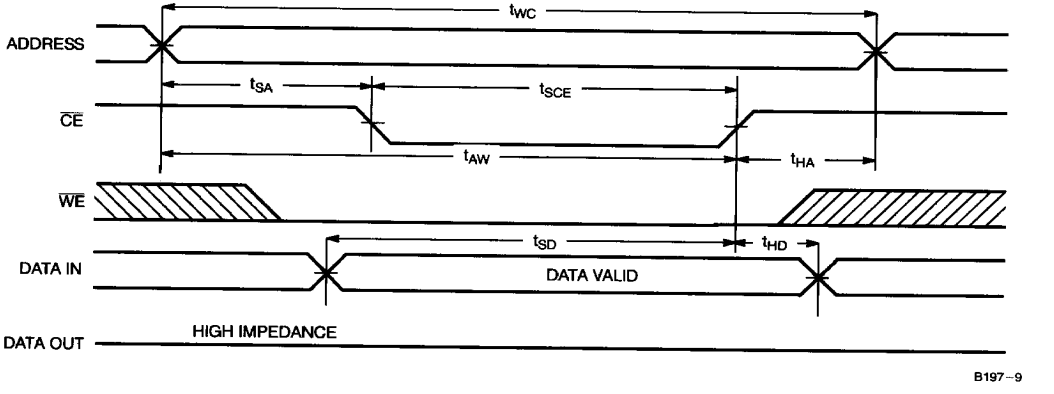
Read Cycle No. 1[10, 11]



Read Cycle No. 2[10, 12]



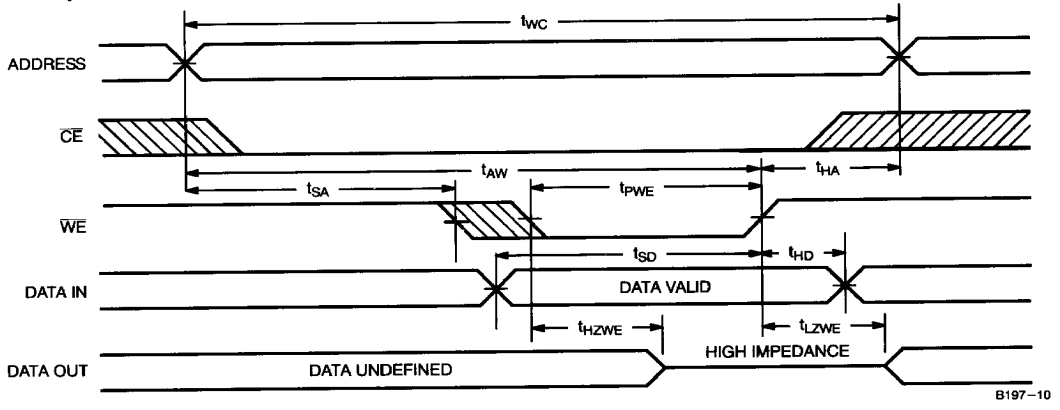
Write Cycle No. 1 ($\overline{CE}$ Controlled)[13]



Notes:
10. $\overline{WE}$ is HIGH for read cycle.
11. Device is continuously selected, $\overline{CE} = V_{IL}$.
12. Address Valid prior to or coincident with $\overline{CE}$ transition LOW.
13. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{WE}$ Controlled)[13]



7B197 Truth Table

$\overline{CE}$	$\overline{WE}$	D_{OUT}	Mode	Power
H	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	Data Out	Read	Active (I_{CC})
L	L	High Z	Write	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
10	CY7B197–10DC	D14	Commercial
	CY7B197–10LC	TBD	
	CY7B197–10PC	P13	
	CY7B197–10VC	V21	
12	CY7B197–12DC	D14	Commercial
	CY7B197–12LC	TBD	
	CY7B197–12PC	P13	
	CY7B197–12VC	V21	
	CY7B197–12DMB	D14	Military
	CY7B197–12LMB	TBD	

Speed (ns)	Ordering Code	Package Type	Operating Range
15	CY7B197–15DC	D14	Commercial
	CY7B197–15LC	TBD	
	CY7B197–15PC	P13	
	CY7B197–15VC	V21	
	CY7B197–15DMB	D14	Military
	CY7B197–15LMB	TBD	
20	CY7B197–20DMB	D14	Military
	CY7B197–20LMB	TBD	

Shaded area contains advanced information.

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Document #: 38–00159–B