SY89113U

2.5V Low Jitter, Low Skew 1:12 LVDS Fanout Buffer with 2:1 Input MUX and Internal Termination

General Description

The SY89113U is a 2.5V low jitter, low skew, 1:12 LVDS fanout buffer optimized for precision telecom and enterprise server distribution applications. The input includes a 2:1 MUX for clock switchover applications. Unlike other multiplexers, this input includes a unique isolation design that minimizes channel-to-channel crosstalk. The SY89113U distributes clock frequencies from DC to >1GHz guaranteed over temperature and voltage. The SY89113U incorporates a synchronous output enable (EN) so that the outputs will only be enabled/disabled when they are already in the LOW state.

CLK0 differential input includes Micrel's unique, 3-pin input termination architecture that directly interfaces to any differential signal (AC- or DC-coupled) as small as 100mV ($200mV_{PP}$) without any level shifting or termination resistor networks in the signal path.

CLK1 differential input includes a new version of Micrel's unique, Any-Input architecture that directly interfaces with single-ended TTL/CMOS logic (including 3.3V logic), single-ended LVPECL, differential (AC- or DC-coupled) LVDS, HSTL, CML, and LVPECL logic levels as small as 200mV ($400mV_{PP}$). CLK1 input requires external termination.

LVDS output swing 325mV into 100Ω with extremely fast rise/fall time guaranteed to be less than 250ps.

The SY89113U operates from a 2.5V±5% supply and is guaranteed over the full industrial temperature range of -40°C to +85°C. The SY89113U is part of Micrel's high-speed, Precision Edge® product line.

All support documentation can be found on Micrel's web site at: www.micrel.com.

Precision Edge®

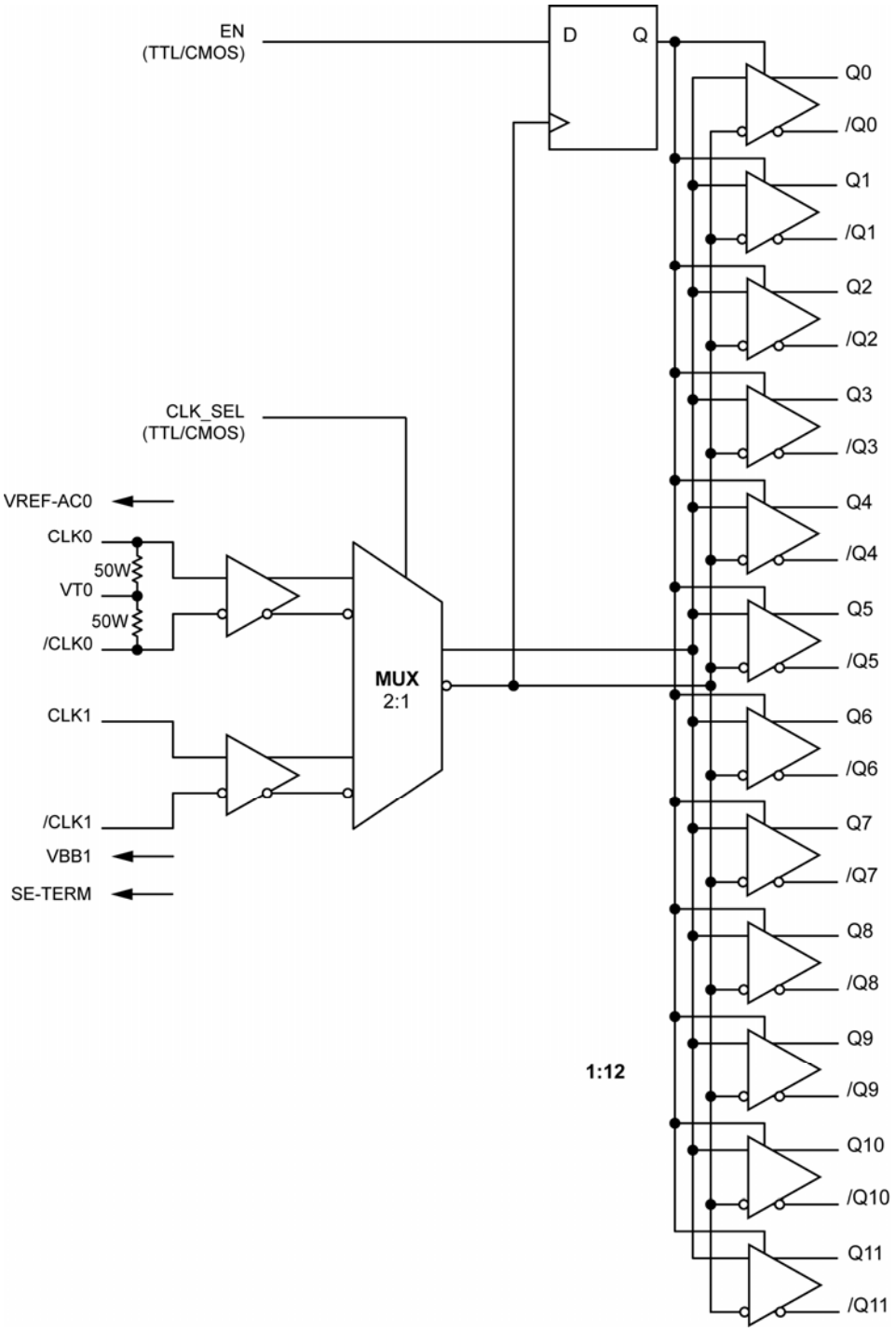
Features

- Selects between 1 of 2 inputs, and provides 12 precision, low skew LVDS output copies
- Guaranteed AC performance over temperature and voltage:
  - DC to >1GHz throughput
  - <975ps propagation delay CLK0-to-Q
  - <250ps rise/fall time
  - <25ps output-to-output skew
- Ultra-low jitter design:
  - $<1ps_{RMS}$ random jitter
  - $<10ps_{PP}$ total jitter (clock)
  - $<1ps_{RMS}$ cycle-to-cycle jitter
  - $<0.7ps_{RMS}$ crosstalk induced jitter
- Unique, patent-pending 2:1 input MUX provides superior isolation to minimize channel-to-channel crosstalk
- CLK0 input features a unique, patent-pending input termination and VT pin that accepts AC- and DC-coupled inputs (CML, LVPECL, LVDS)
- CLK1 accepts virtually any logic standard:
  - Single-ended: TTL/CMOS (including 3.3V logic), LVPECL
  - Differential: LVPECL, LVDS, CML, HSTL
- 325mV LVDS-compatible output swing
- Power supply: 2.5V ±5%
- Industrial temperature range –40°C to +85°C
- Available in 44-pin (7mm x 7mm) MLF™ package

Applications

- Multi-processor server
- SONET/SDH clock/data distribution
- Fibre Channel distribution
- Gigabit Ethernet clock distribution

Functional Block Diagram



hbwhelp@micrel.com or (408) 955-1690

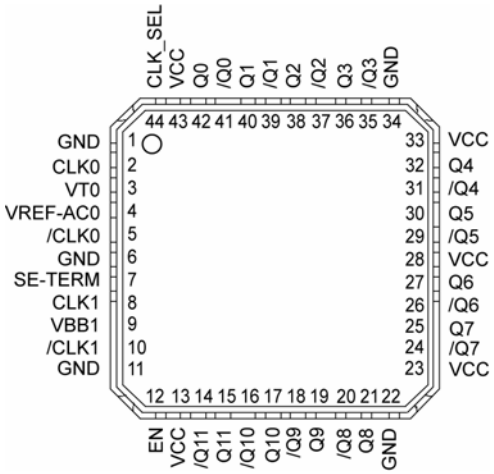
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89113UMG	MLF-44	Industrial	SY89113U with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY89113UMGTR[2]	MLF-44	Industrial	SY89113U with Pb-Free bar-line indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.

Pin Configuration



44-Pin MLF™ (MLF-44)

Truth Table

EN	CLK_SEL	Q	/Q
H	L	CLK0	/CLK0
H	H	CLK1	/CLK1
L	X	L[1]	H[1]

Note:

1. Transition occurs on next negative transition of the non-inverted input.

hbwhelp@micrel.com or (408) 955-1690

Pin Description

Pin Number	Pin Name	Pin Function
1, 6, 11, 22, 34	GND, Exposed Pad	Ground. GND pins and exposed pad must both be connected to the most negative potential of chip the ground.
2, 5	CLK0, /CLK0	Differential Inputs: This input pair is a differential signal input to the device. Input accepts AC- or DC-coupled signals as small as 100mV (200mV$_{PP}$). Each pin of the pair internally terminates to a VT pin through 50Ω. Note that this input defaults to an indeterminate state if left open. Please refer to the "CLK0 Input Interface Applications" section for more details.
3	VT0	Input Termination Center-Tap: Each side of the differential input pair CLK0, /CLK0 terminates to the VT pin. The VT pin provides a center-tap to a termination network for maximum interface flexibility. See “CLK0 Input Interface Applications” section for more details. For DC-coupled CML or LVDS inputs, the VT pin is left floating.
4	VREF-AC0	Reference Voltage: This output biases to V_{CC}–1.2V. It is used when AC-coupling the input CLK0. For AC-coupled applications, connect VREF-AC0 to the VT0 pin and bypass with 0.01µF low ESR capacitor to V_{CC}. See “CLK0 Input Interface Applications” section for more details. Maximum sink/source current is ±1.5mA. Due to the limited drive capability, the VREF-AC0 pin is only intended to drive its respective input pin.
7	SE-TERM	Input Termination Pin: When CLK1 is driven by a single-ended TTL/CMOS signal, tie this pin to GND. In all other modes, let this pin float. See “CLK1 Interface Applications” section for more details.
8, 10	CLK1, /CLK1	Differential Inputs: This input pair is a differential signal input to the device. This input accepts Any-Logic standard as small as 200mV (400mV$_{PP}$). Note that this input defaults to an indeterminate state if left open. Tie either the true or the complement input to ground while the other input is floating. This input can be used for single-ended signals (including TTL/CMOS signals from a 3.3V driver). See “CLK1 Input Interface Applications” section for more details.
9	VBB1	Reference Voltage: This output biases to V_{CC}–1.425V. VBB1 is designed to act as a switching reference for the CLK1 and /CLK1 inputs when configured in single-ended PECL input mode. VBB1 can be used for AC-coupling of CLK1, see Figure 4d for details. Maximum sink/source current is ±1.5mA. Due to the limited drive capability, the VBB1 pin is only intended to drive its respective input pin.
12	EN	This single-ended, TTL/CMOS-compatible input functions as a synchronous output enable. The synchronous enable ensures that enable/disable will only occur when the outputs are in a logic LOW state. Note that this input is internally connected to a 25kΩ pull-up resistor and will default to logic HIGH state (enable) if left open.
13, 23, 28, 33, 43	VCC	Positive power supply. Bypass with 0.1µF//0.01µF low ESR capacitors and place as close to the VCC pins as possible.
44	CLK_SEL	This single-ended, TTL/CMOS-compatible input selects the inputs to the multiplexer. Note that this input is internally connected to a 25kΩ pull-up resistor and will default to logic HIGH state if open.
42, 41 40, 39 38, 37 36, 35 32, 31 30, 29 27, 26 25, 24 21, 20 19, 18 17, 16 15, 14	Q0, /Q0 Q1, /Q1 Q2, /Q2 Q3, /Q3 Q4, /Q4 Q5, /Q5 Q6, /Q6 Q7, /Q7 Q8, /Q8 Q9, /Q9 Q10, /Q10 Q11, /Q11	Differential LVDS Outputs: These LVDS output pairs are the precision, low skew copies of the selected input. Please refer to the, “Truth Table” below for details. Unused output pairs should be terminated with 100Ω across the pair. Each output is designed to drive 325mV into 100Ω. See the “LVDS Output Interface Applications” section for more details.

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage
(Differential Input CLK0, CLK1[4, 5]) .. –0.5V to V_{CC}
Current on Reference Voltage Outputs
Source or sink current on VREF-AC0, VBB1 ..... ±2mA
Termination Current
Source or sink current on VT0 ..... ±100mA
Input Current
Source or sink current on CLK0, /CLK0 ... ±50mA
Lead Temperature (soldering, 20 sec.) ..... +260°C
Storage Temperature (T_s) ..... –65°C to 150°C

Operating Ratings[2]

Supply Voltage (V_{CC}) ..... +2.375V to +2.625V
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance[3]
MLF™ (θ_{JA})
Still-Air ..... 24°C/W
MLF™ (ψ_{JB})
Junction-to-Board ..... 8°C/W

DC Electrical Characteristics[6]

T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply		2.375		2.625	V
I_{CC}	Power Supply Current	No load, max. V_{CC}		240	330	mA
R_{IN}	Input Resistance (CLK0-to-V_T)		45	50	55	Ω
R_{DIFF_IN}	Differential Input Resistance (CLK0-to-/CLK0)		90	100	110	Ω
V_{IH}	Input High Voltage (CLK0, /CLK0)		1.2		V_{CC}	V
	(CLK1, /CLK1)	Note 4	0.2		V_{CC}	V
		Note 5	1.2		3.6	
V_{IL}	Input Low Voltage (CLK0, /CLK0)		0.1		V_{CC}	V
	(CLK1, /CLK1)	Note 4	0.2			V
		Note 5	0			V
V_{IN}	Input Voltage Swing (CLK0, /CLK0)	See Figure 1a.	0.1		V_{CC}	V
	(CLK1, /CLK1)	See Figure 1a.	0.2			V
V_{DIFF_IN}	Differential Input Voltage Swing |CLK0-to-/CLK0|	See Figure 1b.	0.2			V
	|CLK1-to-/CLK1|	See Figure 1b.	0.4			V
V_{T0}	CLK0-to-V_{T0} (CLK0, /CLK0)				1.28	V
$V_{REF-AC0}$	Output Reference Voltage		V_{CC}–1.3	V_{CC}–1.2	V_{CC}–1.1	V
V_{BB1}	Output Reference Voltage		V_{CC}–1.525	V_{CC}–1.425	V_{CC}–1.325	V

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB. θ_{JA} and Ψ_{JB} values are determined for a 4-layer board in still-air, unless otherwise stated.
4. SE-TERM not connected.
5. Using single-ended TTL/CMOS input signals, SE-TERM connects to GND. See Figure 4f.
6. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

hbwhelp@micrel.com or (408) 955-1690

LVDS Outputs DC Electrical Characteristics[7]

V_{CC} = +2.5V ±5%; T_A = –40°C to +85°C; R_L = 100Ω across the output pair, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OUT}	Output Voltage Swing Q, /Q	See Figure 1a.	250	325		mV
$V_{DIFF-OUT}$	Differential Output Voltage Swing Q, /Q	See Figure 1b.	500	650		mV
V_{OCM}	Output Common Mode Voltage		1.125		1.275	V
ΔV_{OS}	Change in V_{OS} between complementary output states				25	mV

LVTTL/CMOS DC Electrical Characteristics[7]

V_{CC} = +2.5V ±5%; T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current		–125		30	µA
I_{IL}	Input LOW Current		–300			µA

Note:

7. The circuit is designed to meet the DC specifications, shown in the above table, after thermal equilibrium has been established.

AC Electrical Characteristics[8]

V_{CC} = +2.5V ±5%; T_A = –40°C to + 85°C, R_L = 100Ω across the output pair, unless otherwise stated.

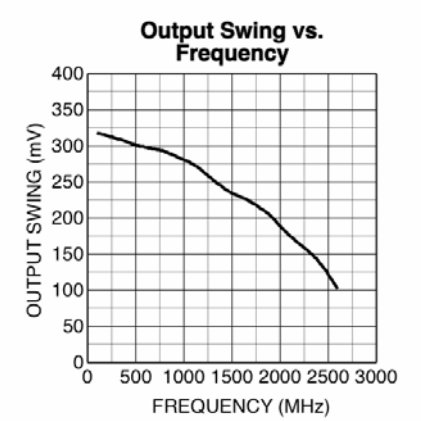
Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Operating Frequency	V_{OUT} ≥ 200mV	1			GHz
t_{PD}	Propagation Delay					
	CLK0-to-Q	V_{IN} ≥ 100mV	625	750	975	ps
	CLK1-to-Q	V_{IN} ≥ 200mV	700	900	1200	ps
	CLK_SEL-to-Q		500	700	900	ps
t_{PD} Tempco	Differential Propagation Delay Temperature Coefficient			90		fs/°C
t_S	Set-up Time					
	EN-to-CLK0	Note 9	100			ps
	EN-to-CLK1	Note 9	0			ps
t_H	Hold Time					
	CLK0-to-EN	Note 9	500			ps
	CLK1-to-EN	Note 9	600			ps
t_{SKEW}	Output-to-Output Skew	Note 10			25	ps
	Part-to-Part Skew CLK0	Note 11			200	ps
	Part-to-Part Skew CLK1	Note 11			250	ps
t_{JITTER}	Cycle-to-Cycle Jitter	Note 12			1	ps_{RMS}
	Random Jitter (RJ)	Note 13			1	ps_{RMS}
	Total Jitter (TJ)	Note 14			10	ps_{PP}
	Adjacent Channel Crosstalk-induced Jitter	Note 15			0.7	ps_{RMS}
t_r, t_f	Output Rise/Fall Time (20% to 80%)	At full output swing.	80	150	250	ps

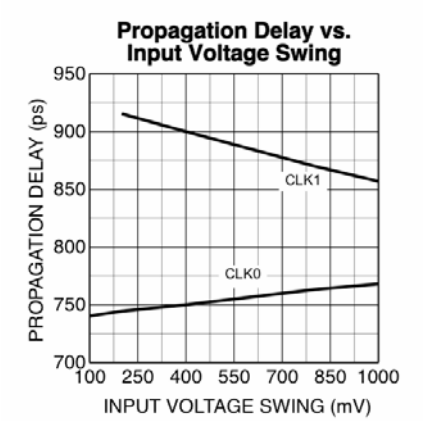
Notes:

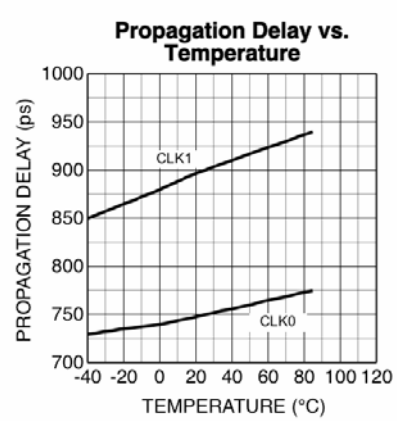
8. High-frequency AC-parameters are guaranteed by design and characterization.
9. Set-up and hold times apply to synchronous applications that intend to enable/disable before the next clock cycle. For asynchronous applications, set-up and hold do not apply.
10. Output-to-output skew is measured between two different outputs under identical input transitions.
11. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs
12. Cycle-to-cycle jitter definition: the variation of periods between adjacent cycles, $T_n - T_{n-1}$ where T is the time between rising edges of the output signal.
13. Random jitter is measured with a K28.7 character pattern, measured at $<f_{MAX}$.
14. Total jitter definition: with an ideal clock input of frequency $<f_{MAX}$, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.
15. Crosstalk-induced jitter is defined as: the added jitter that results from signals applied to two adjacent channels. It is measured at the output while applying two similar, differential clock frequencies that are asynchronous with respect to each other at the inputs.

Typical Operating Characteristics

V_{CC} = 2.5V, GND = 0, V_{IN} = 400mV, R_L = 100Ω across the output pair; T_A = 25°C, unless otherwise stated.

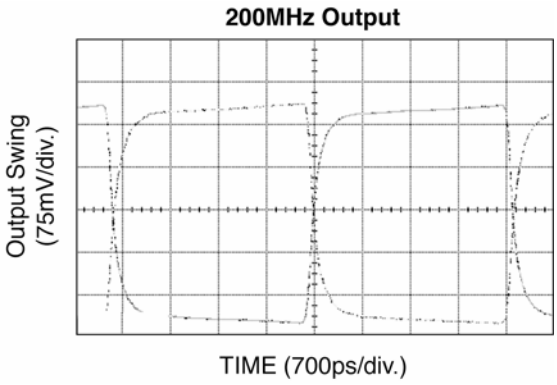


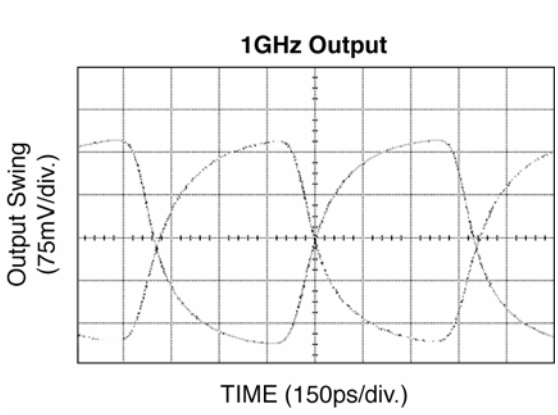




Functional Characteristics

V_{CC} = 2.5V, GND = 0, V_{IN} = 400mV, R_L = 100Ω across the output pair; T_A = 25°C, unless otherwise stated.





hbwhelp@micrel.com or (408) 955-1690

Single-Ended and Differential Swings

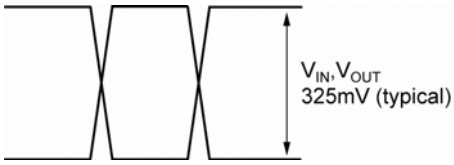


Figure 1a. Single-Ended Voltage Swing CLK0

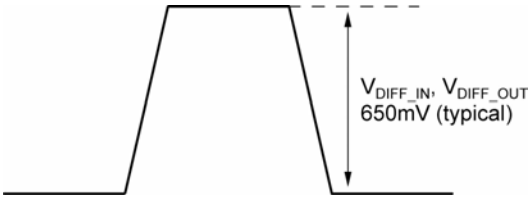
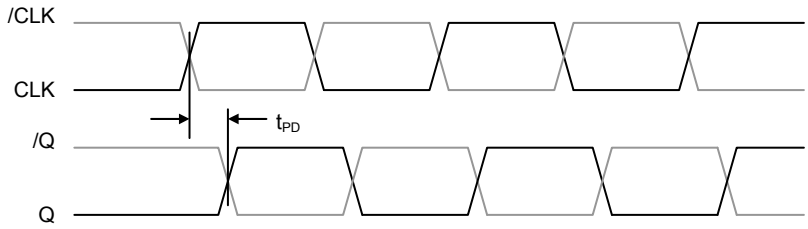
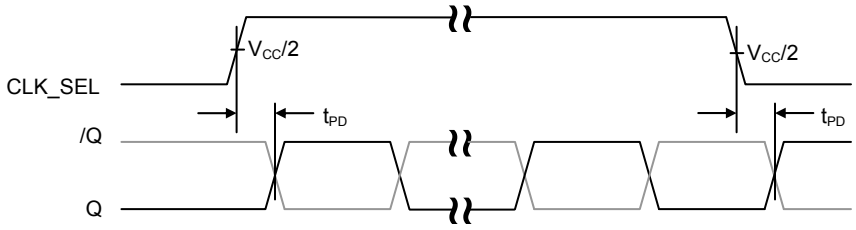


Figure 1b. Differential Voltage Swing CLK0

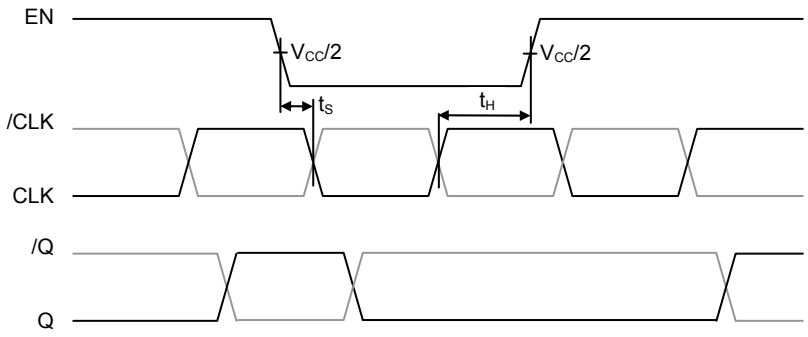
Timing Diagrams



Differential In-to-Differential Out



CLK_SEL-to-Differential Out



Set-Up and Hold Time EN-to-Differential IN

Input and Output Stages

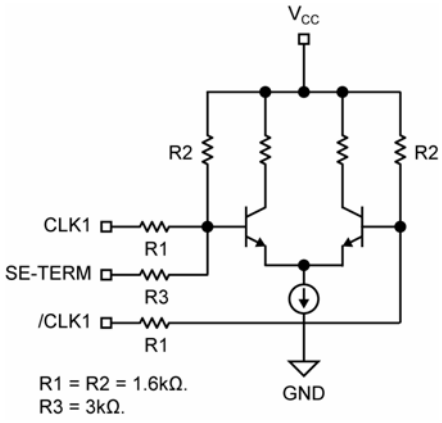


Figure 2a. CLK1 Differential Input Structure

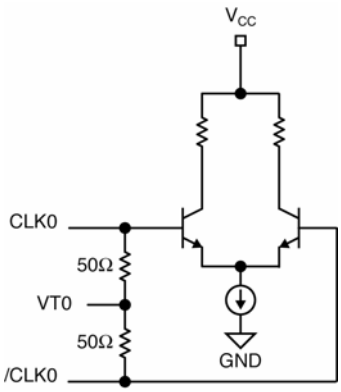


Figure 2b. CLK0 Differential Input Structure

CLK0 Input Interface Applications

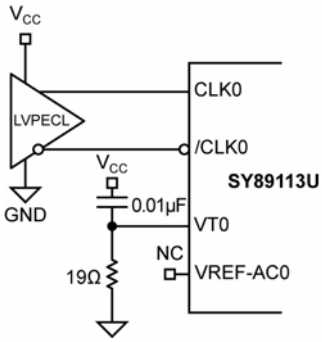


Figure 3a. LVPECL Interface (DC-Coupled)

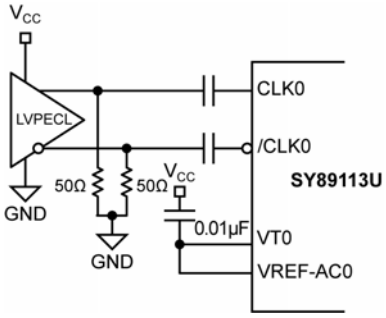
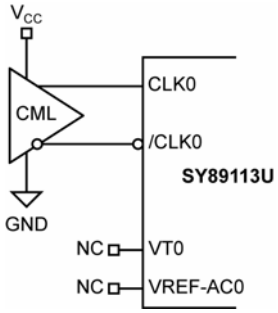


Figure 3b. LVPECL Interface (AC-Coupled)



option: may connect VT to V_{CC}

Figure 3c. CML Interface (DC-Coupled)

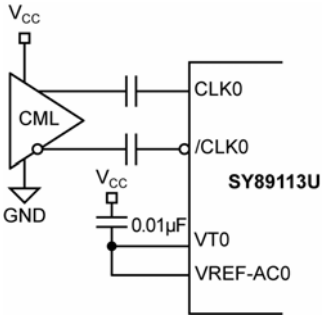


Figure 3d. CML Interface (AC-Coupled)

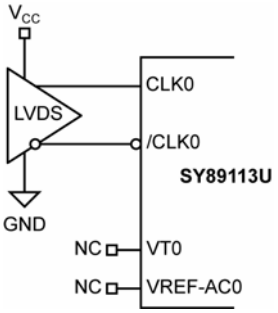


Figure 3e. LVDS Interface

hbwhelp@micrel.com or (408) 955-1690

CLK1 Input Interface Applications

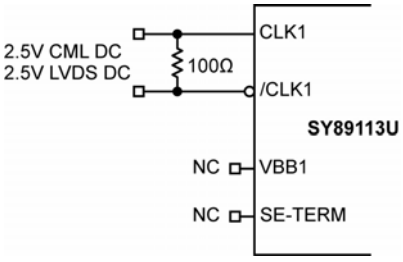


Figure 4a. CML, LVDS Interface (DC-Coupled)

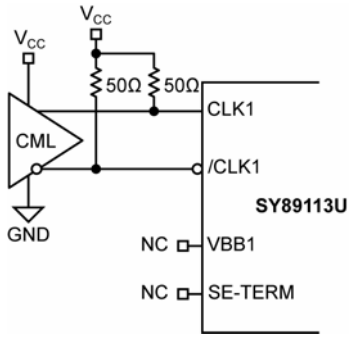


Figure 4b. CML Interface (DC-Coupled)

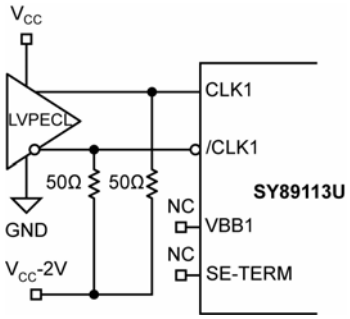


Figure 4c. PECL Interface (DC-Coupled)

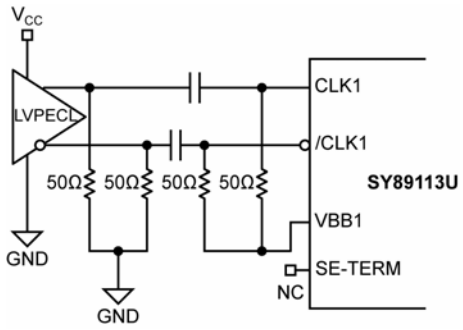


Figure 4d. PECL Interface (AC-Coupled)

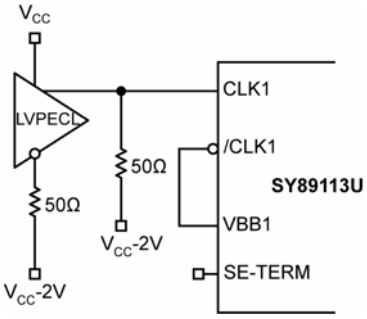
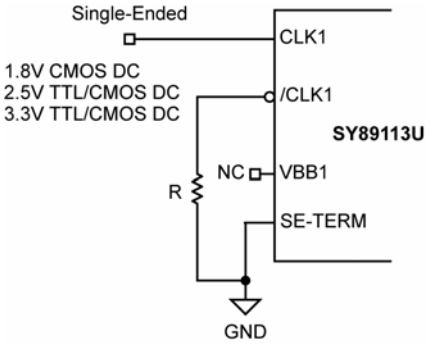


Figure 4e. PECL Interface (Single-Ended)



(See Single-Ended TTL/CMOS Recommended Resistor Table for Recommended Resistor Value R)

Figure 4f. TTL/CMOS Interface (Single-Ended)

Single-Ended TTL/CMOS Recommended Resistor Value

The SY89113U can be driven by a TTL/CMOS input signal. See Figure 4f. The resistor R, in Table 1, below is calculated according to the following equation:

$$R = 1.594 \times \left[\frac{1}{\frac{5.057 \times V_{CC}}{2 \times V_{CC} + V_{IH} + V_{IL}} - 1} - 1 \right] \Omega$$

The equation above is used to determine the optimum value of R for best duty cycle.

	Recommended R (Ω)
1.8V CMOS	261
2.5V CMOS	732
3.3V CMOS	1470

Table 1. Single-Ended TTL/CMOS Recommended Resistors

LVDS Output Interface Applications

LVDS specifies a small swing of 325mV typical, on a nominal 1.2V common mode above ground. The common mode voltage has tight limits to permit large variations in ground between an LVDS driver and receiver. Also, change in common mode voltage, as a function of data input, is kept to a minimum, to keep EMI low.

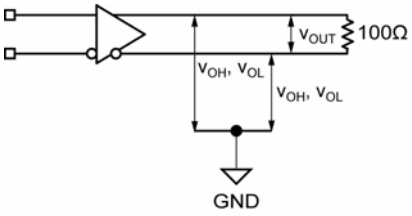


Figure 5a. LVDS Differential Measurement

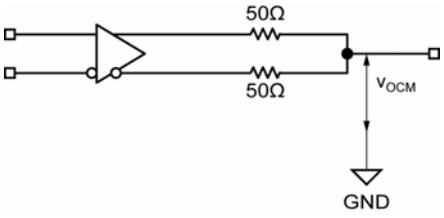
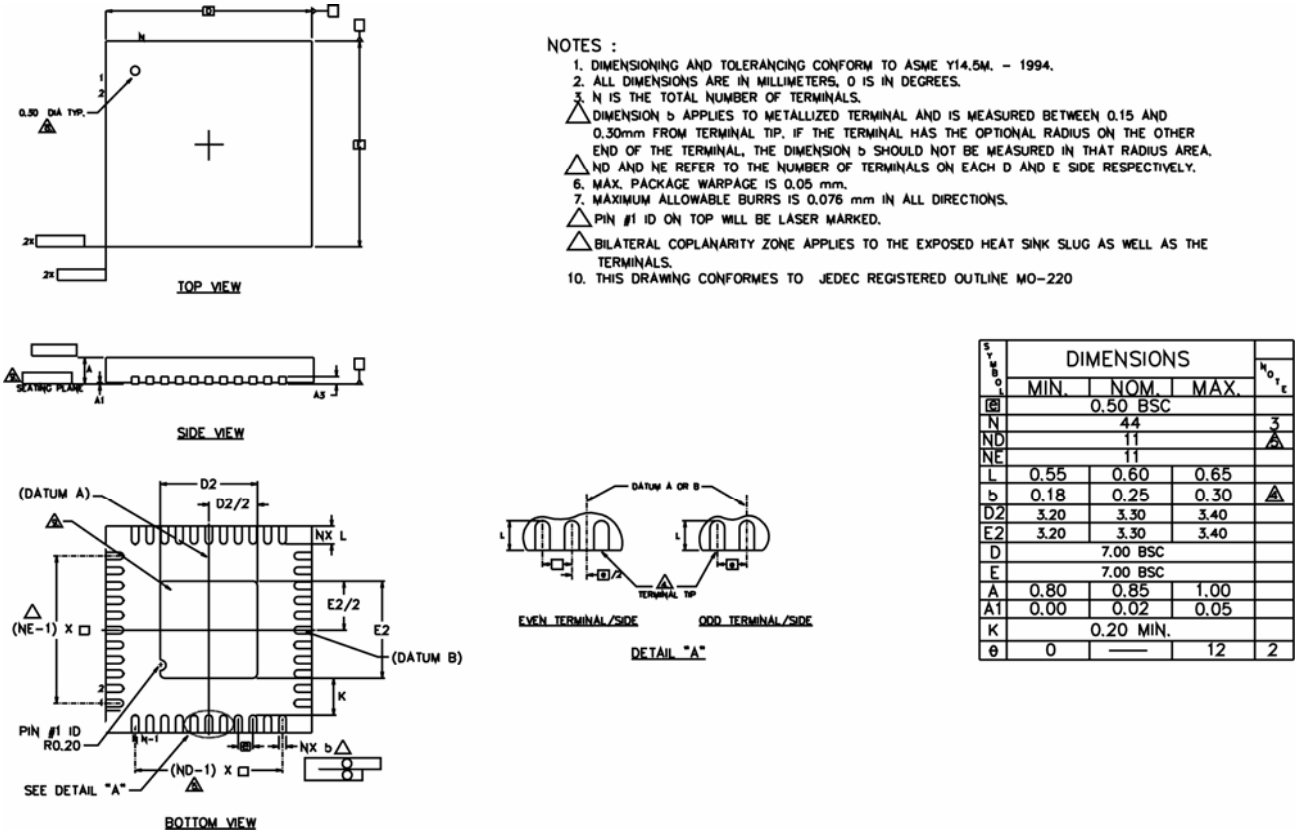


Figure 5b. LVDS Common Mode Measurement

Related Product and Support Documentation

Part Number	Function	Data Sheet Link
SY89112U	2.5/3.3V Low Jitter, Low Skew 1:12 LVPECL Fanout Buffer with 2:1 Input MUX and Internal Termination	http://www.micrel.com/product-info/products/sy89112u.shtml
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml
	MLF™ Application Note	www.amkor.com/products/notes_papers/MLFAppNote.pdf

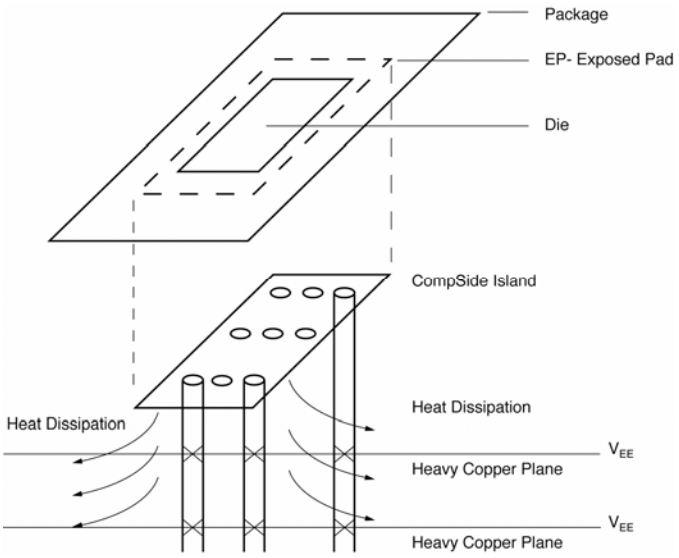
Package Information



NOTES :
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M. – 1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. θ IS IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
6. MAX. PACKAGE WARPAGE IS 0.05 mm.
7. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LASER MARKED.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
10. THIS DRAWING CONFORMES TO JEDEC REGISTERED OUTLINE MO-220

SYMBOL	DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		44		3
ND		11		5
NE		11		
L	0.55	0.60	0.65	
b	0.18	0.25	0.30	4
D2	3.20	3.30	3.40	
E2	3.20	3.30	3.40	
D		7.00 BSC		
E		7.00 BSC		
A	0.80	0.85	1.00	
A1	0.00	0.02	0.05	
K		0.20 MIN.		
θ	0	—	12	2

44-Pin MLF™ (MLF-44)



44-Pin MLF™ (MLF-44)

Package Notes:

1. Package meets Level 2 moisture sensitivity classification, and is shipped in dry pack form.
2. Exposed pads must be soldered to a ground for proper thermal management.

hbwhelp@micrel.com or (408) 955-1690

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http:/www.micrel.com